

REVISIONS

LT#	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
查询"5962-9862101QFA"供应商			

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19															
REV STATUS OF SHEETS	REV																			
	SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14				
PMIC N/A	PREPARED BY Joseph A. Kerby				DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216															
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles F. Saffle, Jr.				MICROCIRCUITS, DIGITAL, ADVANCED CMOS, CRYSTAL CLOCK GENERATOR, MONOLITHIC SILICON															
	APPROVED BY Monica L. Poelking																			
	DRAWING APPROVAL DATE 98-12-21				SIZE A	CAGE CODE 67268	5962-98621													
	REVISION LEVEL				SHEET 1 OF 19															

DSCC FORM 2233
APR 97

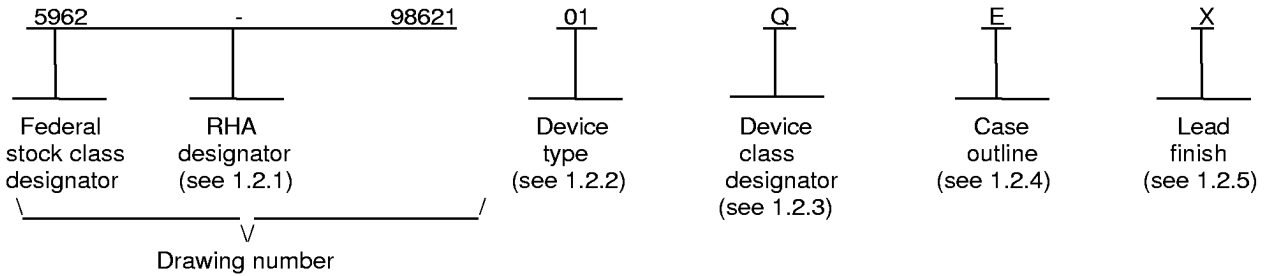
5962-E057-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 [查询"5962-9862101QEA"供应商](#) Scope. This drawing documents the product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ACT3301	Crystal Clock Generator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/ 2/ 3/

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Supply voltage range (V_{CC}).....	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}).....	-0.5 V dc to +7.0 V dc
DC output voltage range (V_{OUT}).....	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC input diode current (I_{IK}).....	± 9 mA
DC output diode current (I_{OK}).....	± 20 mA
DC output source or sink current (I_{OUT}).....	± 70 mA
Maximum power dissipation (P_D).....	500 mW
Storage temperature range (T_{STG}).....	-65°C to +150°C
Lead temperature (soldering, 10 seconds).....	+300°C
Thermal resistance, junction-to-case (θ_{JC}).....	See MIL-STD-1835
Junction temperature (T_J).....	+175°C 4/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC}).....	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}).....	+0.0 V dc to +5.5 V dc
Output voltage range (V_{OUT}).....	+0.0 V dc to V_{CC} V dc
Maximum low level input voltage (V_{IL1}) (OEH, <u>OEL</u>).....	0.8 V dc
Minimum high level input voltage (V_{IH1}) (OEH, OEL).....	2.0 V dc
Maximum low level input voltage (V_{IL2}) (DIVA).....	30% V_{CC}
Minimum high level input voltage (V_{IH2}) (DIVA).....	70% V_{CC}
Maximum low level input voltage (V_{IL3}) (OSC_DR, DIVB).....	10% V_{CC}
One-half input voltage level ($V_{1/2}$) (OSC_DR, DIVB).....	50% V_{CC}
Minimum high level input voltage (V_{IH3}) (OSC_DR, DIVB).....	90% V_{CC}
Maximum high level output current (I_{OH}).....	-48 mA
Maximum low level output current (I_{OL}).....	+48 mA
Case operating temperature range (T_C).....	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

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2. APPLICABLE DOCUMENTS

2.1 Government specification standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

- MIL-STD-883 - Test Method Standard Microcircuits.
- MIL-STD-973 - Configuration Management.
- MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

- MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
- MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 20 - Standardized for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

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3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

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3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available on-site at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 39 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (2) T_A = +125°C, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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Table I. Electrical performance characteristics.

Test and test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and Device class	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Minimum high level input voltage (OEH, OEL)	V _{IH1} <u>4/</u>		All	4.5 V	1, 2, 3	2.0		V
			All	5.5 V	1, 2, 3	2.0		
Maximum low level input voltage (OEH, OEL)	V _{IL1} <u>4/</u>		All	4.5 V	1, 2, 3		0.8	V
			All	5.5 V	1, 2, 3		0.8	
Minimum high level input voltage (DIVA)	V _{IH2} <u>4/</u>		All	4.5 V	1, 2, 3	3.15		V
			All	5.5 V	1, 2, 3	3.85		
Maximum low level input voltage (DIVA)	V _{IL2} <u>4/</u>		All	4.5 V	1, 2, 3		1.35	V
			All	5.5 V	1, 2, 3		1.65	
Minimum high level input voltage (DIVB, OSC_DR)	V _{IH3} <u>4/</u>		All	4.5 V	1, 2, 3	4.05		V
			All	5.5 V	1, 2, 3	4.95		
Maximum low level input voltage (DIVB, OSC_DR)	V _{IL3} <u>4/</u>		All	4.5 V	1, 2, 3		0.45	V
			All	5.5 V	1, 2, 3		0.55	
Minimum 1/2 level input voltage (DIVB, OSC_DR)	V _{1/2} <u>4/</u>		All	4.5 V	1, 2, 3	1.8		V
			All	5.5 V	1, 2, 3	2.2		
Maximum 1/2 level input voltage (DIVB, OSC_DR)	V _{1/2} <u>4/</u>		All	4.5 V	1, 2, 3		2.7	V
			All	5.5 V	1, 2, 3		3.3	
High level output voltage (OUT) 3006	V _{OH1}	OEH = V _{IH1} , DIVA = V _{IH2} , OEL = GND, DIVB = V _{IH3} or V _{1/2} I _{OH} = -50 μA	All	4.5 V	1, 2, 3	4.4		V
			All	5.5 V	1, 2, 3	5.4		
			All	4.5 V	1, 2, 3	3.76		
			All	5.5 V	1, 2, 3	4.76		
		OEH, DIVA, DIVB = V _{CC} , OEL = GND I _{OH} = -48 mA	All	5.5 V	1, 2, 3	3.85		
		OEH, DIVA, DIVB = V _{CC} , OEL = GND I _{OH} = -75 mA <u>5/</u>	All	5.5 V	1, 2, 3			

See footnotes at end of table.

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Table I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified		Device type and Device class	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
							Min	Max	
High level output voltage, low drive (OSC_OUT) 3006	V _{OH2}	OSC_IN, OSC_DR = 0.0 V I _{OH} = -150 μA		All	4.5 V	1, 2, 3	3.46		V
				All	5.5 V	1, 2, 3	4.46		
High level output voltage, medium drive (OSC_OUT) 3006	V _{OH3}	OSC_IN = 0.0 V OSC_DR = V _{CC} I _{OH} = -600 μA		All	4.5 V	1, 2, 3	3.46		V
				All	5.5 V	1, 2, 3	4.46		
High level output voltage, high drive (OSC_OUT) 3006	V _{OH4}	OSC_IN = 0.0 V I _{OH} = -1.0 mA	OSC_DR = 2.25 V	All	4.5 V	1, 2, 3	3.46		V
			OSC_DR = 2.75 V	All	5.5 V	1, 2, 3	4.46		
Low level output voltage (OUT) 3007	V _{OL1}	OE _H = V _{CC} , DIVA = V _{IL2} , OE _L = V _{IL1} , DIVB = V _{IL3} or V _{1/2} I _{OL} = 50 μA		All	4.5 V	1, 2, 3		0.1	V
				All	5.5 V	1, 2, 3		0.1	
		OE _H = V _{CC} , DIVA, DIVB = GND, OE _L = GND I _{OL} = 48 mA		All	4.5 V	1, 2, 3		0.44	
				All	5.5 V	1, 2, 3		0.44	
Low level output voltage, low drive (OSC_OUT) 3007	V _{OL2}	OSC_IN = V _{CC} OSC_DR = 0.0 V I _{OL} = 150 μA		All	4.5 V	1, 2, 3		0.74	V
				All	5.5 V	1, 2, 3		0.74	
Low level output voltage, medium drive (OSC_OUT) 3007	V _{OL3}	OSC_IN, OSC_DR = V _{CC} I _{OL} = 600 μA		All	4.5 V	1, 2, 3		0.74	V
				All	5.5 V	1, 2, 3		0.74	
Low level output voltage, high drive (OSC_OUT) 3007	V _{OL4}	OSC_IN = V _{CC} I _{OL} = 1.0 mA	OSC_DR = 2.25 V	All	4.5 V	1, 2, 3		0.74	V
			OSC_DR = 2.75 V	All	5.5 V	1, 2, 3		0.74	
Positive input clamp voltage 3022	V _{IC+}	For input under test, I _{IN} = 9.0 mA		All	4.5 V	1, 2, 3		5.7	V
Negative input clamp voltage 3022	V _{IC-}	For input under test, I _{IN} = -9.0 mA		All	4.5 V	1, 2, 3		-1.2	V
Input current high (DIVA, DIVB, OSC_DR) 3010	I _{IH}	V _{IN} = 5.5 V		All	5.5 V	1, 2, 3	200	380	μA

See footnotes at end of table.

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Table I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified		Device type and Device class	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
							Min	Max	
Input current low (DIVB, OSC_DR) 3009	I _{IL}	V _{IN} = 0.0 V		All All	5.5 V	1, 2, 3	-200	-380	μA
Input current high (OEL) 3010	I _{IH}	V _{IN} = 5.5 V		All All	5.5 V	1, 2, 3	85	175	μA
Input current low (DIVA, OEL) 3009	I _{IL}	V _{IN} = 0.0 V		All All	5.5 V	1, 2, 3		-6.0	μA
Input current high (OEH) 3010	I _{IH}	V _{IN} = 5.5 V		All All	5.5 V	1, 2, 3		6.0	μA
Input current low (OEH) 3009	I _{IL}	V _{IN} = 0.0 V		All All	5.5 V	1, 2, 3	-85	-175	μA
Input current high (OSC_IN) 3010	I _{IH}	V _{IN} = 5.5 V		All All	5.5 V	1, 2, 3	20	125	μA
Input current low (OSC_IN) 3009	I _{IL}	V _{IN} = 0.0 V		All All	5.5 V	1, 2, 3	-20	-125	μA
Quiescent supply current, output low 3005	I _{CCL}	OEH = 5.5 V OEL = 0.0 V For all other inputs, V _{IN} = V _{CC} or GND		All All	5.5 V	1, 2, 3		240	μA
Quiescent supply current, output high 3005	I _{CCH}	OEH = 5.5 V OEL = 0.0 V For all other inputs, V _{IN} = V _{CC} or GND		All All	5.5 V	1, 2, 3		45.0	μA
Quiescent supply current, output three-state 3005	I _{CCZ}	OEH = 0.0 V OEL = 5.5 V For all other inputs, V _{IN} = V _{CC} or GND		All All	5.5 V	1, 2, 3		45.0	μA
Quiescent supply current delta, OSC_IN open 3005	ΔI _{CCO}	OSC_IN = Open For all other inputs, V _{IN} = V _{CC} or GND	OSC_DR = 0.45 V	All All	4.5 V	1, 2, 3	0.6		mA
			OSC_DR = 0.55 V	All All	5.5 V	1, 2, 3		6.5	
		OSC_IN = Open For all other inputs, V _{IN} = V _{CC} or GND	OSC_DR = 4.05 V	All All	4.5 V	1, 2, 3	1.7		
			OSC_DR = 4.95 V	All All	5.5 V	1, 2, 3		12.4	
		OSC_IN = Open For all other inputs, V _{IN} = V _{CC} or GND	OSC_DR = 1.8 V, 2.7 V	All All	4.5 V	1, 2, 3	5.5		
			OSC_DR = 2.2 V, 3.3 V	All All	5.5 V	1, 2, 3		31.5	

See footnotes at end of table.

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Table I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and Device class	V _{CC}	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Quiescent supply current delta, input 3 level 3005	ΔI _{CC3L}	DIVB, OSC_DR = 2.75 V For all other inputs, V _{IN} = V _{CC} or GND	All All	5.5 V	1, 2, 3		1.5	mA
Quiescent supply current delta, TTL input level 3005	ΔI _{CCT} <u>6/</u>	<u>OE</u> L, <u>OE</u> H = V _{CC} - 2.1 V For all other inputs, V _{IN} = V _{CC} or GND	All All	5.5 V	1, 2, 3		1.5	mA
Three-state output leakage current high 3021	I _{OZH} <u>7/</u>	V _{OUT} = V _{CC} <u>OE</u> H = 0.8 V, <u>OE</u> L = 2.0 V For all other inputs, V _{IN} = V _{CC} or GND	All All	4.5 V	1, 2, 3		5.0	μA
			All All	5.5 V	1, 2, 3		5.0	
Three-state output leakage current low 3020	I _{OZL} <u>7/</u>	V _{OUT} = 0.0 V <u>OE</u> H = 0.8 V, <u>OE</u> L = 2.0 V For all other inputs, V _{IN} = V _{CC} or GND	All All	4.5 V	1, 2, 3		-150.0	μA
			All All	5.5 V	1, 2, 3		-180.0	
Functional tests 3014	<u>8/</u>	See 4.4.1b Verify output V _{OUT}	All All	4.5 V	7, 8	L	H	
			All All	5.5 V	7, 8	L	H	
Output enable time, OEL or OEH to OUT 3003	t _{PZH} <u>10/</u>	C _L = 50 pF, R _L = 500Ω See figure 4	All All	4.5 V	9, 10, 11	1.0	31.5	ns
	t _{PZL} <u>10/</u>	C _L = 50 pF, R _L = 500Ω See figure 4	All All	4.5 V	9, 10, 11	1.0	28.0	
Output disable time, OEL or OEH to OUT 3003	t _{PHZ} <u>10/</u>	C _L = 50 pF, R _L = 500Ω See figure 4	All All	4.5 V	9, 10, 11	1.0	21.5	ns
	t _{PLZ} <u>10/</u>	C _L = 50 pF, R _L = 500Ω See figure 4	All All	4.5 V	9, 10, 11	1.0	16.0	

- 1/ For tests not listed in the referenced MIL-STD-883, (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein.
- 2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{CC} and ΔI_{CC} tests, where the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.
- 3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I, as applicable, at 4.5 V ≤ V_{CC} ≤ 5.5 V.
- 4/ The V_{IH} and V_{IL} tests are not required if applied as forcing functions for V_{OH} and V_{OL} tests.
- 5/ Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum.

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Table I. Electrical performance characteristics - Continued.

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- 6/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1 \text{ V}$ (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed.
- 7/ Three-state output conditions are required.
- 8/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. The input voltage levels have the allowable tolerances in accordance with MIL-STD-883 already incorporated.
- 9/ AC limits at $V_{CC} = 5.5 \text{ V}$ are equal to the limits at $V_{CC} = 4.5 \text{ V}$ and guaranteed by testing at $V_{CC} = 4.5 \text{ V}$. Minimum ac limits for $V_{CC} = 5.5 \text{ V}$ are 1.0 ns and guaranteed by guardbanding the $V_{CC} = 4.5 \text{ V}$ minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

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Device type	01
Case outlines	F
Terminal number	Terminal symbol
1	NC
2	OSC_OUT
3	NC
4	NC
5	OEL
6	OEH
7	OSCLO_1
8	GND
9	OUT
10	VCC
11	NC
12	DIVA
13	OSC_DR
14	DIVB
15	OSCLO_2
16	OSC_IN

NC = no connection

Terminal descriptions	
Terminal symbol	Description
OSC_IN	Input to Oscillator Inverter. The output of the crystal would be connected here.
OSC_OUT	Resistive Buffered Output of the Oscillator Inverter.
OSC_DR	3 Level input pin that selects Oscillator Drive Level.
DIVA	Input used to select Binary Divide-By Option. This pin has CMOS compatible input levels.
DIVB	3 Level input used to select Binary Divide-By value.
OEH	Active High Three-state enable pin. This pin pulls to a high value when left floating and three-states the output when forced low. This pin has TTL compatible input levels.
OEL	Active Low Three-state enable pin. This pin pulls to a low value when left floating and three-states the output when forced high. This pin has TTL compatible input levels.
OUT	This pin is the main clock output on the device.
OSCLO_1	The Oscillator Low pin is the ground for the Oscillator.
OSCLO_2	This pin is the same signal as OSCLO_1.
VCC	The power pin for the chip.
GND	The ground pin for all sections of the circuitry except the oscillator and oscillator related circuitry.

FIGURE 1. Terminal connections.

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Division Selection

DIVB	DIVA	$\overline{\text{OEL}}$	OEH	Divider Output
$V_{1/2}$	0 or Open	X	X	Divide-by 1
1	0 or Open	0	1	Divide-by 2
0	0 or Open	0	1	Divide-by 4
$V_{1/2}$	1	0	1	Divide-by 8
1	1	0	1	Divide-by 16
0	1	0	1	Divide-by 32
X	X	1	X	Output Reset High at Re-enable
X	X	X	0	Output Reset High at Re-enable

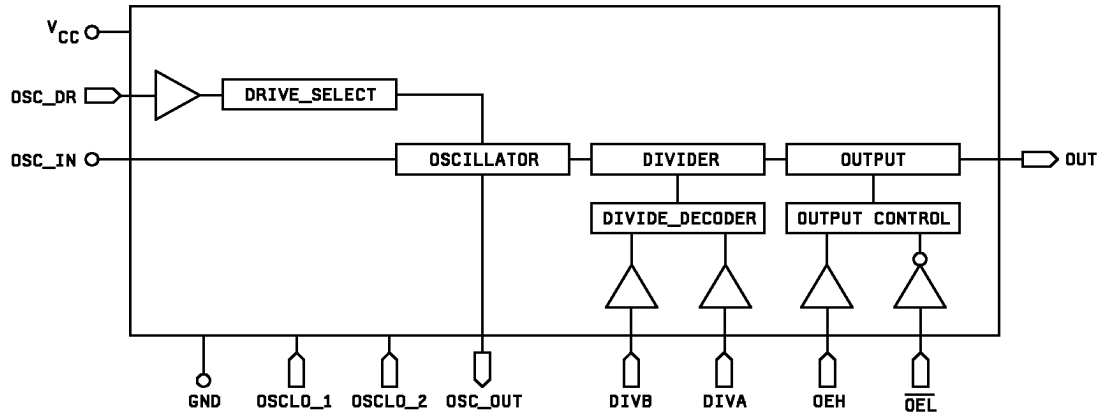
Drive Selection

OSC_DR	OSC_OUT drive
0	Low
1	Medium
$V_{1/2}$	High

1 = High voltage level
 0 = Low voltage level
 X = Irrelevant
 $V_{1/2} = V_{CC} / 2$

FIGURE 2. Truth tables.

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INPUT DRIVERS

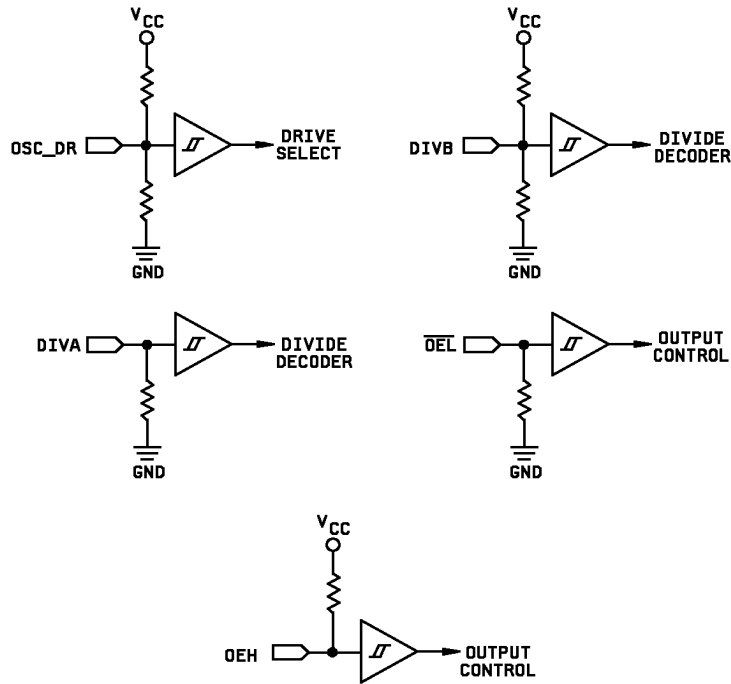


FIGURE 3. Logic diagram.

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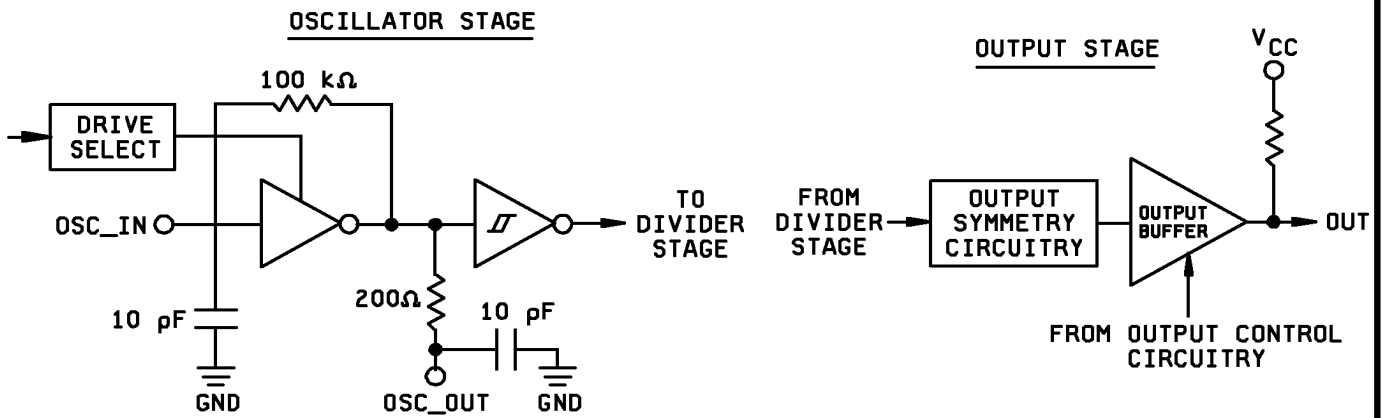
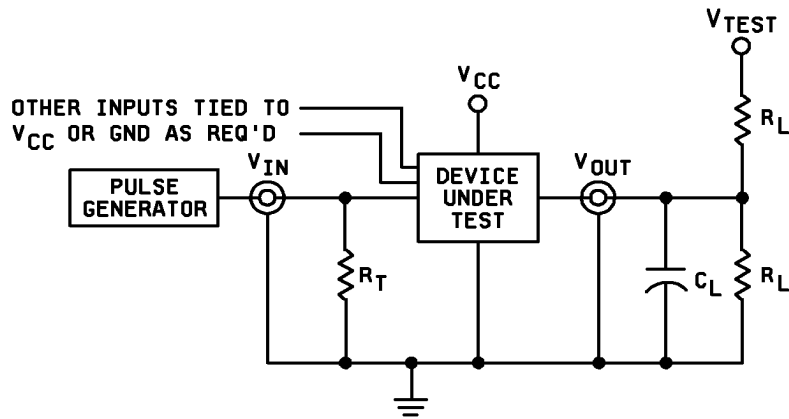
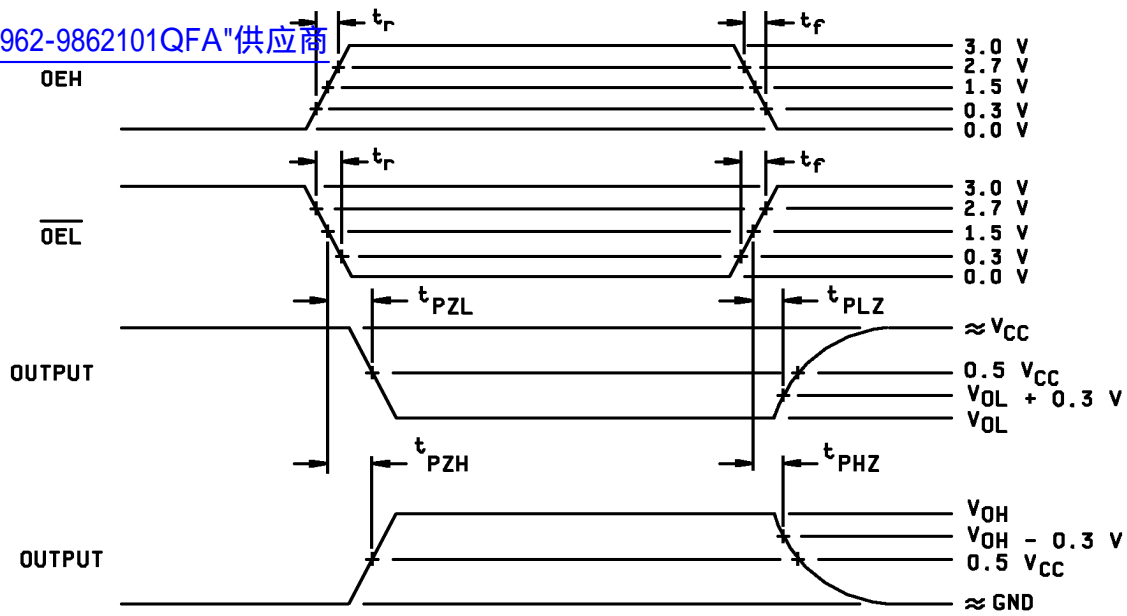


FIGURE 3. Logic diagram – Continued.

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NOTES:

1. When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = 2 \times V_{CC}$.
2. When measuring t_{PHZ} , t_{PZH} , t_{PLH} and t_{PHL} : $V_{TEST} = \text{open}$.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. $C_L = 50 \text{ pF}$ minimum or equivalent (includes test jig and probe capacitance).
5. $R_L = 500\Omega$ or equivalent.
6. $R_T = 50\Omega$ or equivalent.
7. Input signal from pulse generator: $V_{IN} = 0.0 \text{ V}$ to 3.0 V ; $PRR \leq 10 \text{ MHz}$; $t_r \leq 3.0 \text{ ns}$; $t_f \leq 3.0 \text{ ns}$; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V , respectively; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.

FIGURE 4. Switching waveforms and test circuit.

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4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>1/</u> 1, 2, 3, 7, 8, 9, 10, 11	<u>2/</u> 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7,8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

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4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

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6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application is used for QML-38535 and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

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DATE: 98-12-21

Approved sources of supply for SMD 5962-98621 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9862101QFA	27014	54ACT3301W-QML

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

27014

Vendor name and address

National Semiconductor
 2900 Semiconductor Drive
 P.O. Box 58090
 Santa Clara, CA 95052-8090
 Point of contact: 5 Foden Road
 South Portland, ME 04106

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