REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17																

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
99-10-14

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, MEMORY, DIGITAL, FLASH EPROM, 2M X 8-BIT, MONOLITHIC SILICON

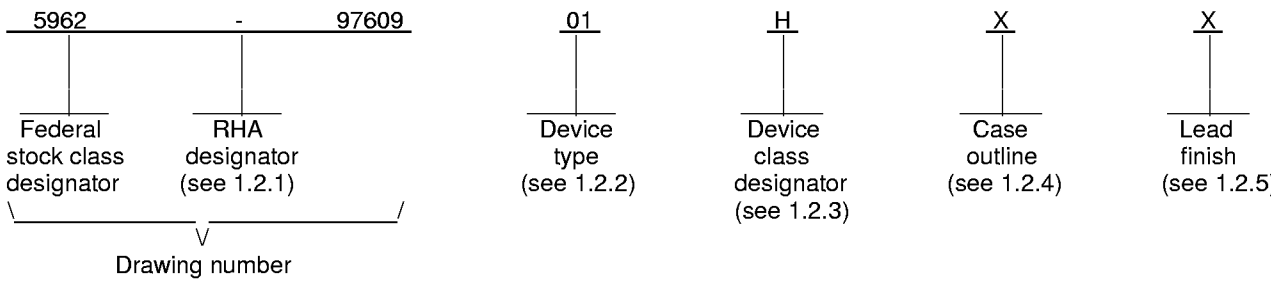
SIZE	CAGE CODE	
A	**67268**	**5962-97609**

SHEET 1 OF 17

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowest high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	WMF2M8-150	FLASH EPROM, 2M X 8-bit	150 ns
02	WMF2M8-120	FLASH EPROM, 2M X 8-bit	120 ns
03	WMF2M8-90	FLASH EPROM, 2M X 8-bit	90 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	56	Ceramic flatpack, lead formed

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) 2/	-2.0 V dc to +7.0 V dc
Signal voltage range (any pin except A9) 2/	-2.0 V dc to +7.0 V dc
Power dissipation (P_D)	0.33 W maximum at 5 MHz
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Data retention	10 years minimum
Endurance (write/erase cycles)	10,000 cycles minimum
RESET, OE, and A9 voltage for auto select and sector protect (V_{ID}):	
	-2.0 V dc to +12.5 V dc 3/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.0 V dc to V_{CC} + 0.5 V dc
Case operating temperature range (T_C)	-55 °C to +125 °C
RESET, OE, and A9 voltage for auto select and sector protect (V_{ID}):	
	+11.5 V dc to +12.5 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Minimum DC voltage in input or I/O pins is -0.5 V dc. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V dc for periods up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} +0.5 V dc. During voltage transitions, outputs may overshoot to V_{CC} +2.0 V dc for periods up to 20 ns.
3/ Minimum DC input voltage on $\overline{\text{RESET}}$, $\overline{\text{OE}}$, and A9 is -0.5 V dc. During voltage transitions, $\overline{\text{RESET}}$, $\overline{\text{OE}}$, and A9 may overshoot V_{SS} to -2.0 V dc for periods up to 20 ns. Maximum DC input voltage on A9 is +13.5 V dc which may overshoot to +14.0 V dc for periods up to 20 ns.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4, 5, and 6.

3.2.5 Block diagram. The block diagram shall be as specified on figure 7.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 8.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Programming procedure. The programming procedure shall be as specified by the manufacturer and shall be available upon request.

3.6 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.7 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.8 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.9 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for the initial characterization and after any design process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase cycles listed in section 1.3 herein over the full military temperature range. The vendors procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which any affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC parameters							
Input leakage current	I_{LI}	V_{CC} = 5.5 V dc, V_{IN} = GND to V_{CC}	1,2,3	All		10	µA
Output leakage current	I_{LO}	V_{CC} = 5.5 V dc, V_{IN} = GND to V_{CC}	1,2,3	All		10	µA
V_{CC} active current for read	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5 MHz, V_{CC} = 5.5 V dc	1,2,3	All		40	mA
V_{CC} active current for program or erase 3/	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{CC} = 5.5 V dc	1,2,3	All		60	mA
V_{CC} standby current	I_{CC3}	V_{CC} = 5.5 V dc, $\overline{CS}$ = V_{IH}, f = 5 MHz, RESET = V_{CC} ± 0.3 V	1,2,3	All		0.25	mA
Input low level 3/	V_{IL}		1,2,3	All	-0.5	0.8	V
Input high level 3/	V_{IH}		1,2,3	All	2.0	V_{CC} + 0.5 V	V
Output low voltage	V_{OL}	V_{CC} = 4.5 V dc, I_{OL} = 12.0 mA	1,2,3	All		0.45	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V dc, I_{OH} = -2.5 mA	1,2,3	All	0.85 x V_{CC}		V
Low V_{CC}, lockout voltage	V_{LKO}		1,2,3	All	3.2	4.2	V
Dynamic characteristics							
Address capacitance 3/	C_{AD}	V_{IN} = 0 V dc, f = 1.0 MHz, T_A = +25°C	4	All		12	pF
Output enable 3/ capacitance	C_{OE}	V_{IN} = 0 V dc, f = 1.0 MHz, T_A = +25°C	4	All		12	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic characteristics - Continued.							
Write enable 3/ capacitance	C_{WE}	V_{IN} = 0 V dc, f = 1.0 MHz, $T_A = +25°C$	4	All		12	pF
Chip select 3/ capacitance	C_{CS}	V_{IN} = 0 V dc, f = 1.0 MHz, $T_A = +25°C$	4	All		12	pF
Data I/O capacitance 3/	$C_{I/O}$	V_{IN} = 0 V dc, f = 1,0 MHz, $T_A = +25°C$	4	All		12	pF
Functional testing							
Functional tests		See 4.3.1c	7,8A,8B	All			
Read cycle AC timing characteristics							
Read cycle time 3/	t_{RC}	See figure 4	9,10,11	01 02 03	150 120 90		ns
Address access time	t_{ACC}	See figure 4	9,10,11	01 02 03		150 120 90	ns
Chip select access time	t_{CE}	See figure 4	9,10,11	01 02 03		150 120 90	ns
Output enable to output valid	t_{OE}	See figure 4	9,10,11	01 02 03		55 50 40	ns
Output hold from address, CS or OE change, whichever is first 3/	t_{OH}	See figure 4	9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write/Erase/Program AC timing characteristics $\overline{WE}$ controlled.							
Write cycle time 3/	t_{WC}	See figure 5	9,10,11	01 02 03	150 120 90		ns
Chip select setup time	t_{CS}	See figure 5	9,10,11	All	0		ns
Write enable pulse width	t_{WP}	See figure 5	9,10,11	01, 02 03	50 45		ns
Address setup time	t_{AS}	See figure 5	9,10,11	All	0		ns
Data setup time	t_{DS}	See figure 5	9,10,11	01, 02 03	50 45		ns
Data hold time	t_{DH}	See figure 5	9,10,11	All	0		ns
Address hold time	t_{AH}	See figure 5	9,10,11	01, 02 03	50 45		ns
Write enable pulse width high 3/	t_{WPH}	See figure 5	9,10,11	All	20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write/Erase/Program AC charateristics $\overline{CS}$ controlled.							
Write cycle time 3/	t_{WC}	See figure 6	9,10,11	01 02 03	150 120 90		ns
Write enable setup time	t_{WS}	See figure 6	9,10,11	All	0		ns
Chip select pulse width	t_{CP}	See figure 6	9,10,11	01, 02 03	50 45		ns
Address setup time	t_{AS}	See figure 6	9,10,11	All	0		ns
Data hold time	t_{DH}	See figure 6	9,10,11	All	0		ns
Data setup time	t_{DS}	See figure 6	9,10,11	01, 02 03	50 45		ns
Address hold time	t_{AH}	See figure 6	9,10,11	01, 02 03	50 45		ns
Chip select pulse width high 3/	t_{CPH}	See figure 6	9,10,11	All	20		ns

1/ Unless otherwise specified, 4.5 V dc $\le V_{CC} \le$ 5.5 V dc and V_{SS} = 0 V.
2/ Unless otherwise specified, the DC test conditions are as follows:
Input pulse levels: $V_{IH} = V_{CC}$ - 0.3 V and V_{IL} = 0.3 V.
Unless otherwise specified, the AC test conditions are as follows:
Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V.
Input rise and fall times: 5 nanoseconds.
Input and output timing reference levels: 1.5 V.
3/ Parameters shall be tested as part of device characterization and after design and process changes. Parameters shall be tested to the limits specified in table I for all lots not specifically tested.

Case outline X

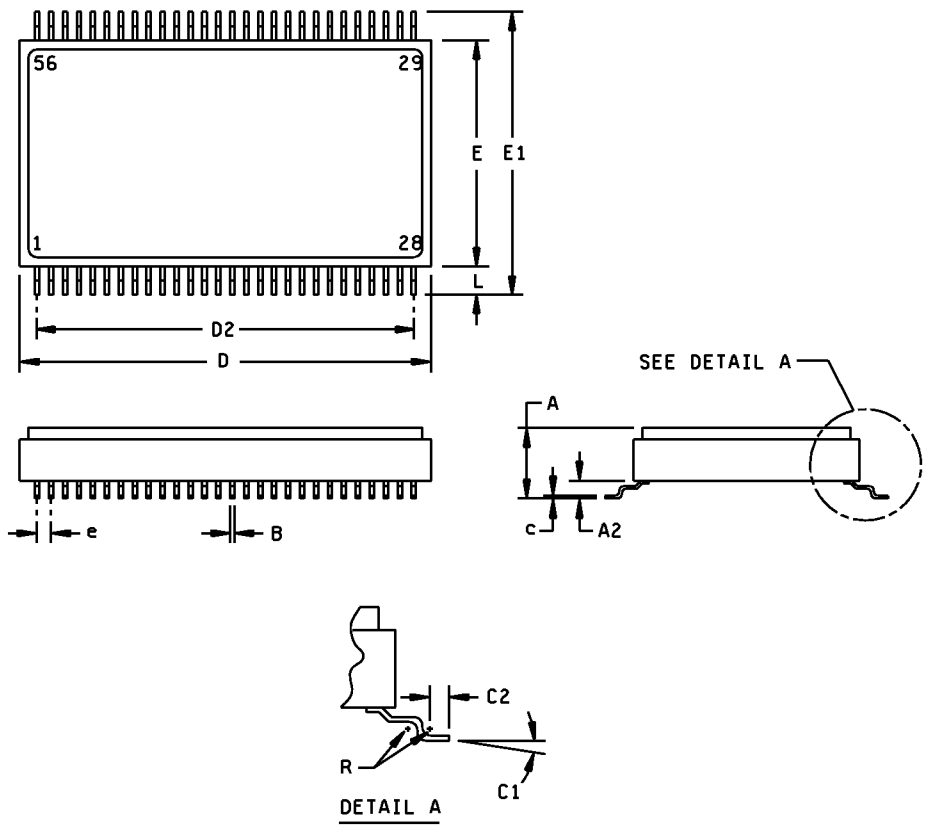


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-97609**
		REVISION LEVEL	SHEET **10**

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.06		.160
A2	0.38	0.64	.033	.047
B	0.20	0.30	.008	.012
c	0.13	0.23	.006	.010
C1	0°	-4°	0°	-4°
C2	0.51 TYP		.020 TYP	
D	23.37	23.88	.920	.940
D2	21.59 TYP		.850 TYP	
E	12.80	13.11	.504	.516
E1	16.00	16.26	.630	.640
e	0.80 TYP		.315 TYP	
L	1.58 TYP		.063 TYP	
R	0.18 TYP		.007 TYP	

NOTES:

1. The U.S preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outline(s) - Continued.

Device types	All	Device types	All	Device types	All	Device types	All
Case outline	X	Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{CS}$	17	NC	33	I/O2	49	A3
2	A12	18	I/O7	34	NC	50	A2
3	A13	19	NC	35	NC	51	A1
4	A14	20	RY/$\overline{BY}$	36	NC	52	A9
5	A15	21	$\overline{OE}$	37	A0	53	A10
6	NC	22	$\overline{WE}$	38	I/O0	54	A11
7	NC	23	NC	39	NC	55	$\overline{RESET}$
8	NC	24	NC	40	I/O1	56	NC
9	A20	25	I/O5	41	NC		
10	A19	26	NC	42	V_{CC}		
11	A18	27	I/O4	43	A8		
12	A17	28	V_{CC}	44	GND		
13	A16	29	GND	45	A7		
14	V_{CC}	30	NC	46	A6		
15	GND	31	I/O3	47	A5		
16	I/O6	32	NC	48	A4		

NOTE: NC is a no connection

FIGURE 2. Terminal connections.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	MODE
V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Read
V_{IL}	V_{IH}	V_{IL}	D_{IN}	Write
V_{IH}	X	X	High Z	Standby
V_{IL}	V_{IH}	V_{IH}	High Z	Output disable

NOTES:
1. V_{IH} = High logic level
2. V_{IL} = Low logic level
3. X = Do not care (either high or low)
4. High Z = High impedance state

FIGURE 3. Truth table.

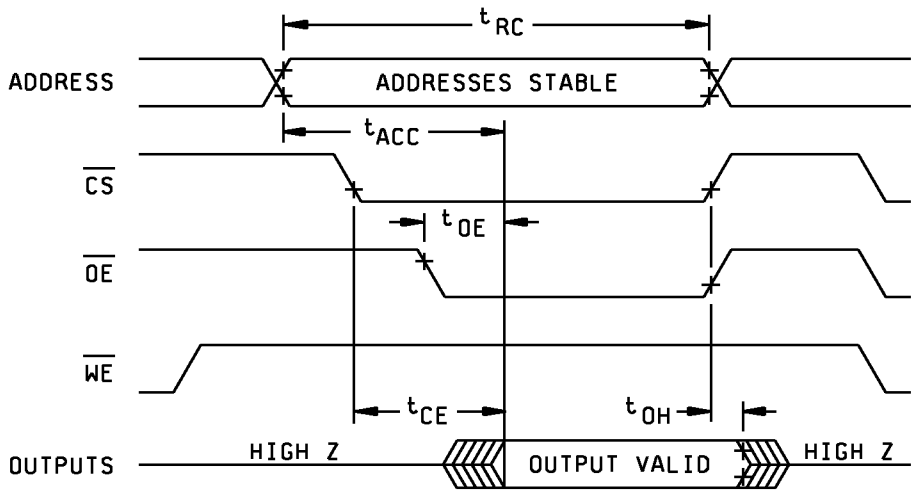


FIGURE 4. Read cycle timing diagram.

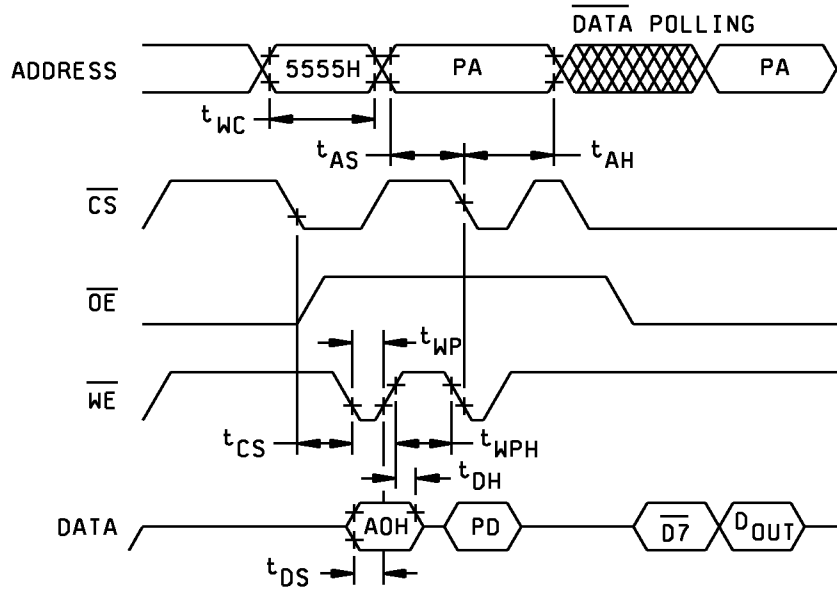


FIGURE 5. Write cycle timing diagram, $\overline{WE}$ controlled.

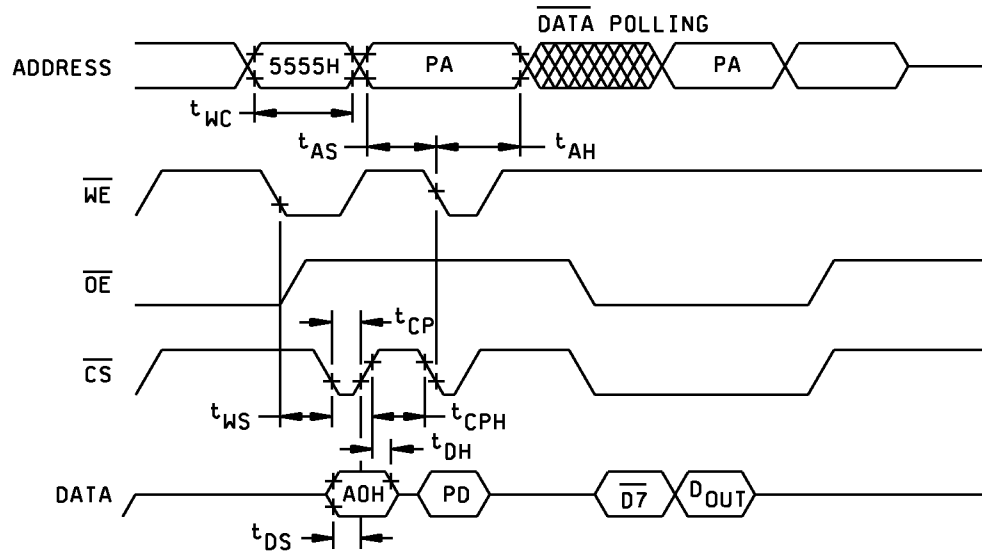


FIGURE 6. Write cycle timing diagram, $\overline{CS}$ controlled.

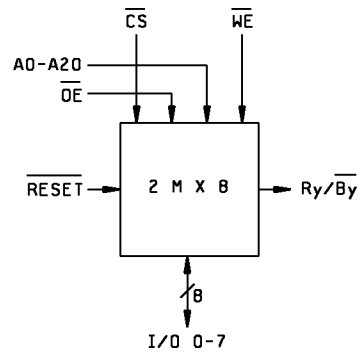
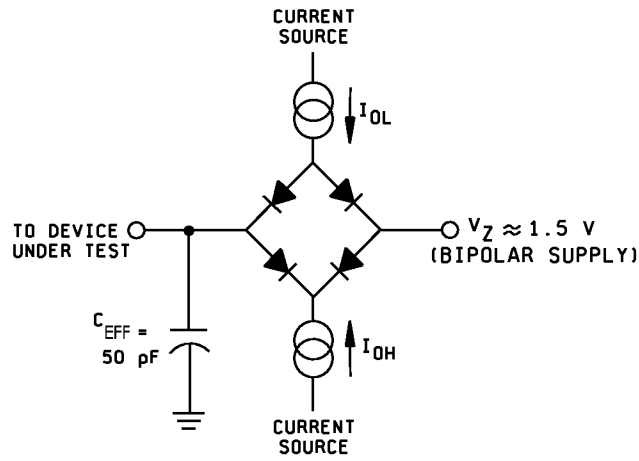


FIGURE 7. Block diagram.



Parameter	Typ.	Unit
Input pulse level	V_{IL} = 0 V, V_{IH} = 3.0 V	V
Input rise and fall	5	ns
Input and output reference level	1.5	V
Timing reference level	1.5	V

NOTES:
1. V_Z is programmable from +2 V to +7 V.
2. I_{OL} and I_{OH} are programmable from 0 to 16 mA.
3. Tester impedance is Z_0 = 75 ohms.
4. V_Z is typically the midpoint of V_{OH} and V_{OH}.
5. I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 8. Output load circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical parameters	1*,2,3,4,7,8A,8B,9,10,11
Group A test requirements	1,2,3,4,7,8A,8B,9,10,11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10,11
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table on figure 3.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance withMIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-10-14

Approved sources of supply for SMD 5962-97609 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9760901HXA 5962-9760901HXC	54230 54230	WMF2M8-150DAQ5 WMF2M8-150DAQ5
5962-9760902HXA 5962-9760902HXC	54230 54230	WMF2M8-120DAQ5 WMF2M8-120DAQ5
5962-9760903HXA 5962-9760903HXC	54230 54230	WMF2M8-90DAQ5 WMF2M8-90DAQ5

1/ The lead finish shown for each PIN representing a hermetic package is available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
54230	White Electronic Designs Corporation 3601 East University Drive. Phoenix, AZ 85034