DM634

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16-CHANNEL CONSTANT CURRENT LED DRIVER WITH PROGRAMMABLE PWM OUTPUTS

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DM634

16-CHANNEL CONSTANT CURRENT LED DRIVER WITH PROGRAMMABLE PWM OUTPUTS

General Description

DM634 is a 16-channel constant current sink LED driver. Each channel has adjustable 16-bits (65536 steps) grayscale PWM control current outputs. 7-bit global brightness control is included in supporting user to adjust chip current easily. It incorporates shift registers, data latches, constant current circuitry with current value set by an external resistor, selectable oscillator source for PWM functioning, and built-in LED open/short detection circuit to detect error status. It supports thermal alarm and shutdown function; system retrieve the message to indicate when junction temperature over limitation of chip. It is specifically designed for LED display and lighting applications.

Features

- Constant-current outputs: 5mA to 90mA
- 16-bit linear PWM control current output per channel
- 7-bit high accuracy global brightness control
- Maximum output voltage: 17V
- Maximum clock frequency: 25MHz
- Selectable internal/external PWM reference clock
- PWM free-running capability (refresh rate ~ 275 Hz with internal oscillator ~ 18 MHz)
- Build-in real-time LED open/short detection
- Thermal Alarm and Shotdown –
  Alarm : Junction Temperature >110℃
  Shutdown : Junction Temperature > 180℃
- Package and pin assignment (except QFN32) compatible to conventional LED driver series (ST2221C, DM134B/5B, DM13C)
- Power supply voltage: 3.3V to 5.5 V

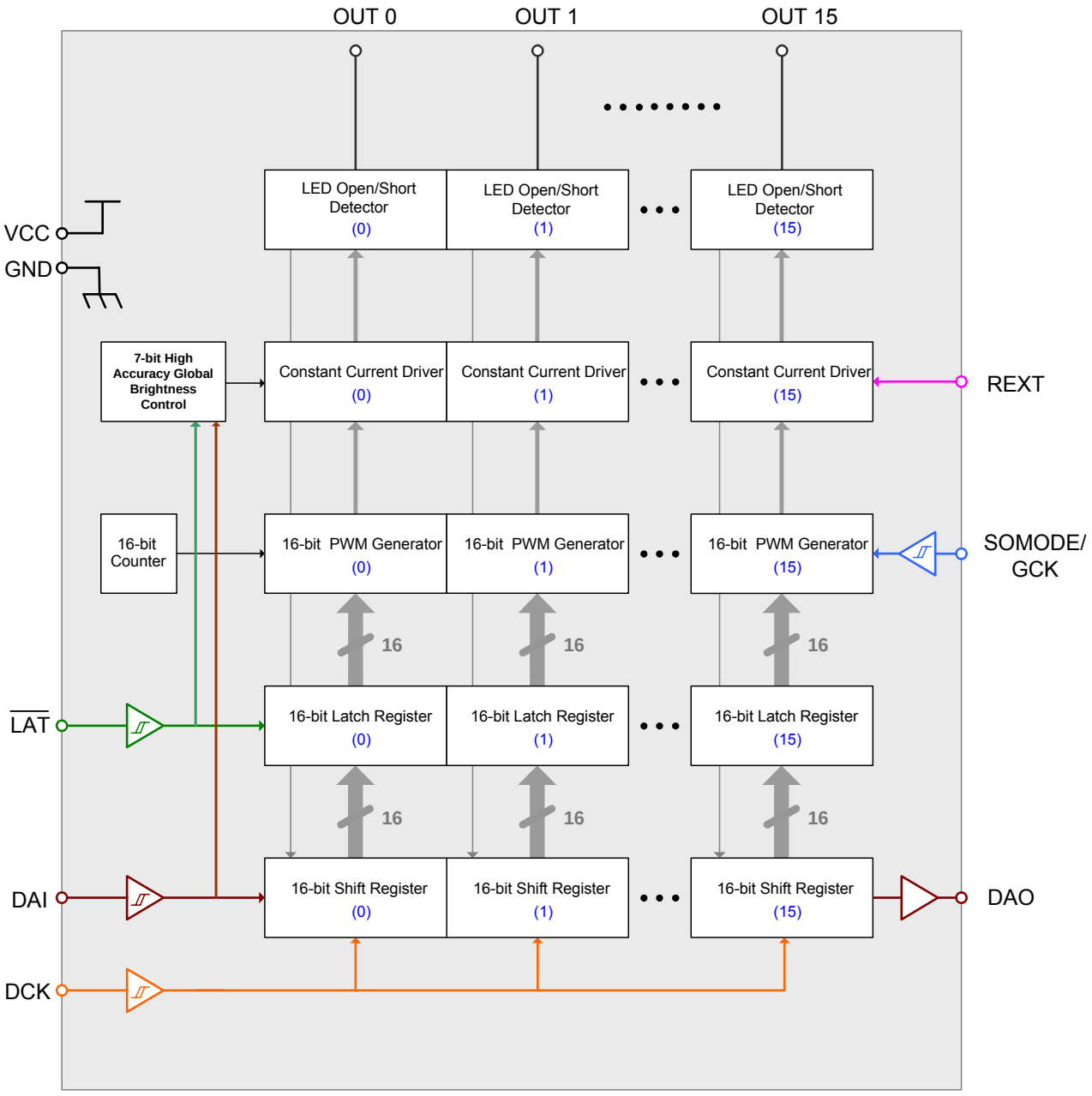
Applications

- Indoor/Outdoor LED Video Display
- LED Variable Message Signs (VMS) System
- LED Decorative Lighting

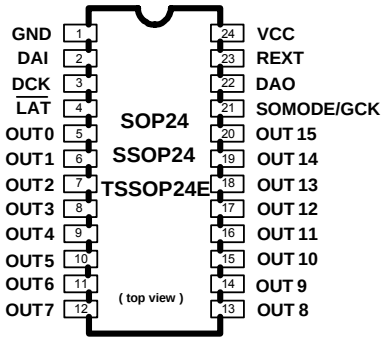
Package Types

- SOP24, SSOP24, TSSOP24E (with exposed pad)

Block Diagram



Pin Connection

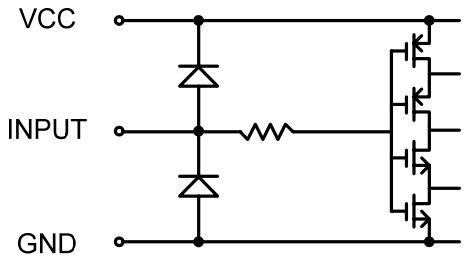


Pin Description

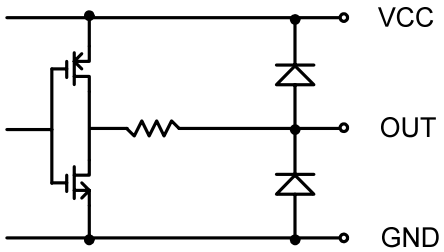
PIN No.	PIN NAME	FUNCTION
SOP24/SSOP24/TSSOP24E: 1 TSSOP24E: exposed pad	GND	Ground terminal.
SOP24/SSOP24/TSSOP24E: 2	DAI	Serial data input terminal.
SOP24/SSOP24/TSSOP24E: 3	DCK	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.
SOP24/SSOP24/TSSOP24E: 4	$\overline{\text{LAT}}$	Input terminal of data strobe: **'H'** means data on shift register goes through latch (level trigger), **'L'** means data is latched.
SOP24/SSOP24/TSSOP24E: 5~20	OUT0~15	Sink constant-current outputs (open-drain).
SOP24/SSOP24/TSSOP24E: 21	SOMODE /GCK	Serial Out Mode Selection(SOMODE) : **'H'**: DAO is shifted out and synchronized to falling edge of DCK, **'L'** : DAO is shifted out and synchronized to rising edge of DCK. Gray Scale Clock(GCK) : Input terminal for PWM operation.
SOP24/SSOP24/TSSOP24E: 22	DAO	Serial data output terminal.
SOP24/SSOP24/TSSOP24E: 23	REXT	External resistors connected between REXT and GND for output current value setting.
SOP24/SSOP24/TSSOP24E: 24	VCC	Supply voltage terminal.

Equivalent Circuit of Inputs and Outputs

1. DCK, DAI, $\overline{LAT}$, SOMODE/GCK terminals



2. DAO terminals



PCB Layout Consideration

To connect an external resistor to REXT pin and ground can determine the maximum output current. If there is any disturbance occurred to REXT pin, the constant current output may be unstable or noisy. Since REXT (pin23), DAO (pin22), and SOMODE/GCK (pin21) are next to each other, the most possible interference is caused by DAO or SOMODE/GCK signal. Accordingly, it is recommended that adding some shielding area within the above pins in PCB layout, or laying the signal line of above pins on different PCB layer will prevent the noise problems effectively.

Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VCC	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VCC+0.3	V
Output Current	IOUT	100	mA
Output Voltage	VOUT	-0.3 ~ 17	V
Input Clock Frequency	FDCK	25	MHz
GND Terminal Current	IGND	1600	mA
Power Dissipation (4 layer PCB, Ta=25°C)	PD	4.31(TSSOP24E exposed pad)	W
		2.5(SOP24)	
		1.81(SSOP24)	
Thermal Resistance (4 layer PCB, Ta=25°C)	Rth(j-a)	29 (TSSOP24E exposed pad)	°C/W
		50 (SOP24)	
		69 (SSOP24)	
Operating Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VCC	—	3.3	5.0	5.5	V
Output Voltage	VOUT	Driver On *1	1.0	—	0.5VCC	V
Output Voltage	VOUT	Driver Off *2	—	—	17	
Output Current	IO	OUTn	5	—	90	mA
	IOH	VOH = VCC – 0.4 V	-0.8	—	-2	
	IOL	VOL = 0.2 V	+0.8	—	+2	
Input Voltage	VIH	VCC = 3.3 V ~ 5.5V	0.8VCC	—	VCC	V
	VIL		0.0	—	0.2VCC	
Input Clock Frequency	FDCK	Single Chip Operation	—	—	25	MHz
Input PWM Frequency	FGCK	VCC= 3.3V ~ 5.5V	—	—	25	
Pulse Width	tw $\overline{LAT}$	VCC = 5.0V	15	—	—	ns
DCK Pulse Width	tw DCK		15	—	—	
Set-up Time for DAI	tsetup(D)		10	—	—	
Hold Time for DAI	thold(D)		10	—	—	
Set-up Time for $\overline{LAT}$	tsetup(L)		10	—	—	
Hold Time for $\overline{LAT}$	thold(L)		10	—	—	
Internal Oscillator Frequency	FOSC		14.4	18	22	MHz

*1 Notice that the power dissipation is limited to its package and ambient temperature.
*2 The driver output voltage including any overshoot stress has to be compliant with the maximum voltage (17V).

Electrical Characteristics (VCC = 5.0 V, Ta = 25°C, GBC = 95 unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leakage Current	IOL	VOH = 17 V	—	—	±1.0	uA
Output Voltage (S-OUT)	VOL	IOL = 1.5 mA	—	—	0.4	V
	VOH	IOH= -1.3mA	4.5	—	—	
Output Current Skew (Channel-to-Channel) *1	IOL1	VOUT = 1.0 V Rrext = 2.2 KΩ	—	—	±3	%
Output Current Skew (Chip-to-Chip) *2	IOL2		18.275	—	20.607	mA
Output Voltage Regulation	% / VOUT	Rrext = 2.2 KΩ VOUT = 1 V ~ 3 V	—	±0.1	±0.5	% / V
Supply Voltage Regulation	% / VCC	Rrext = 2.2 KΩ	—	±1	±4	
Supply Current *3	$I_{DD(off)}$	power on all pins are open unless VCC and GND (free-running mode)	—	5.41	6.5	mA
	$I_{DD(off)}$	power on all pins are open unless VCC and GND (external GCK mode)	—	4.61	—	mA
	$I_{DD(off)}$	input signal is static Rrext = 12.4 KΩ all outputs turn off	—	5.97	—	
	$I_{DD(off)}$	input signal is static Rrext = 2.2 KΩ all outputs turn off	—	8.27	—	
	$I_{DD(off)}$	input signal is static Rrext = 570 Ω all outputs turn off	—	17.61	—	

*1 Channel-to-channel skew is defined as the ratio between (any Iout – average Iout) and average Iout, where average Iout = (Imax + Imin) / 2.
*2 Chip-to-Chip skew is defined as the range into which any output current of any IC falls.
*3 IO excluded.

Electrical Characteristics (VCC = 3.3 V, Ta = 25°C, GBC = 95 unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leakage Current	IOL	VOH = 17 V	—	—	±1.0	uA
Output Voltage (S-OUT)	VOL	IOL = 1.5 mA	—	—	0.4	V
	VOH	IOH= -1.3 mA	2.8	—	—	
Output Current Skew (Channel-to-Channel) *1	IOL1	VOUT = 1.0 V Rrext = 2.2 KΩ	—	—	±3	%
Output Current Skew (Chip-to-Chip) *2	IOL2		18.275	—	20.607	mA
Output Voltage Regulation	% / VOUT	Rrext = 2.2 KΩ VOUT = 1 V ~ 3 V	—	±0.1	±0.5	% / V
Supply Voltage Regulation	% / VCC	Rrext = 2.2 KΩ	—	±1	±4	
Supply Current *3	$I_{DD(off)}$	power on all pins are open unless VCC and GND (free-running mode)	—	4.19	—	mA
	$I_{DD(off)}$	power on all pins are open unless VCC and GND (external GCK mode)	—	3.79	—	
	$I_{DD(off)}$	input signal is static Rrext = 12.4 KΩ all outputs turn off	—	4.75	—	
	$I_{DD(off)}$	input signal is static Rrext = 2.2 KΩ all outputs turn off	—	7.04	—	
	$I_{DD(off)}$	input signal is static Rrext = 570 Ω all outputs turn off	—	16.014	—	

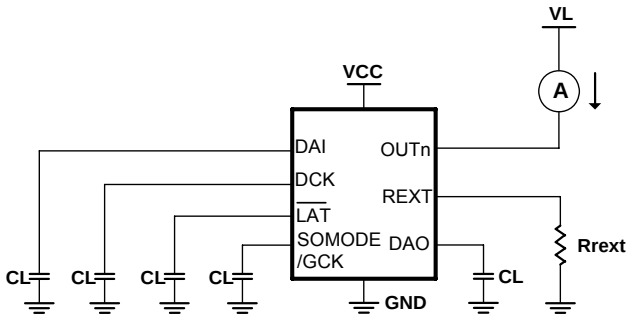
*1 Channel-to-channel skew is defined as the ratio between (any Iout – average Iout) and average Iout, where average Iout = (Imax + Imin) / 2.
*2 Chip-to-Chip skew is defined as the range into which any output current of any IC falls.
*3 IO excluded.

Switching Characteristics (VCC = 5.0V, Ta = 25°C, GBC = 95 unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L' to 'H')	GCK-to-OUT	tpLH	VIH = VCC VIL = GND Rrext = 2.2 KΩ VL = 5.0 V CL = 13 pF	—	47.5	—	ns
	DCK(rising)-to-DAO			—	25	—	
	DCK(falling)-to-DAO			—	14.4	—	
Propagation Delay ('H' to 'L')	GCK-to-OUT	tpHL		—	28.5	—	
	DCK(rising)-to-DAO			—	24	—	
	DCK(falling)-to-DAO			—	9.7	—	
Output Current Rise Time		tor		—	15	—	
Output Current Fall Time		tof		—	7.5	—	
Output to output Delay Time Unit		td		—	33	—	
Output Current (Propagation Delay after $\overline{LAT}$ trigger)		top*1		—	—	4.6	ms

Switching Characteristics (VCC = 3.3V, Ta = 25°C, GBC = 95 unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L' to 'H')	GCK-to-OUT	tpLH	VIH = VCC VIL = GND Rrext = 2.2 KΩ VL = 3.3 V CL = 13 pF	—	51.5	—	ns
	DCK(rising)-to-DAO			—	30.5	—	
	DCK(falling)-to-DAO			—	18.3	—	
Propagation Delay ('H' to 'L')	GCK-to-OUT	tpHL		—	31.5	—	
	DCK(rising)-to-DAO			—	29	—	
	DCK(falling)-to-DAO			—	14.4	—	
Output Current Rise Time		tor		—	20	—	
Output Current Fall Time		tof		—	10	—	
Output to output Delay Time Unit		td		—	34	—	
Output Current (Propagation Delay after $\overline{LAT}$ trigger)		top*1		—	—	4.6	ms



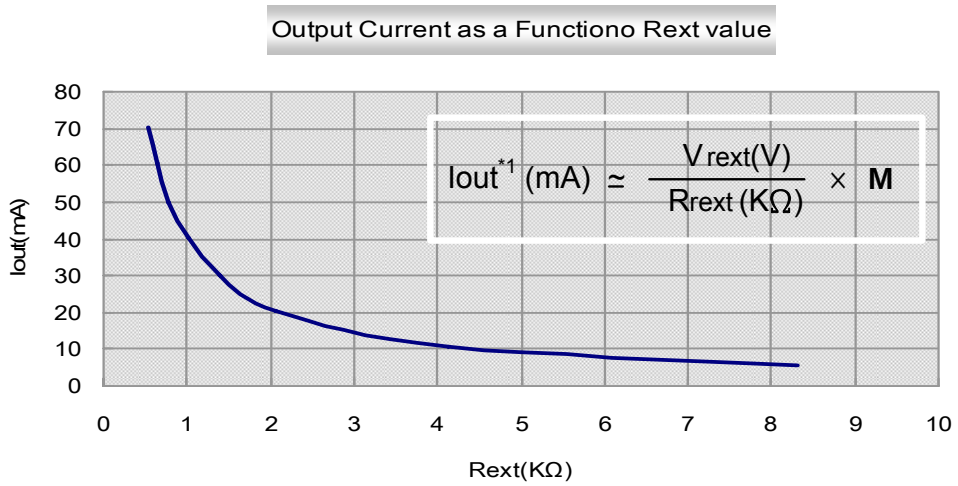
Switching Characteristics Test Circuit

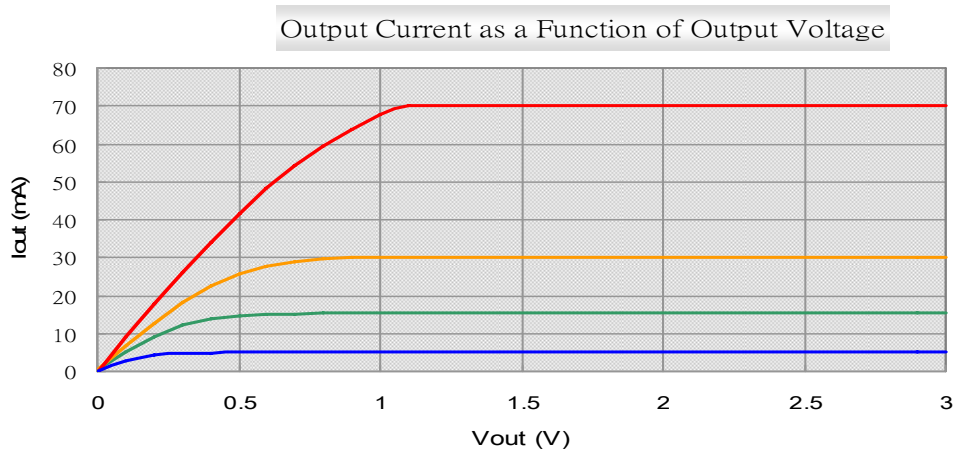
*1 Reload the new PWM data at the end of the last PWM frame.

Constant-Current Output

Constant-current value (Iout[*1]) of each output channel is set by an external resistor connected between the REXT pin and GND. The current scale ranging can be adjusted from 5mA to 70mA by varying the resistor value. User can input GBC value to increase Iout to 90mA. The reference voltage of REXT terminal (Vrext) is approximately 1.23V. The output current value is calculated by the following equation:

Iout(mA)	5	10	20	30	40	50	60	70
M	41.13	39.35	36.78	35.09	33.75	32.53	31.35	30.09





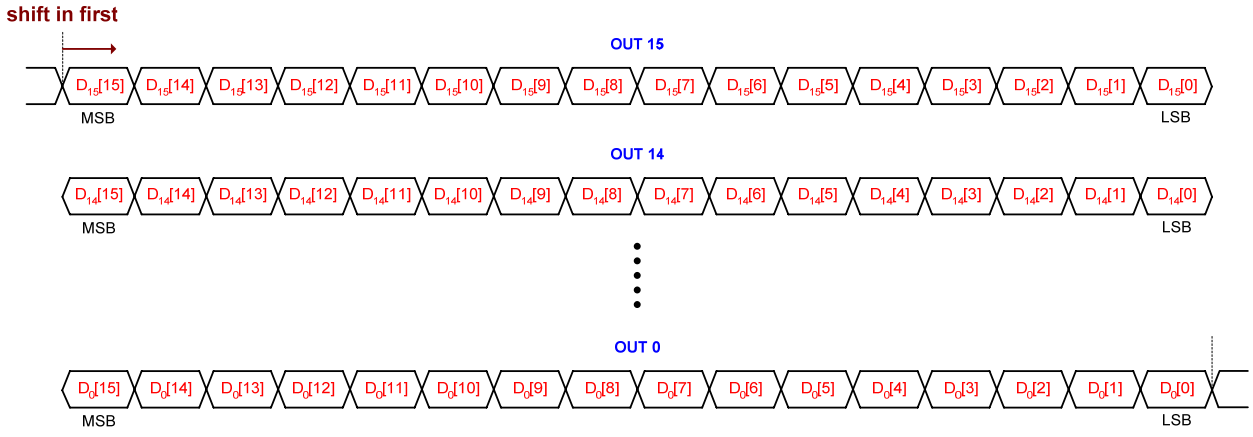
In order to obtain a good performance of constant-current output, a suitable output voltage is necessary. Users can get related information about the minimum output voltage above.

[*1] Iout is typical current value setting under 100% PWM duty cycle and 95 D_{GBC} Value.

Serial Data Interface

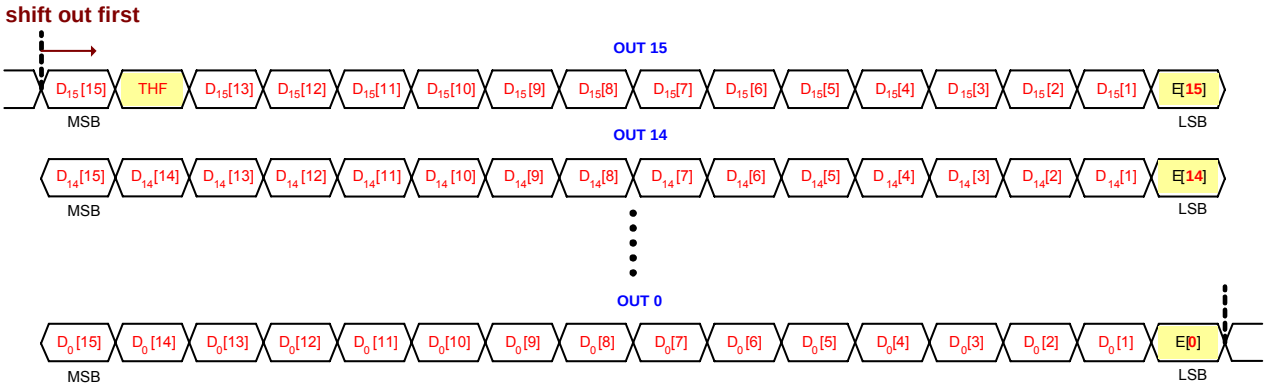
The serial-in data (DAI) will be clocked into 16 × 16 bit shift registers synchronized on the rising edge of the clock (DCK). The data will be transferred into the 16 × 16 bit latch registers when the strobe signal ($\overline{LAT}$) is kept at high level (level trigger); otherwise, the data will be held. The latch pulse should be sent after the falling edge of the last clock within a frame data. The trigger timing of the serial-out data (DAO) will be shifted out on synchronization to the rising edge of the clock if serial out selection (SOMODE) is kept at low level. And if serial out selection (SOMODE) is kept at high level, the serial-out data (DAO) will be shifted out on synchronization to the falling edge of the clock (DCK).

Input Data Format



$$\text{Active width per frame(\%)} = \frac{D[15]\times2^{15}+D[14]\times2^{14}+D[13]\times2^{13}+D[12]\times2^{12}+D[11]\times2^{11}+D[10]\times2^{10}+D[9]\times2^{9}+D[8]\times2^{8}+D[7]\times2^{7}+D[6]\times2^{6}+D[5]\times2^{5}+D[4]\times2^{4}+D[3]\times2^{3}+D[2]\times2^{2}+D[1]\times2^{1}+D[0]\times2^{0}}{65536}$$

Serial-out Data Format



＊E[**15**], E[**14**], ... E[**0**] are Error Messages of LED Open Detection. ‘1’ is normal, and ‘0’ is abnormal.

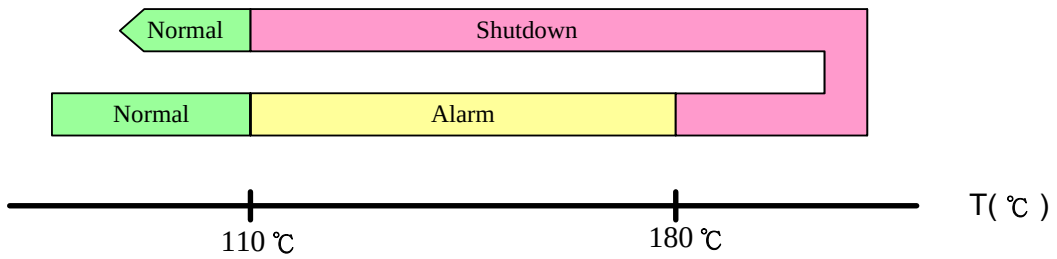
＊THF is the Error Message of chip thermal detection. ‘1’ is normal, and ‘0’ is abnormal.

LED Open/Short Detection

DM634 provides a real time monitor of LED open / short detection function without extra components or circuit design. When O/S flag[*1] set “L”, it will be identified as a LED open failure when the output is turned on but the output voltage is below 0.3V. The test result of each channel will write to its correspondent shift register which is in LSB position (D_{15}[0], D_{14}[0], …., D_0[0]) while strobe signal is active. User can refer to timing diagram on page12. Detecting report could be retrieved from serial-out (DAO) data. If the system reads ‘1’ back, that indicates LED is in normal status. But if ‘0’ was retrieved, it means LED open failure has occurred. In the short detection, O/S flag set “H”. And system reads result as ‘1’ means normal, ‘0’ means LED short failure occurred. The short detection threshold voltage is 65% of VCC. In order to make sure LED open/short detection function is in well operating condition, it is recommended that all the luminance data are wrote to ‘1’ then almost turning on the outputs during detection process.

Thermal Alarm and Shutdown

During operation, when the junction temperature of the chip reaches approximately above 180℃, driver will shutdown all the outputs. Basically, the chip will cool down and return to the safe operating temperature which is approximately below 110℃. DM634 will restart all the outputs at the same time. Operating upon 180℃ may cause chip to be damaged permanently.

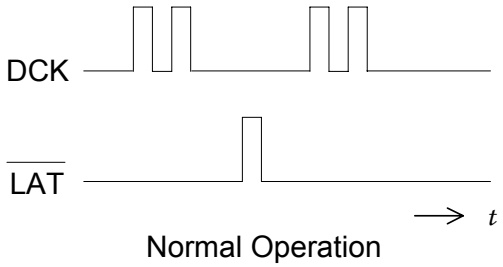


DM634 provides a real time monitor of chip thermal alarm and shutdown function. Except avoid the damage occurs when local junction temperature over the limitation, system can recognize which chip is under this situation. When O/S flag set “ 0”, it will be identified as the chip thermal over 110℃ as the THF flag retrieved ‘ 0’. The test result of each chip will write to its correspondent shift register which is in the position (D_{255}[0]) while strobe signal is active. User can refer to timing diagram on page14. Detecting report could be retrieved from serial-out (DAO) data. If the system reads ‘ 1’ back, that indicates chip is in normal status. But if ‘ 0’ was retrieved, it means the chip juction temperature is over 180℃ when O/S flag set to ‘ 1’ .

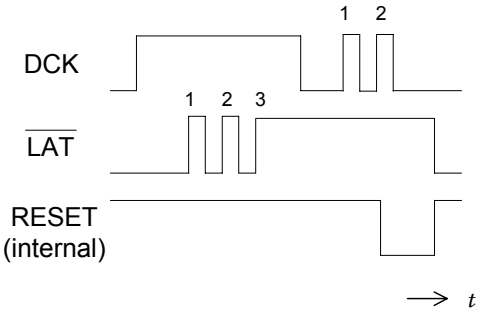
[*1] “L” is the default value of O/S flag. User can refer to Global Brightness Control to know how to set O/S flag on page 16.

Selection of Internal/External PWM Frequency

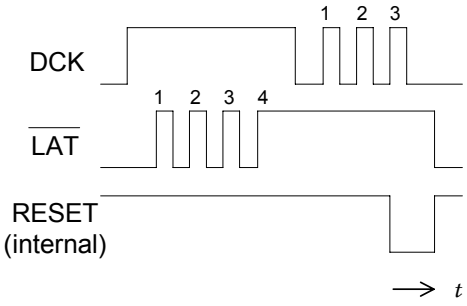
The default operation mode is the **free-running** PWM signal generated by internal oscillator after power-on. Users could switch internal to external PWM frequency source by following timing sequence. There are two alternative options could be selected. The option 1 shows three rising edges of latch pulse ($\overline{LAT}$) when the clock (DCK) kept at high level then two rising edges of clock (DCK) pulse when the latch pulse ($\overline{LAT}$) kept at high level. Then the SOMODE/GCK pin could input external frequency to operate PWM function. The option 2 shows four rising edges of latch pulse($\overline{LAT}$) when clock(DCK) kept at high level then sending three rising edges of clock (DCK) signal, while latch($\overline{LAT}$) signal kept high level at the same time. Meanwhile the GCK external mode can be set back to the free-running mode. Notice that when internal RESET at low level, all the shift registers in DM634 will be cleared (Kept at Low level) and all output current will be off immediately.



Normal Operation



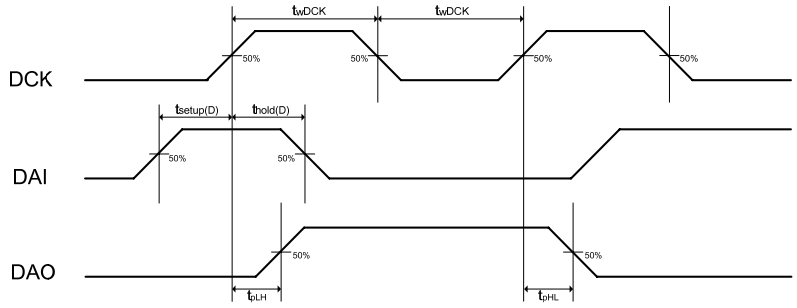
Option 1 : Timing Combination to set up external GCK mode



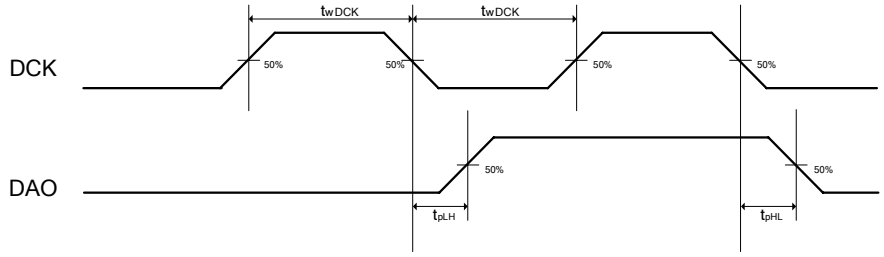
Option 2 : Timing Combination to set up free-running mode

Timing Diagram

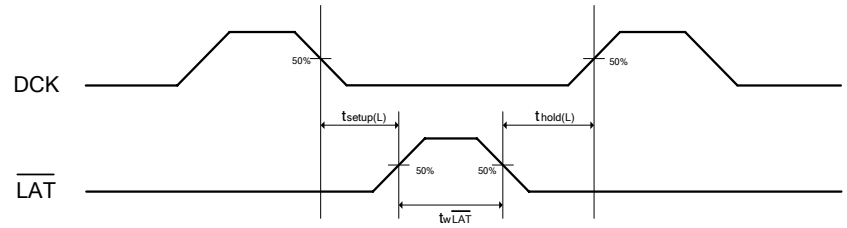
1. DCK(rising edge) - DAI, DAO (SOMODE = ”L” at free-running mode, or external GCK mode)



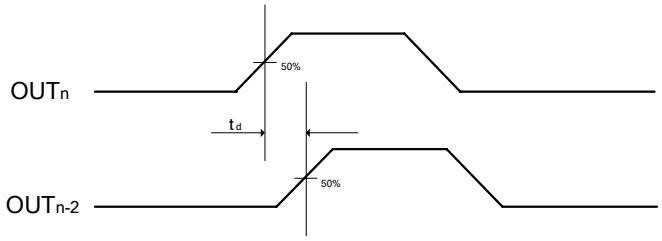
2. DCK(falling edge) - DAO (SOMODE = “H” at free-running mode)



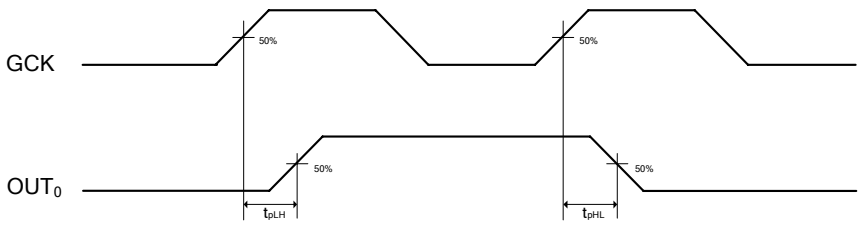
3. DCK-$\overline{LAT}$



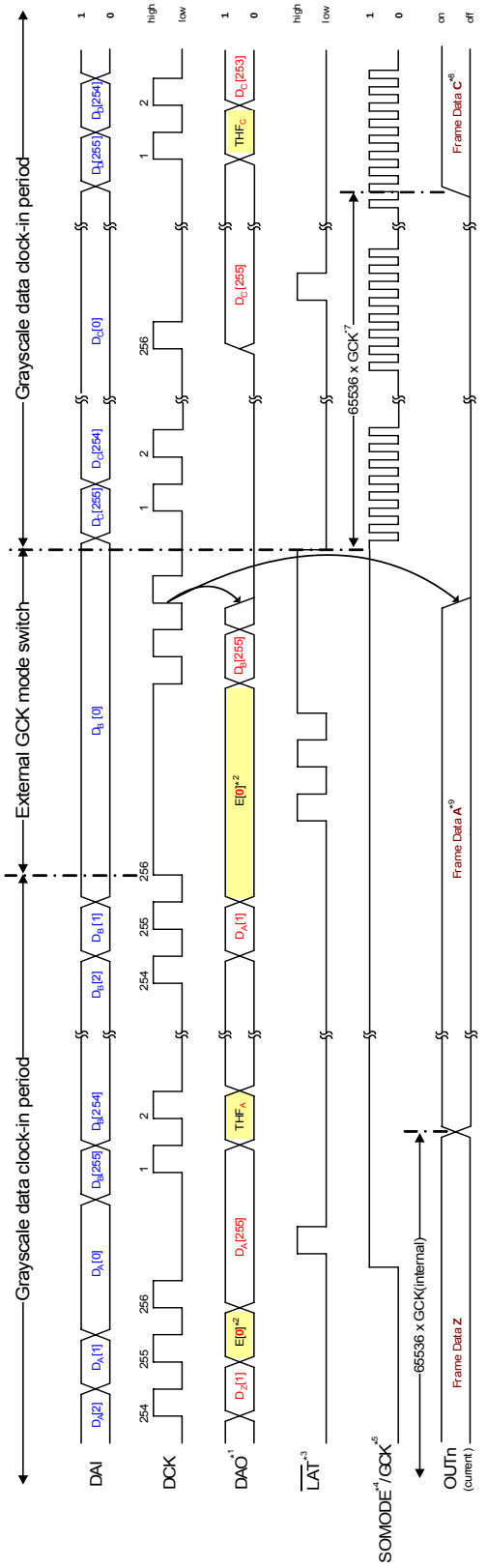
4. Output to Output Delay Time Unit (n=2,3,4,5,6,7,10,11,12,13,14,15)



5. GCK-OUT_0



Timing Diagram (free-running mode switch to external GCK mode example)



*1 DAO is shifted out on synchronization to rising / falling edge of DCK according to SOMODE is "L" / "H".

*2 E[0] is the error message of LED open/short detection according to O/S flag is "L" / "H".

*3 THF is the flag of alarm / shutdown according to O/S flag is "L" / "H".

*4 $\overline{LAT}$ is level trigger, not edge trigger.

*5 SOMODE function work in free-running mode. SOMODE default value is "L" when external GCK mode selected.

*6 When switching to external GCK mode, all registers in DM634 will be reset simultaneously.

*7 Starting the new PWM frame after the last PWM period finish competely.

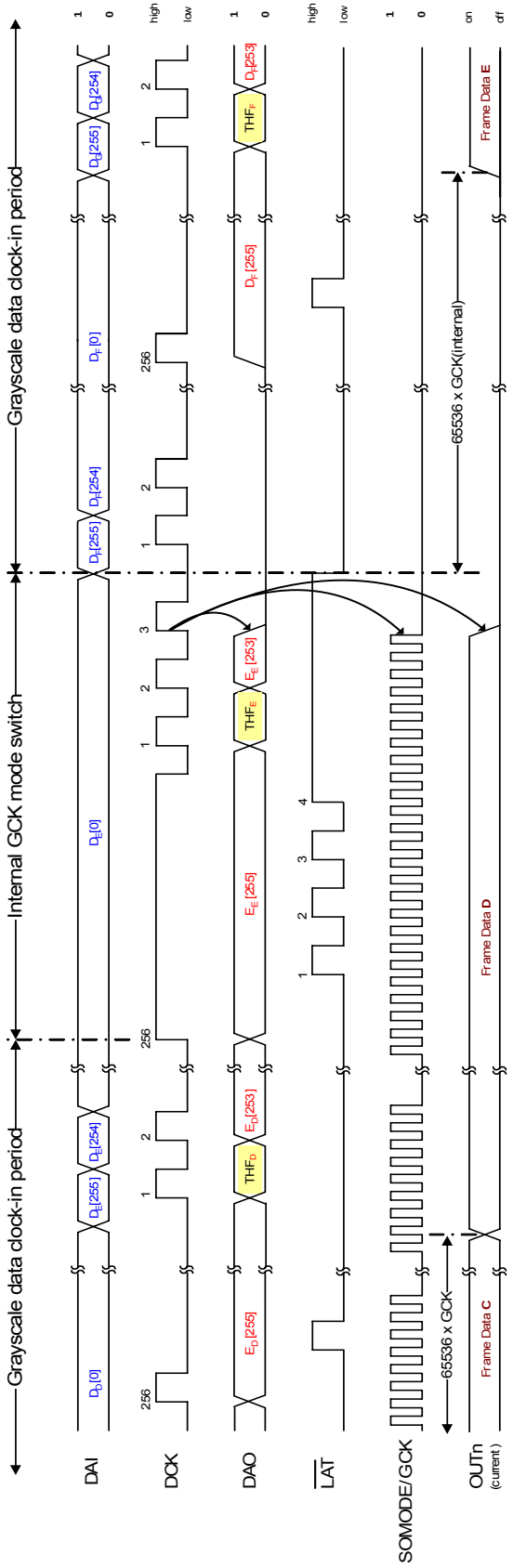
*8 When swithcing to GCK mode, outputs will be active after 65536 GCK pulses.

When using external frequency for PWM operation, the PWM refresh rate (frame rate) can be calculated by following equation :

$$\text{Refresh Rate (Hz)} = \frac{\text{Input GCK Frequency (Hz)}}{\text{Total PWM resolution } (2^{16})}$$

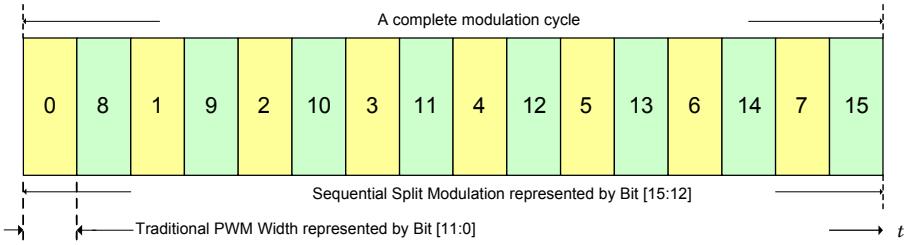
For example, if the refresh rate in display system is higher than 60Hz, the input GCK frequency must be higher than 4M Hz.

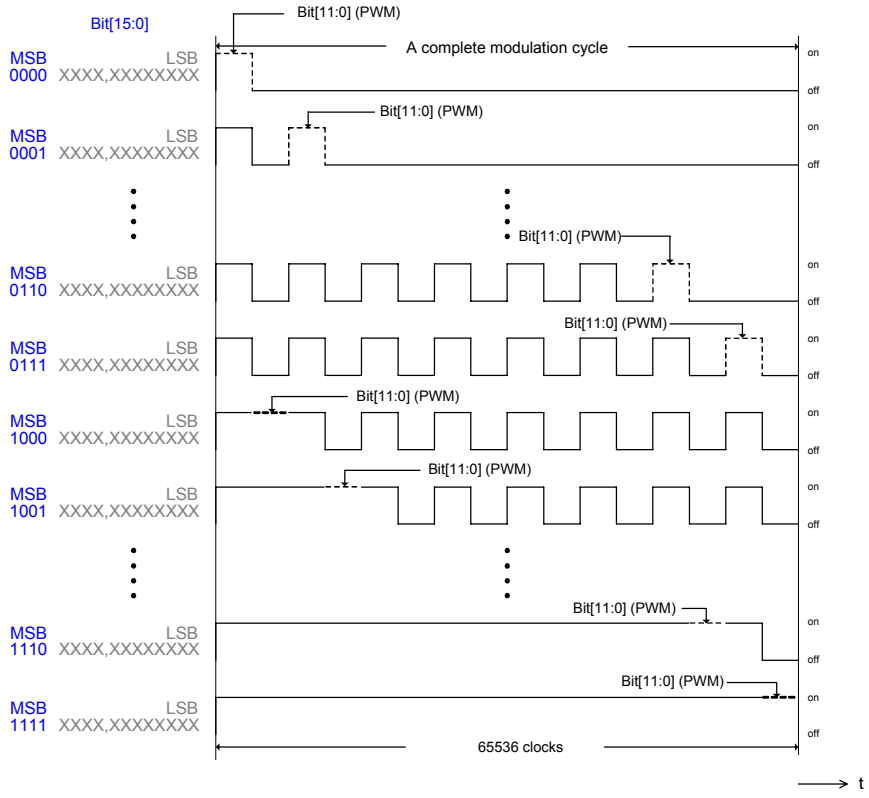
Timing Diagram (external GCK mode switch to free-running mode example)



Output Modulation Technique

DM634 provides a new LED drive technique of output modulation. It mixes traditional Pulse Width Modulation (PWM) represented by LSB 12 bit with Sequential Split Modulation (SSM) represented by MSB 4 bit. The main benefits of SSM are to drive LED with an equivalent higher refresh rate (up to 380Hz in DM634 when F_{GCK} = 25MHz) and change bit to next bit smoothly. The relationships between PWM and SSM in time domain can be refer to the diagram below (not to scale):





Ultra High Resolution Current Outputs

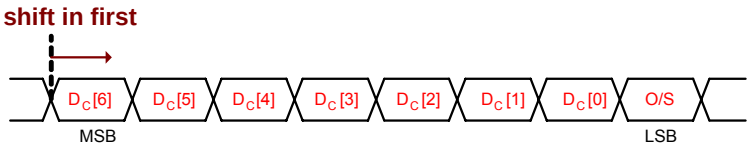
DM634 could provide 16-bit linear PWM control current outputs for each channel. There are two advantages for system design. One is DM634 has sufficient bit resolution (65536 steps), not only LED color information but additional data such as global brightness, dot correction, and gamma correction can be represented by the proper algorithms. The other is to reduce a lot of clock and data rate compared to conventional ON-OFF type LED drivers.

High Accuracy Global Brightness Correction

DM634 has built-in global brightness Correction feature. It can save PCB space and cost of system by eliminating the circuit of Rrext value adjusting or voltage drop adjusting across the external resistors. The output current is calculating by following equation[*1*2*3]:

$$Iout^{*1} = Vrext / Rext \times M^{*2} \times (1 + D_{GBC}{}^{*3})/96$$

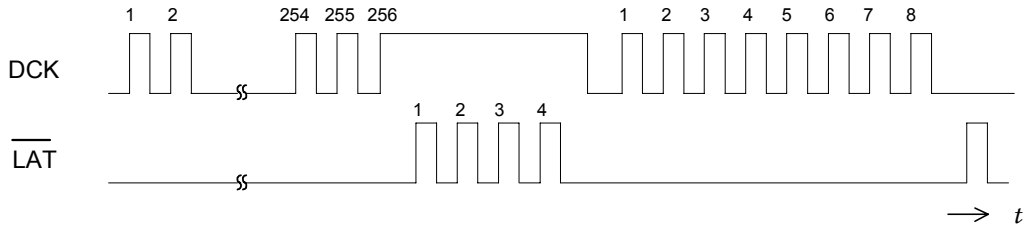
Global Brightness data and Open/Short Flag format



The Shift in data sequence of GBC data and detection flag as above. Dc[6], Dc[5] to Dc[0] are 7-bit data of GBC value. The last bit O/S is the flag of detection. When O/S flag set “L”, the LED open detection function be selected. Otherwise, if the flag set “H”, the LED short failure detection function be selected. .

Global Brightness Control

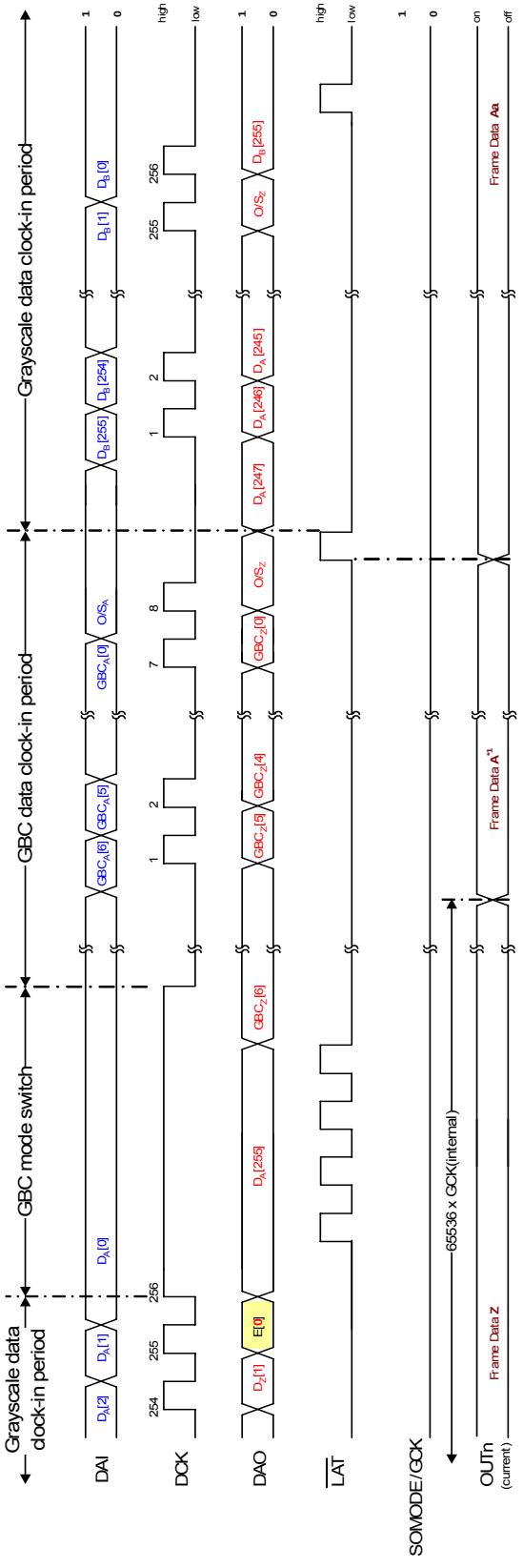
The default GBC data (D_{GBC}) is “1011111” (Iout = 75% Imax[*4]) after power-on. Users could shift GBC data in by following timing sequence without changing luminous data. The sequence shows four triggering latch pulses ($\overline{LAT}$) with high level clock (DCK), circuit switch into GBC mode at falling edge of the 4th latch pulse ($\overline{LAT}$) then user can make eight triggering clock pulses to set 7-bit GBC data and O/S flag. Notice that PWM data won’t be changed while GBC data is latched.



Timing Combination to set GBC data and O/S flag

[*1] Iout is the current value setting under 100% PWM duty cycle.
[*2] Vrext/Rext * M as the equation in Page 9.
[*3] D_{GBC} is the data of global brightness correction. User can refer to Timing Sequence to know how to set D_{GBC} on page 18.
[*4] Imax means the GBC data is “1111111”.

Timing Diagram (GBC data input example)



*1 The difference between Frame data A and Aa is max output current.

Output to Output Delay

DM634 has build-in output to output delay with a special arrangement. This arrangement help chip avoid noise cause by large current during channels switching. The arrangement details are shown as following table.

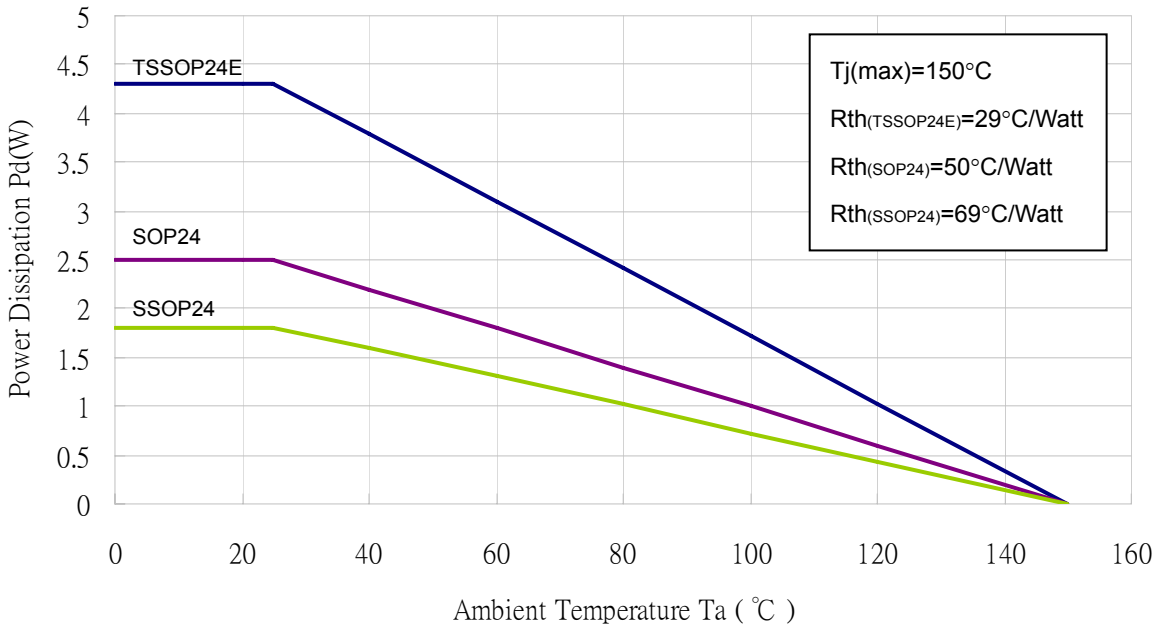
Channel	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Delay units	0	4	1	5	2	6	3	7	3	7	2	4	1	5	0	4

Power Dissipation

The power dissipation of a semiconductor chip is limited to its package and ambient temperature, in which the device requires the maximum output current calculated for given operating conditions. The maximum allowable power consumption can be calculated by the following equation:

$$Pd(max)(Watt) = \frac{Tj(junction\ temperature)(max)(℃) - Ta(ambient\ temperature)(℃)}{Rth(junction\text{-}to\text{-}air\ thermal\ resistance)(℃/Watt)}$$

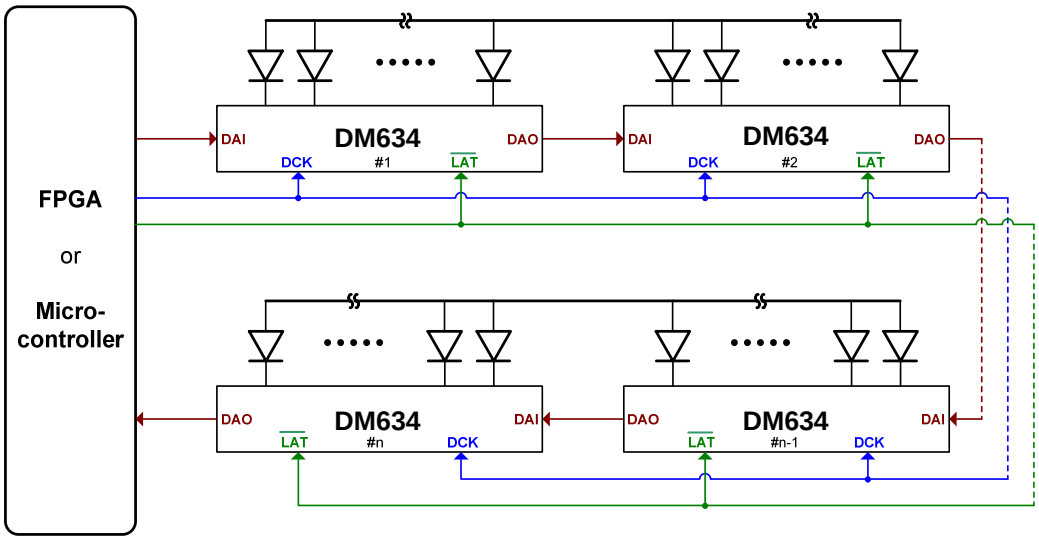
The relationship between power dissipation and operating temperature can be referred to the figure below:



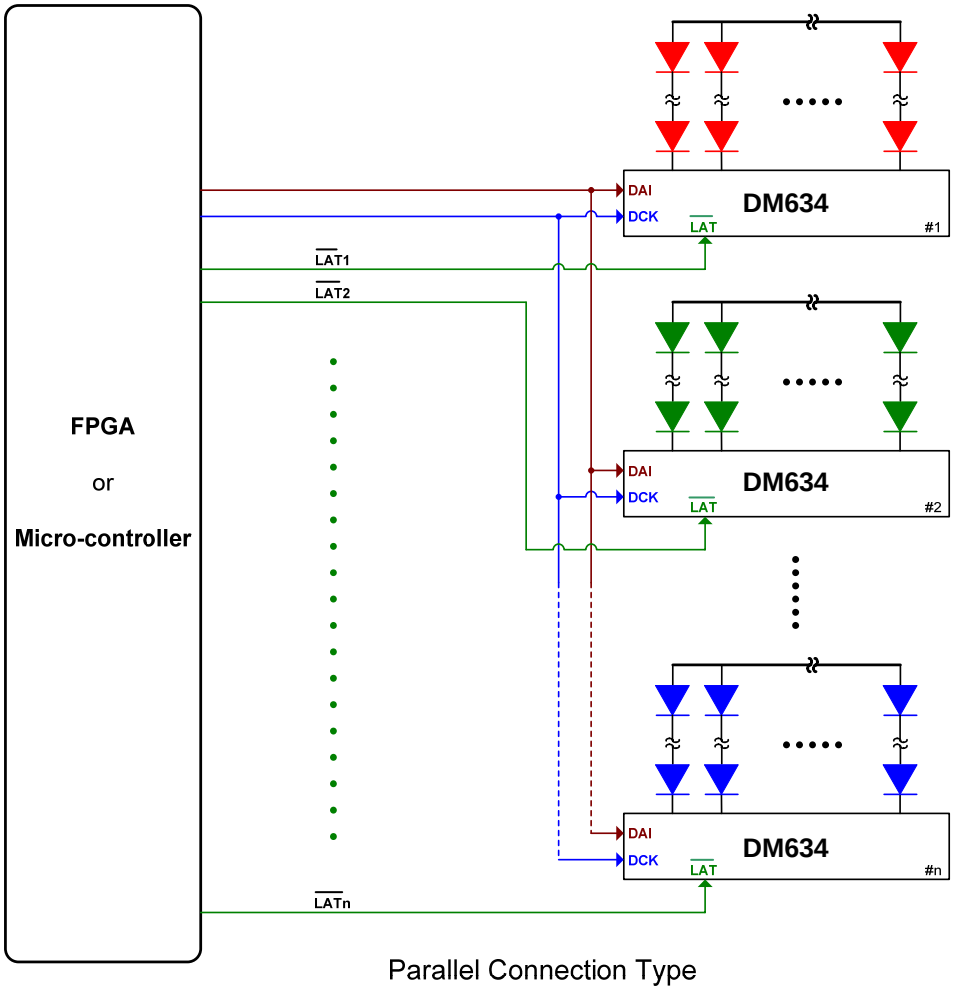
The power consumption of IC can be determined by the following equation and should be less than the maximum allowable power dissipation:

$$Pd(W) = V_{CC}(V) \times I_{DD}(A) + Vout0 \times Iout0 \times Duty0 + \cdots\cdots + Vout15 \times Iout15 \times Duty15 \leq Pd(max)(W)$$

Typical Application



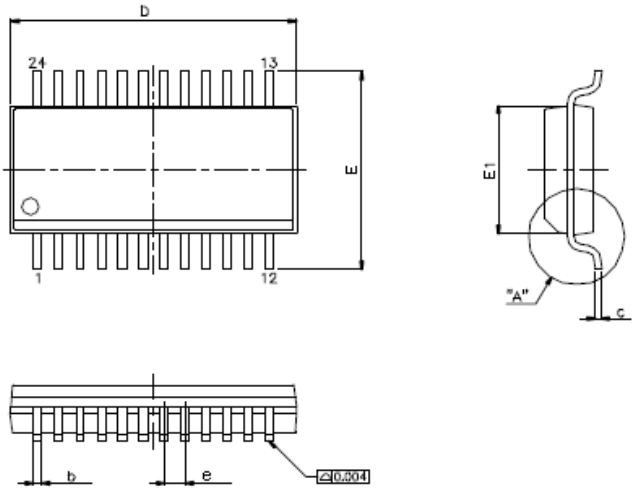
Serial Connection Type



Parallel Connection Type

Package Outline Dimension

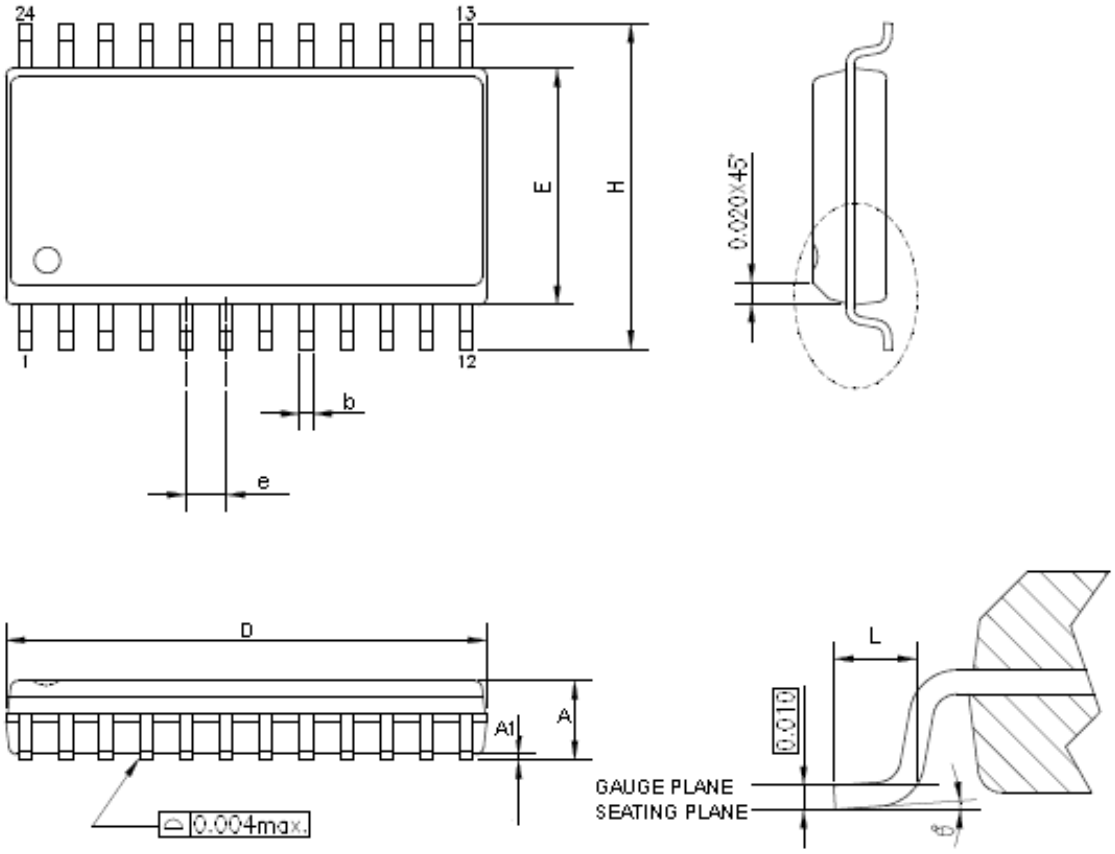
DM634-SSOP



SYMBOLS	DIMENSIONS IN INCH			DIMENSIONS IN MM		
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	-	-	0.059	-	-	1.499
b	0.008	-	0.012	0.203	-	0.305
C	0.007	-	0.010	0.178	-	0.254
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
e	0.025 BSC			0.635 BSC		
E1	0.150	0.154	0.157	3.810	3.912	3.988
L	0.016	0.025	0.050	0.406	0.635	1.270
L1	0.041 BSC			1.041 BSC		
θ°	0	-	8	0	-	8

Package Outline Dimension

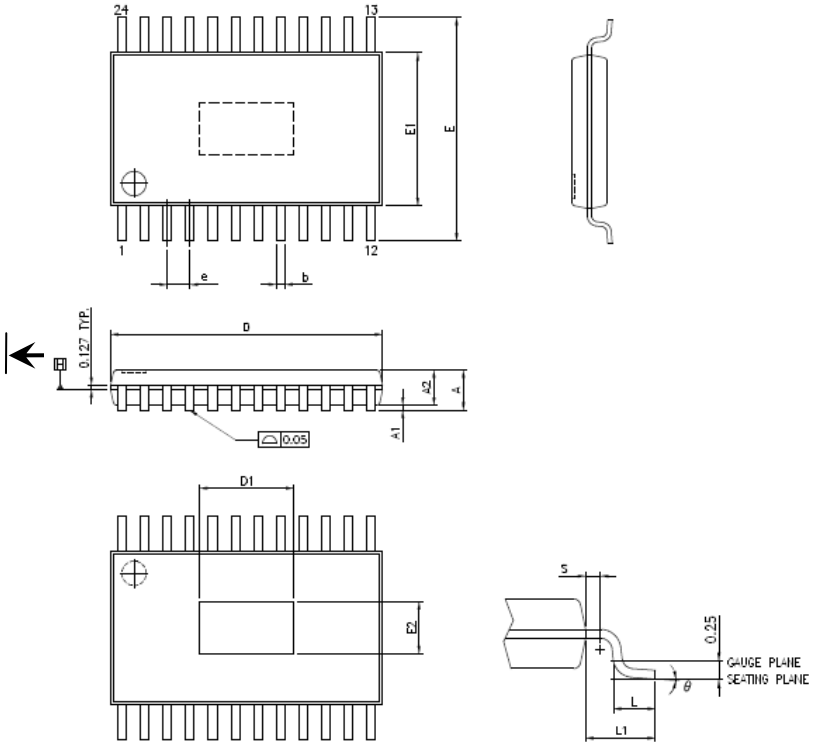
DM634-SOP



SYMBOLS	DIMENSIONS IN INCH			DIMENSIONS IN MM		
A	-	-	0.104	-	-	2.642
A1	0.004	-	-	0.102	-	-
b	0.016 BSC			0.406 BSC		
D	0.612	0.618	0.624	15.545	15.697	15.850
E	0.292	0.296	0.299	7.417	7.518	7.595
e	0.05 BSC			1.270 BSC		
H	0.405	0.412	0.419	10.287	10.465	10.643
L	0.021	0.031	0.041	0.533	0.787	1.041
θ°	0	4	8	0	4	8

Package Outline Dimension

DM634-TSSOP (exposed pad)



SYMBOLS	DIMENSIONS IN INCH			DIMENSIONS IN MM		
A	-	-	0.047	-	-	1.200
A1	0.000	-	0.006	0.000	-	0.150
A2	0.031	0.039	0.041	0.800	1.000	1.050
b	0.007	-	0.012	0.190	-	0.300
D	0.303	0.307	0.311	7.700	7.800	7.900
E1	0.169	0.173	0.177	4.300	4.400	4.500
E	0.252 BSC			6.400 BSC		
e	0.0256 BSC			0.650 BSC		
L1	0.039 REF			1.000 REF		
L	0.018	0.024	0.030	0.450	0.600	0.750
S	0.008	-	-	0.200	-	-
θ°	0	-	8	0	-	8
PAD SIZE (112×18E)						
E2	0.090	-	0.112	2.280	-	2.850
D1	0.146	-	0.182	3.700	-	4.620

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