28-Bit to 56-Bit Registered Buffer With Address Parity Test One Pair to Four Pair Differential Clock PLL Driver

Check for Samples: SN74SSQEB32882

FEATURES

- **1-to-2 Register Outputs and 1-to-4 Clock Pair Outputs Support Stacked DDR3 RDIMMs**
- **CKE Powerdown Mode for Optimized System Power Consumption**
- **1.5V/1.35V/1.25V Phase Lock Loop Clock Driver for Buffering One Differential Clock Pair (CK and $\overline{CK}$) and Distributing to Four Differential Outputs**
- **1.5V/1.35V/1.25V CMOS Inputs**
- **Checks Parity on Command and Address (CS-Gated) Data Inputs**
- **Configurable Driver Strength**
- **Uses Internal Feedback Loop**

APPLICATIONS

- **DDR3 Registered DIMMs up to DDR3-1866**
- **DDR3L Registered DIMMs up to DDR3L-1600**
- **DDR3U Registered DIMMs up to DDR3U-1333**
- **Single-, Dual- and Quad-Rank RDIMM**

DESCRIPTION

This JEDEC SSTE32882 28-bit 1:2 or 26-bit 1:2 and 4-bit 1:1 registering clock driver with parity is designed for operation on DDR3 registered DIMMs with V_{DD} of 1.5 V, on DDR3L registered DIMMs with V_{DD} of 1.35 V and on DDR3U registered DIMMs with V_{DD} of 1.25 V.

All inputs are 1.5 V, 1.35V and 1.25 V CMOS compatible. All outputs are CMOS drivers optimized to drive DRAM signals on terminated traces in DDR3 RDIMM applications. The clock outputs Yn and $\overline{Yn}$ and control net outputs DxCKEn, $\overline{DxCSn}$ and DxODTn can be driven with a different strength and skew to optimize signal integrity, compensate for different loading and equalize signal travel speed.

The SN74SSQEB32882 has two basic modes of operation associated with the Quad Chip Select Enable ($\overline{QCSEN}$) input. When the $\overline{QCSEN}$ input pin is open (or pulled high), the component has two chip select inputs, $\overline{DCS0}$ and $\overline{DCS1}$, and two copies of each chip select output, $\overline{QACS0}$, $\overline{QACS1}$, $\overline{QBCS0}$ and $\overline{QBCS1}$. This is the "QuadCS disabled" mode. When the $\overline{QCSEN}$ input pin is pulled low, the component has four chip select inputs DCS[3:0], and four chip select outputs, $\overline{QCS}$[3:0]. This is the "QuadCS enabled" mode. Through the remainder of this specification, $\overline{DCS}$[n:0] will indicate all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. $\overline{QxCS}$[n:0] will indicate all of the chip select outputs.

The device also supports a mode where a single device can be mounted on the back side of a DIMM. If MIRROR=HIGH, Input Bus Termination (IBT) has to stay enabled for all input signals in this case.

The SN74SSQEB32882 operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going HIGH, and $\overline{CK}$ going LOW. This data could be either re-driven to the outputs or it could be used to access device internal control registers.

The input bus data integrity is protected by a parity function. All address and command input signals are added up and the last bit of the sum is compared to the parity signal delivered by the system at the input PAR_IN one clock cycle later. If they do not match the device pulls the open drain output $\overline{ERROUT}$ LOW. The control signals (DCKE0, DCKE1, DODT0, DODT1, $\overline{DCS}$[n:0]) are not part of this computation.

The SN74SSQEB32882 implements different power saving mechanisms to reduce thermal power dissipation and to support system power down states. By disabling unused outputs the power consumption is further reduced.

The package is optimized to support high density DIMMs. By aligning input and output positions towards DIMM finger signal ordering and SDRAM ballout the device de-scrambles the DIMM traces allowing low cross talk design with low interconnect latency.

Edge controlled outputs reduce ringing and improve signal eye opening at the SDRAM inputs.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION

$T_{CASE(max)}$	PACKAGE(1)		ORDERABLE (2) PART NUMBER	TOP-SIDE MARKING
See Table 4	176ZAL	Tape and Reel	SN74SSQEB32882ZALR	EB32882A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

APPLICATION INFORMATION

Vendor Specific SPD Content

SPD EEPROM on DDR3 RDIMMs has 3 vendor specific bytes for vendor and revision ID. This information can be sued by the system BIOS. The following table showsthe correct values for SN74SSQEB32882.

Table 2. Vendor specific SPD content for SN74SSQEB32882

Byte	Value	Description
65	0x80	Vendor ID, part 1
66	0x97	Vendor ID, part 2
67	0x33	Revision ID

Application Reports

For additional Information on SN74SSQEB32882 DDR3 Register please review the following application reports:

- DDR3 Register CMR programming
- DDR3 RDIMM SPD settings
- Yn phase shift on SN74SSQEA32882
- DDR3 Register IBT Measurement

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings Over Operating Free-Air Temperature Range(1)

PARAMETER			VALUE	UNIT
V_{DD}	Supply voltage		–0.4 to +1.975	V
V_I	Receiver input voltage	See (2) and (3)	–0.4 to V_{DD} + 0.5	V
V_{REF}	Reference voltage		–0.4 to V_{DD} + 0.5	V
V_O	Driver output voltage	See (2) and (3)	–0.4 to V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	–50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$	±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin		±100	mA
T_{stg}	Storage temperature		–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 1.975 V maximum.

Table 4. Case Temperature vs Speed Node

PARAMETER		DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	UNIT
$T_{case(max)}$	Maximum case temperature (1)	+109	+108	+106	+103	+101	°C

(1) The temperature values fit to JEDEC RAW cards A, B, and C. The user must keep T_{case} below the specified values in order to keep the junction temperature below +125°C. Other combinations of features and termination resistors can require lower case temperature and extra cooling. These combinations depend on the specific application.

PACKAGE INFORMATION

Pinout Configuration

The package is a 8mm × 13.5mm 176-pin BGA with 0.65mm ball pitch in a 11 × 20 grid. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.65mm ball pitch.

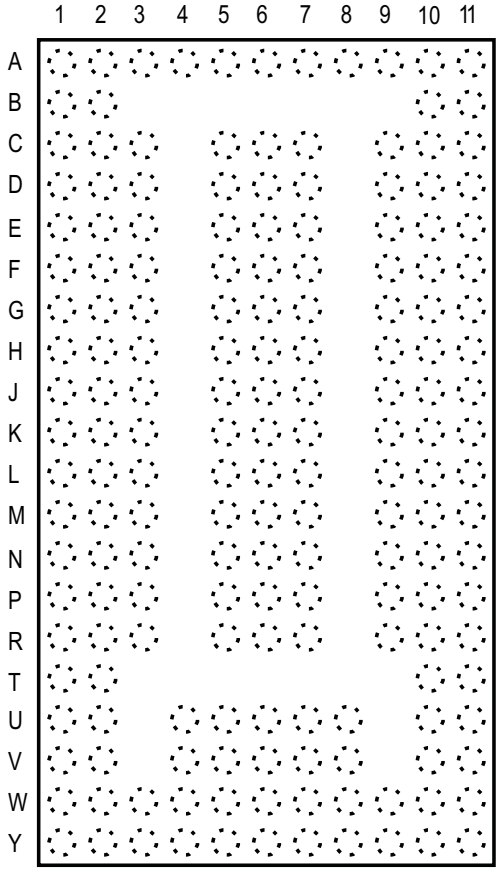


Figure 1. Pinout Configuration

www.ti.com

PACKAGING INFORMATION

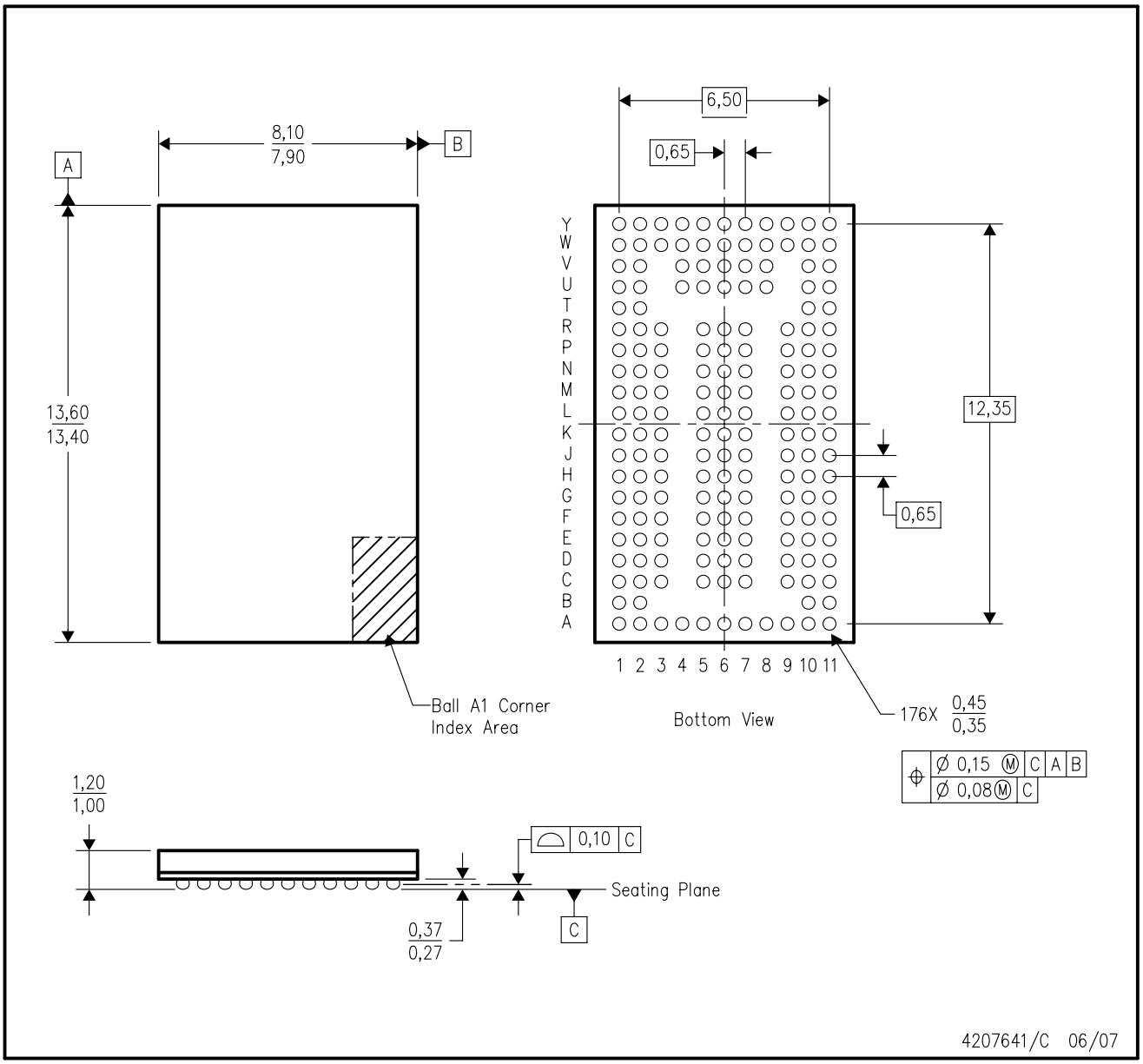
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
SN74SSQEB32882ZALR	ACTIVE	BGA	ZAL	176	1000	Green (RoHS & no Sb/Br)	SNAGAU	Level-3-260

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

ZAL (R–PBGA–N176) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This package is lead–free.

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