REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET	55	56	57																
REV																			
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS															
REV															
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Charles F. Saffle

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles F. Saffle

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
99-06-16

MICROCIRCUIT, DIGITAL, CMOS, BUS INTERFACE TERMINAL CONTROLLER, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	5962-99581
	A	67268	

SHEET 1 OF 57

DSCC FORM 2233
APR 97

5962-E344-99

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	99581	01	Q	X	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AR629	Bus interface terminal controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA7-P180	180	Ceramic pin grid array

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage (V_{DD})	-0.5 V dc to +7.0 V dc
Input or Output voltage (V_O,V_I)	-0.5 V dc to V_{DD}+ 0.5 V dc
Maximum power dissipation (P_D)	500 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-ambient (θ_{JA})	26°C/W
Junction Temperature (T_J)	+150°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage (V_{DD})	4.75 V dc to +5.25 V dc
Ground (V_{SS})	0.0 V dc
Input voltage (V_I)	V_{SS} to V_{DD}
Output voltage (V_O)	V_{SS} to V_{DD}
Ambient temperature (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to V_{SS} = GND.
3/ The limits for the parameters specified herein shall apply over the full specified VCC range and case temperature range of -55°C to +125°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
DC Parametric Tests							
Continuity test		Upper diode, lower diode	1, 2, 3	01	Pass		
Known state I_{DD}	SI_{DD}	V_{DD} = 5 V	1, 2, 3	01		6.0	mA
Known state (Magnitude)	SI_{SS}	V_{DD} = 4.75 V, V_{DD} = 5 V, V_{DD} = 5.25 V	1, 2, 3	01		1.5	mA
Input capacitance	C_{IN}	f = 1 Mhz 1/	4	01		20	pF
Output capacitance	C_{OUT}	f = 1 Mhz 1/	4	01		20	pF
High level input voltage	V_{IH}	V_{DD} = V_{DD} max, V_{DD} = V_{DD} min 2/	1, 2, 3	01	2.0		V
Low level input voltage	V_{IL}	V_{DD} = V_{DD} max, V_{DD} = V_{DD} min 2/	1, 2, 3	01		0.8	V
High level output voltage	V_{OH}	V_I = V_{DD} or V_{SS}, I_{OH} = -20 µA	1, 2, 3	01	V_{DD}-0.1		V
Low level output voltage	V_{OL}	V_I = V_{DD} or V_{SS}, I_{OL} = 20 µA	1, 2, 3	01		0.1	V
High level output current	I_{OH}	V_I = V_{DD} or V_{SS}, V_{OH} = V_{DD} –0.8 V, V_{DD} = V_{DD} min	1, 2, 3	01		-4.0	mA
Low level output current	I_{OL}	V_I = V_{DD} or V_{SS}, V_{OL} = 0.4V, V_{DD} = V_{DD} min	1, 2, 3	01	4.0		mA
Input Leakage current	I_{IL}	No pull resistor	1, 2, 3	01	-10	10	µA
Input Leakage current	I_{IH}	V_I = V_{DD} or V_{SS}, V_{DD} = V_{DD} max	1, 2, 3	01	-10	10	µA
Input current with pull-up resistor	I_{PU}	V_I = V_{SS} or V_{DD}, V_{DD} = V_{DD} max	1, 2, 3	01	-200	20	µA
Output leakage current high, no pull	I_{OZH}	V_O = V_{DD} , V_{DD} = V_{DD} max 3/	1, 2, 3	01		10	µA
Output leakage current low, no pull	I_{OZL}	V_O = V_{SS} , V_{DD} = V_{DD} max 3/	1, 2, 3	01	-10		µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
DC Parametric Tests - continued							
Output leakage current, pull-up	I_{OPL}	$V_O = V_{SS}$ 3/	1, 2, 3	01	-200		µA
Output leakage current, pull-up	I_{OPH}	$V_O = V_{DD}$, 3/ $V_{DD} = V_{DD}$ max	1, 2, 3	01		20	µA
Dynamic supply current	D_{IDD}	FC = 32 Mhz, $V_{DD} = V_{DD}$ max	1, 2, 3	01		110.0	mA
Positive going Schmitt trigger input threshold	V_{t+}	$V_{DD} = V_{DD}$ max, $V_{DD} = V_{DD}$ min	1, 2, 3	01		0.75 V_{DD}	V
Negative going Schmitt trigger input threshold	V_{t-}	$V_{DD} = V_{DD}$ max, $V_{DD} = V_{DD}$ min	1, 2, 3	01	1.0		V
Schmitt hysteresis voltage	V_H	$V_{DD} = V_{DD}$ max, $V_{DD} = V_{DD}$ min	1, 2, 3	01	1.0		V
Gross functional		$V_{DD} = 5.0$ V, $V_{DD} = 4.75$ V, $V_{DD} = 5.25$ V	7, 8	01	pass		
Fmax functional		$V_{DD} = 5.0$ V, $V_{DD} = 4.75$ V, $V_{DD} = 5.25$ V	7, 8	01	Pass		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
AC Subsystem Read Characteristics 4/							
AD Setup time to ASO high	T_{AAS}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	3T-40	3T+25	ns
DMA start to DMA start	T_{BDMA}	$V_{DD} = 5\ V \pm 5\%$	9, 10, 11	01	315T		ns
Delay from DSO rising edge to tri-state	T_{D3S}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	1T-20	1T+40	ns
Delay from RICK to ASO low	T_{DAS}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	1T	1T+40	ns
BSAO high delay from BUSA high	T_{DBAH}		9, 10, 11	01		25	ns
BUSA response time	T_{DBAK}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	0	130T	ns
BUSA response time (1 WAT)	T_{DBAK1}	$V_{DD} = 5\ V \pm 5\%$	9, 10, 11	01	0	126T	ns
BUSA response time (WAIT)	T_{DBAKW}	$V_{DD} = 5\ V \pm 5\%$	9, 10, 11	01	0	122T-TWRWT	ns
BSAO low delay from BUSR high, BUSA low	T_{DBAL}		9, 10, 11	01		25	ns
Time from BUSA low to BUSR tri-state	T_{DBABR}	0 WAIT	9, 10, 11	01		17T+61	ns
		1 WAIT				21T-61	
		Max WAIT				148T+61	
BUSR high to BUSA high delay	T_{DBRBA}		9, 10, 11	01	31		ns
Delay from RICK to BUSR low	T_{DBRQ}		9, 10, 11	01		80	ns
Time BUSA low prior to RICK	T_{DBSW}		9, 10, 11	01	1T-10	5T+26	ns
DSO Delay from RICK	T_{DDS}		9, 10, 11	01		80	ns
DSO high to BUSR tri-state	T_{DDSBR}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	1T-20	1T+50	ns
IOCK high after rising edge of RICK	T_{DIO}		9, 10, 11	01		37	ns
RICK to DSO high	T_{DRDSH}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	1T	1T+40	ns
RWO delay from RICK	T_{DRW}		9, 10, 11	01		80	ns
AD hold time from ASO high	T_{HASA}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	2T-35	2T+40	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
AC Subsystem Read Characteristics – continued 4/							
Wait hold after RICK	T_{HAW}		9, 10, 11	01	22		ns
Data in hold after RICK	T_{HDI}		9, 10, 11	01	30		ns
DSO hold after WAIT	T_{HDS}	V_{DD} = 4.75 V, V_{DD} = 5 V ± 5%	9, 10, 11	01	5T	9T+30	ns
RWO hold after WAIT	T_{HRW}	V_{DD} = 4.75 V, V_{DD} = 5 V ± 5%	9, 10, 11	01	6T	10T+30	ns
ASO hold after WAIT	T_{HWAS}	V_{DD} = 5 V ± 5%	9, 10, 11	01	6T	10T+30	ns
Data setup prior to RICK	T_{SDI}		9, 10, 11	01	30		ns
WAIT setup to RICK	T_{SWA}		9, 10, 11	01	22		ns
ASO pulse width	T_{WAS}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	2T-25	2T+25	ns
DSO pulse width	T_{WDS}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	6T-25		ns
Read WAIT Pulse width	T_{WRWT}	V_{DD} = 4.75 V, V_{DD} = 5 V ± 5%	9, 10, 11	01		122T	ns
WAIT pulse width high	T_{WWH}		9, 10, 11	01	4T+22		ns
AC Subsystem Write Characteristics 4/							
Delay from ASO High to DSO low	T_{DASDS}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	4T-25	4T+25	ns
BUSA response time	T_{DBAK}	TG = 2, V_{DD} = 5 V ± 5%	9, 10, 11	01	0	130T	ns
		TG = 3, V_{DD} = 5 V ± 5%			0	162T	
		TG = 4, V_{DD} = 5 V ± 5%			0	194T	
		TG = 5, V_{DD} = 5 V ± 5%			0	226T	
		TG = 6, V_{DD} = 5 V ± 5%			0	258T	
BUSA response time (1WAT)	T_{DBAK1}	TG = 2, V_{DD} = 5 V ± 5%	9, 10, 11	01	0	126T	ns
		TG = 3, V_{DD} = 5 V ± 5%			0	158T	
		TG = 4, V_{DD} = 5 V ± 5%			0	190T	
		TG = 5, V_{DD} = 5 V ± 5%			0	222T	
		TG = 6, V_{DD} = 5 V ± 5%			0	254T	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
AC Subsystem Write Characteristics – continued 4/							
BUSA response time (WAIT)	T_{DBAKW}	TG = 2, V_{DD} = 5 V ± 5%	9, 10, 11	01	0	122T-TWWWT	ns
		TG = 3, V_{DD} = 5 V ± 5%			0	154T-TWWWT	
		TG = 4, V_{DD} = 5 V ± 5%			0	186T-TWWWT	
		TG = 5, V_{DD} = 5 V ± 5%			0	218T-TWWWT	
		TG = 6, V_{DD} = 5 V ± 5%			0	250T-TWWWT	
Data out to DSO low	T_{HDDS}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	2T-35		ns
Data out hold from DSO	T_{HDSD}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	1T-5	1T+25	ns
Rcv DMA start to transmit DMA start	T_{RTDMA}	TG = 2, V_{DD} = 5 V ± 5%	9, 10, 11	01	275T		ns
		TG = 3, V_{DD} = 5 V ± 5%			307T		
		TG = 4, V_{DD} = 5 V ± 5%			315T		
		TG = 5, V_{DD} = 5 V ± 5%			315T		
		TG = 6, V_{DD} = 5 V ± 5%			315T		
DSO pulse width	T_{WDS}	V_{DD} = 4.75 V, V_{DD} = 5.25 V 5/	9, 10, 11	01	4T-25		ns
Write WAIT pulse width	T_{WWWT}	TG = 2, V_{DD} = 5 V ± 5%	9, 10, 11	01		122T	ns
		TG = 3, V_{DD} = 5 V ± 5%				154T	
		TG = 4, V_{DD} = 5 V ± 5%				186T	
		TG = 5, V_{DD} = 5 V ± 5%				218T	
		TG = 6, V_{DD} = 5 V ± 5%				250T	
Time from BUSA low to BUSR tri-state	T_{DBABR}	0 WAIT, V_{DD} = 5 V ± 5%	9, 10, 11	01		17T+61	ns
		1 WAIT, V_{DD} = 5 V ± 5%				21T+61	
		Max WAIT, V_{DD} = 4.75 V				148T+61	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
AC Internal Register Access Characteristics 4/							
Delay from ASO high to DSO falling edge	T_{DASDS}		9, 10, 11	01	20		ns
Delay from CS falling edge to ASO falling edge	T_{DCSAS}		9, 10, 11	01	0		ns
Delay from DSO rising edge to CS rising edge	T_{DCSDS}		9, 10, 11	01	0		ns
Delay from CS falling edge to WAIT high	T_{DCSFW}		9, 10, 11	01		26	ns
Delay from CS rising edge to WAIT release	T_{DCSRW}		9, 10, 11	01		27	ns
Data valid after rising edge of DSO	T_{DHO}		9, 10, 11	01	0		ns
Error register data valid after falling edge of DSO	T_{DSO}	$V_{DD} = 5\ V \pm 5\%$	9, 10, 11	01		2T+25	ns
LWM/IVR data valid after falling edge of DSO	T_{DSO}		9, 10, 11	01		40	ns
Address hold time after rising edge of ASO	T_{HAI}		9, 10, 11	01	15		ns
Address setup time prior to rising edge of ASO	T_{SAI}		9, 10, 11	01	30		ns
Address strobe pulse width	T_{WAS}		9, 10, 11	01	30		ns
AC Internal Register/Receive Valid and Interrupt Vector Strobe Timing 4/							
Delay from AE low to AO active	T_{DAOA}	$V_{DD} = 4.75\ V$, $V_{DD} = 5.25\ V$ 5/	9, 10, 11	01	0	25	ns
Delay from AE high to AO tri-state	T_{DAOZ}	$V_{DD} = 4.75\ V$, $V_{DD} = 5.25\ V$ 5/	9, 10, 11	01	0	40	ns
RERF pulse width	T_{LRERF}	$V_{DD} = 5\ V \pm 5\ \%$	9, 10, 11	01	7T		ns
XERF pulse width	T_{LXERF}	$V_{DD} = 5\ V \pm 5\ \%$	9, 10, 11	01	7T		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
AC Internal Register / Receive Data Characteristics 4/							
Delay from BUSQ to leading RIVS low	T_{DBRIVS}	V_{DD} = 5 V ± 5 % 6/	9, 10, 11	01		90T	ns
Delay from end of last bit time to BUSQ	T_{DBUSQ}		9, 10, 11	01	6T-40	7T+46	ns
Delay from last word of string to BUSQ	T_{DBUSQ1}		9, 10, 11	01	5T-40	7T+46	ns
Delay from BUSQ to error register valid (non-NRBA)	T_{DERR}	V_{DD} = 4.75 V, V_{DD} = 5 V ± 5 %	9, 10, 11	01	7T	64T	ns
Delay from BUSQ to error register valid (NRBA)	T_{DERR}	TG = 2, V_{DD} = 5 V ± 5 %	9, 10, 11	01	160T		ns
Delay from BUSQ to error register valid (NRBA error on next to last date word)	T_{DERR}	V_{DD} = 5 V ± 5 %	9, 10, 11	01		292T	ns
Delay from RIVS low to STAC low	T_{DFSTAC}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	5T-30	5T+35	ns
Delay from BUSQ to IVR valid	T_{DINT}		9, 10, 11	01	68T	75T	ns
Time from RIVS low to 12th bit time	T_{DLRIVS}		9, 10, 11	01		5T	ns
Delay from leading RIVS to trailing RIVS	$T_{DLTRIVS}$	V_{DD} = 5 V ± 5 % 7/	9, 10, 11	01		31T	ns
Delay from BUSQ to LWM valid	T_{DLWM}	V_{DD} = 5 V ± 5 %	9, 10, 11	01	12T	20T	ns
Delay from RIVS high to STAC high	T_{DRSTAC}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	2T-30	2T+35	ns
Delay from end of DMA to trailing RIVS low	T_{DTRIVS}		9, 10, 11	01	2T	46T	ns
AO hold after leading RIVS falling edge	T_{HRAL}	V_{DD} = 5 V ± 5 %	9, 10, 11	01	65T		ns
AO hold after trailing RIVS falling edge	T_{HRAT}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	4T-35		ns
AO setup prior to RIVS falling edge	T_{SAR}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	2T-35		ns
Delay from end of last bit time to DMA start	T_{SDMA}	V_{DD} = 4.75 V, V_{DD} = 5 V ± 5 %	9, 10, 11	01	13T	20T	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
AC Internal Register / Receive Data Characteristics - continued 4/							
Width of BUSQ high during data sync	T_{WBUSQ}		9, 10, 11	01		38T	ns
Width Bus Quiet high during interstring gap	T_{WBUSQ1}		9, 10, 11	01		64T	ns
RIVS pulse low width	T_{WRIVS}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	2T-10	2T+35	ns
Time from AO valid to DMA start	$T_{DAOBUSR}$	$V_{DD} = 5\ V \pm 5\ \%$	9, 10, 11	01	30T		ns
AC Internal Register / Transmit Data Characteristics 4/							
Time from AO valid to DMA window start	T_{AODMA}	$V_{DD} = 5\ V \pm 5\ \%$	9, 10, 11	01	1T		ns
Delay from end of last bit time to BUSQ	T_{DBUSQ}		9, 10, 11	01	6T-40	7T+46	ns
Delay from last word of string to BUSQ	T_{DBUSQ1}	$V_{DD} = 5\ V \pm 5\ \%$	9, 10, 11	01	5T-40	7T+46	ns
Delay from BUSQ to error register valid (non NXBA)	T_{DERR}	V_{DD} = 4.75 V, $V_{DD} = 5\ V \pm 5\ \%$	9, 10, 11	01	15T	124T	ns
BUSQ to error register valid (NXBA)	T_{DERR}	$V_{DD} = 5\ V \pm 5\ \%$	9, 10, 11	01	-340T		ns
Delay from XIVS to STAC low	T_{DFSTAC}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	5T-30	5T+35	ns
Delay from IVR valid to XIVS	T_{DINT}		9, 10, 11	01	14T	20T	ns
Delay from BUSQ to LWM valid	T_{DLWM}	$V_{DD} = 5\ V \pm 5\ \%$	9, 10, 11	01		20T	ns
Delay from 3rd bit to leading XIVS	T_{DLXIVS}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	3T-35	3T+55	ns
Delay from XIVS to STAC high	T_{DRSTAC}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	2T-30	2T+35	ns
Delay from parity bit to trailing XIVS	T_{DTXIVS}	V_{DD} = 4.75 V, $V_{DD} = 5\ V \pm 5\ \%$	9, 10, 11	01	48T	96T	ns
AO hold after leading XIVS falling edge	T_{HXAL}	$V_{DD} = 5\ V \pm 5\ \%$	9, 10, 11	01	65T		ns
AO hold after trailing edge of XIVS falling	T_{HXAT}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	4T-35		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
AC Internal Register / Transmit Data Characteristics – continued 4/							
AO setup prior to falling edge of XIVS	T_{SAX}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	2T-35		ns
Delay from bit 7 to DMA Start	T_{SDMA}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	13T-35	13T+60	ns
Width of BUSQ high during data sync	T_{WBUSQ}	V_{DD} = 5 V ± 5 %	9, 10, 11	01	30T	38T	ns
BUS quiet high during interstring gap	T_{WBUSQ1}	V_{DD} = 5 V ± 5 %	9, 10, 11	01	55T	64T	ns
XIVS pulse low width	T_{WXIVS}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	2T-10	2T+35	ns
AC Personality PROM Interface (XPP/RPP/MPP) Characteristics 4/							
Delay from CLRX high to XCS low	T_{DCLXCS}	V_{DD} = 5 V ± 5 %	9, 10, 11	01	24T	27T+9	ns
Delay from EXST high to STAC low	T_{DEXST}	8/	9, 10, 11	01		3T+35	ns
Delay from STAC low to EXST high	T_{DSTEX}	9/	9, 10, 11	01		5T+35	ns
EX3-0 output hold after EXT strobe	T_{HBEX}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	2T-10		ns
BUS1 address hold time after RICK	T_{HRB}	Single byte	9, 10, 11	01	2T		ns
BUS2 data input to RICK hold time	T_{HRB2}		9, 10, 11	01	60		ns
Receive PROM chip select hold after RICK	T_{HRCS}		9, 10, 11	01	2T		ns
Load strap hold time after RICK	T_{HRLS}		9, 10, 11	01	2T		ns
RZ2-0 address hold time after RICK	T_{HRRZ}		9, 10, 11	01	2T		ns
XX address hold time after RICK	T_{HRXX}		9, 10, 11	01	2T		ns
XY address hold time after RICK	T_{HRXY}		9, 10, 11	01	2T		ns
XZ address hold time after RICK	T_{HRXZ}		9, 10, 11	01	2T		ns
Transmit PROM chip select hold after RICK	T_{HXCS}		9, 10, 11	01	2T		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
AC Personality PROM Interface (XPP/RPP/MPP) Characteristics – continued 4/							
Minimum data hold time	T_{MHR}		9, 10, 11	01	60		ns
Minimum data setup time	T_{MSR}		9, 10, 11	01	30		ns
EX3-0 output stable before EXT strobe	T_{SBEX}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	6T-35		ns
BUS1 address setup time prior to RICK	T_{SRB}	Single byte, double byte, triple byte	9, 10, 11	01	14T-150		ns
BUS2 data input to RICK setup time	T_{SRB2}		9, 10, 11	01	30		ns
Load strap setup time prior to RICK	T_{SRLS}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	14T-70		ns
RZ2-0 address setup time prior to RICK	T_{SRRZ}	Single byte, double byte, triple byte	9, 10, 11	01	14T-150		ns
XX address setup time prior to RICK	T_{SRXX}	Single byte, double byte, triple byte	9, 10, 11	01	14T-150		ns
XY address setup time prior to RICK	T_{SRXY}	Single byte, double byte, triple byte	9, 10, 11	01	14T-150		ns
XZ address setup time prior to RICK	T_{SRXZ}	Single byte, double byte, triple byte	9, 10, 11	01	14T-150		ns
CLRX pulse width	T_{WCLRX}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	2T-10	2T+20	ns
Extension strobe pulse width	T_{WEXST}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	2T-10		ns
Receive PROM chip select setup time	T_{WRCS}	Single byte, double byte, triple byte	9, 10, 11	01	14T-40		ns
Transmit PROM chip select setup time	T_{WXCS}	Single byte, double byte, triple byte	9, 10, 11	01	14T-40		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
AC – Serial Transmit Characteristics 4/							
Time from TXHB low to TXO rising edge	T_1	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	1T-12	2T+24	ns
Time from TXHB high to TXO falling edge	T_2	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	1T-12	1T+24	ns
Time from GA rising edge to STAC falling edge	T_{DGAST}	$V_{DD} = 5\ V \pm 5\ \%$	9, 10, 11	01	104T	110T	ns
GA pulse width	T_{WGA}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01	3T-14	4T+10	ns
Data bit pulse width	T_{WDB}	V_{DD} = 4.75 V, V_{DD} = 5.25 V 10/	9, 10, 11	01	16T-15		ns
½ data bit pulse width	T_{WHDB}	V_{DD} = 4.75 V, V_{DD} = 5.25 V 11/, 12/	9, 10, 11	01	8T-15		ns
PPSSP pulse width	T_{WPPSSP}	V_{DD} = 4.75 V, V_{DD} = 5.25 V 11/	9, 10, 11	01	8T-10	10T+25	ns
PSSP pulse width	T_{WPSSP}	V_{DD} = 4.75 V, V_{DD} = 5.25 V 11/	9, 10, 11	01	8T-15		ns
AC XICK / RICK characteristics 4/							
Receive or transmit input clock frequency	F_C	$V_{DD} = 5\ V \pm 5\ \%$	9, 10, 11	01	0	32.32	Mhz
Clock period	T_C	$V_{DD} = 5\ V \pm 5\ \%$, TS = 1/FC	9, 10, 11	01	30.94		ns
Propagation delay from RICK to IOCK	T_{DIO}	5/	9, 10, 11	01		37	ns
Clock pulse width, high	T_{WH}	V_{DD} = 4.75 V, V_{DD} = 5.25 V 13/	9, 10, 11	01	0.33T	0.67T	ns
Clock pulse width, low	T_{WL}	V_{DD} = 4.75 V, V_{DD} = 5.25 V 13/	9, 10, 11	01	0.33T	0.67T	ns
Hold time of ADDATA bus after falling edge of DSO	T_{HDATA}	V_{DD} = 4.75 V, V_{DD} = 5.25 V	9, 10, 11	01		5	ns

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ Tested during initial qualification only and after process or design changes. Tested at +25°C only.

2/ TTL input only.

3/ All output leakage current is measured at tri-state.

4/ C_L = 50 pF for all tests.

5/ Same as National symbol T_{DAE}.

6/ Same as National symbol $T_{DBUSQRIVS}$.

7/ Same as National symbol $T_{DRIVSRIVS}$.

8/ Same as National symbol T_{DES}

9/ Same as National symbol T_{DSE}.

10/ Same as National symbol T_{WTXO}.

11/ These parameters are measured at 2.0 V on the rising and falling edges of a high pulse and extrapolated to 0.8 V on the rising and falling edges of a low pulse.

12/ Same as National symbol T_{WTXOH} and T_{WTXOL}.

13/ T_{WH} is measured from 0.75 V_{DD} on the clock rising edge and 0.75 V_{DD} -1.0 V on the clock falling edge. T_{WL} is measured from 1 V on the clock falling edge and 2V on the clock rising edge. The clock used to measure these parameters has a minimum slew rate of 1.0 V/ ns.

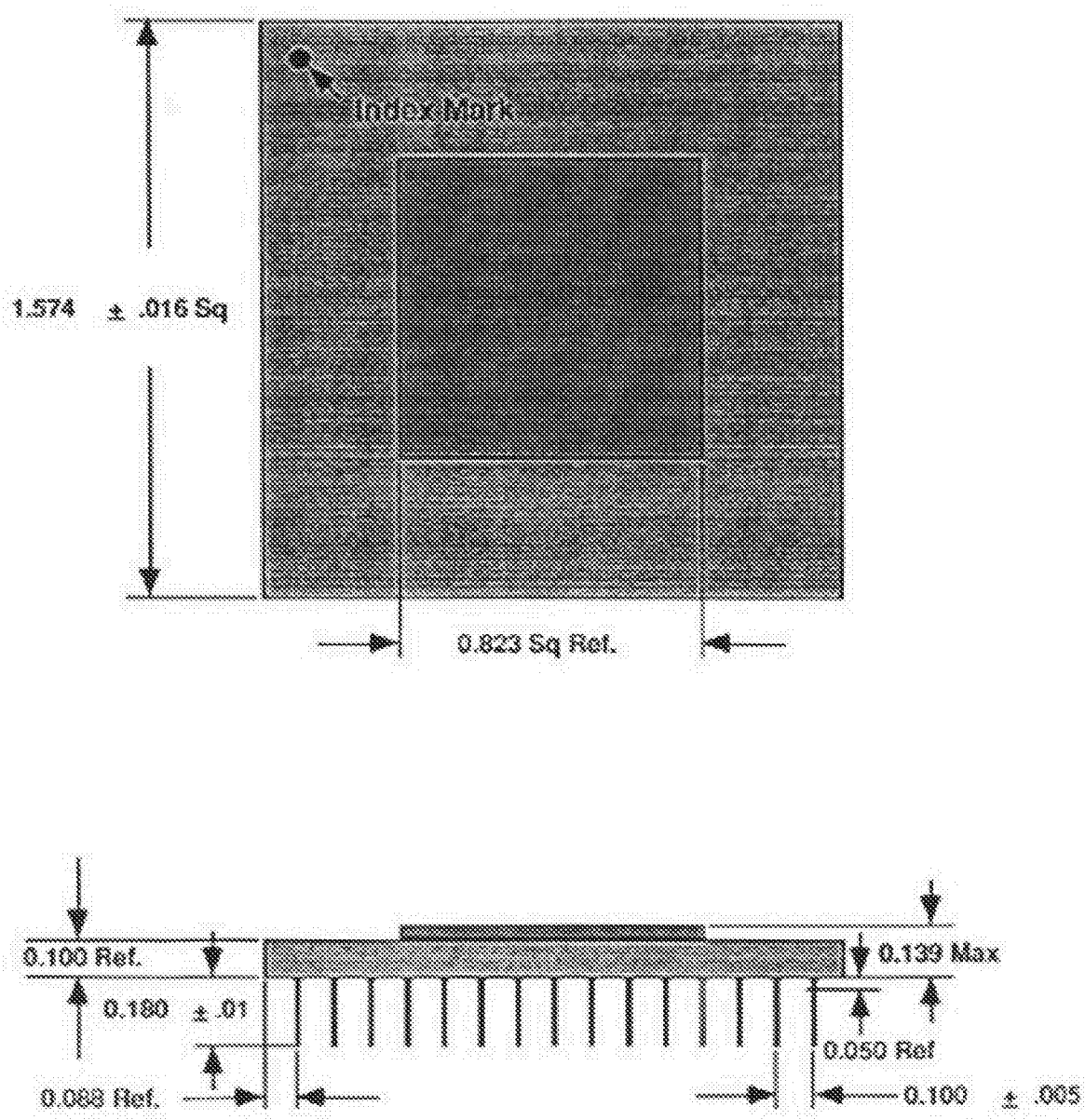


Figure 1. Case outline

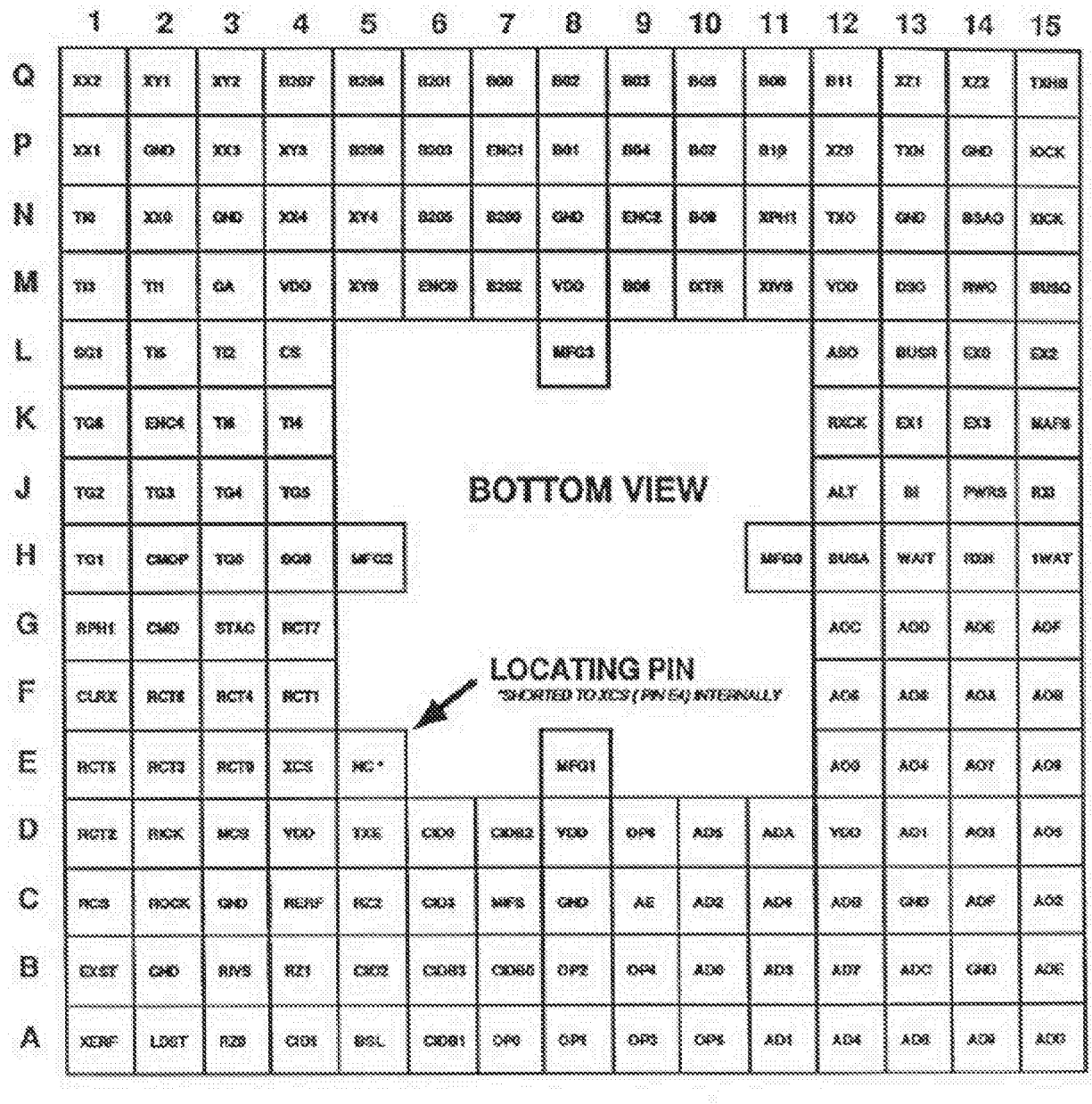


FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-99581
		REVISION LEVEL	SHEET 19

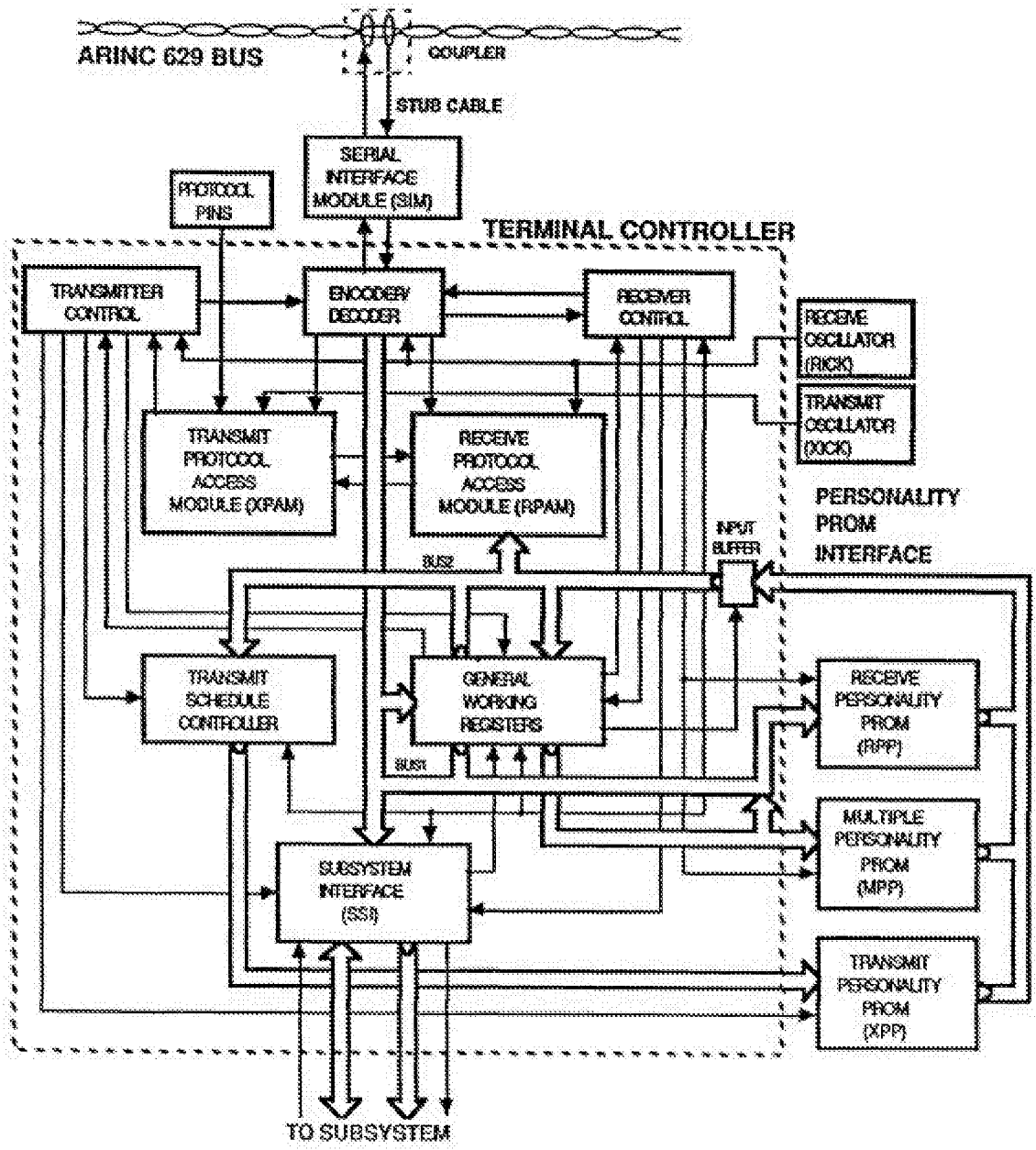
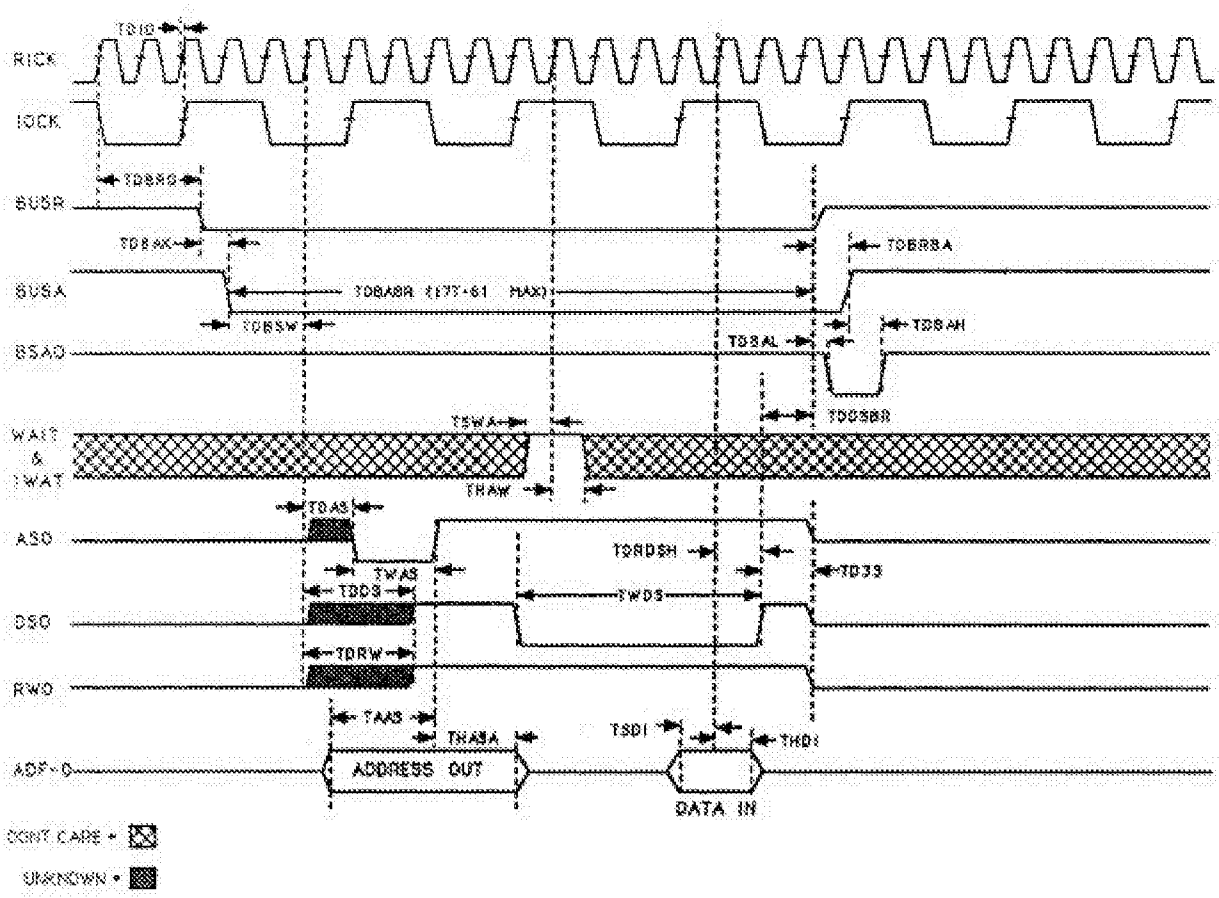
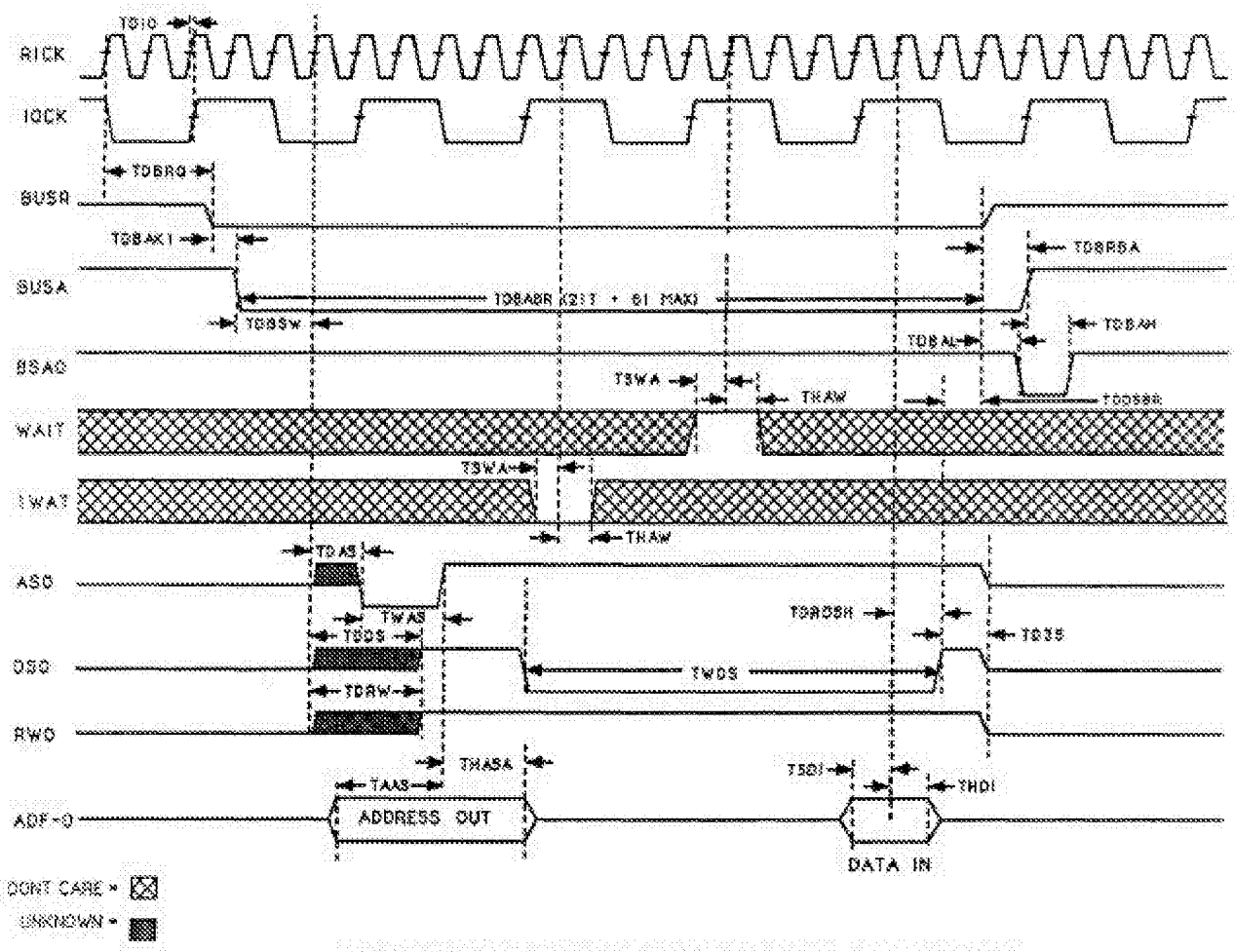


FIGURE 3. Block diagram.



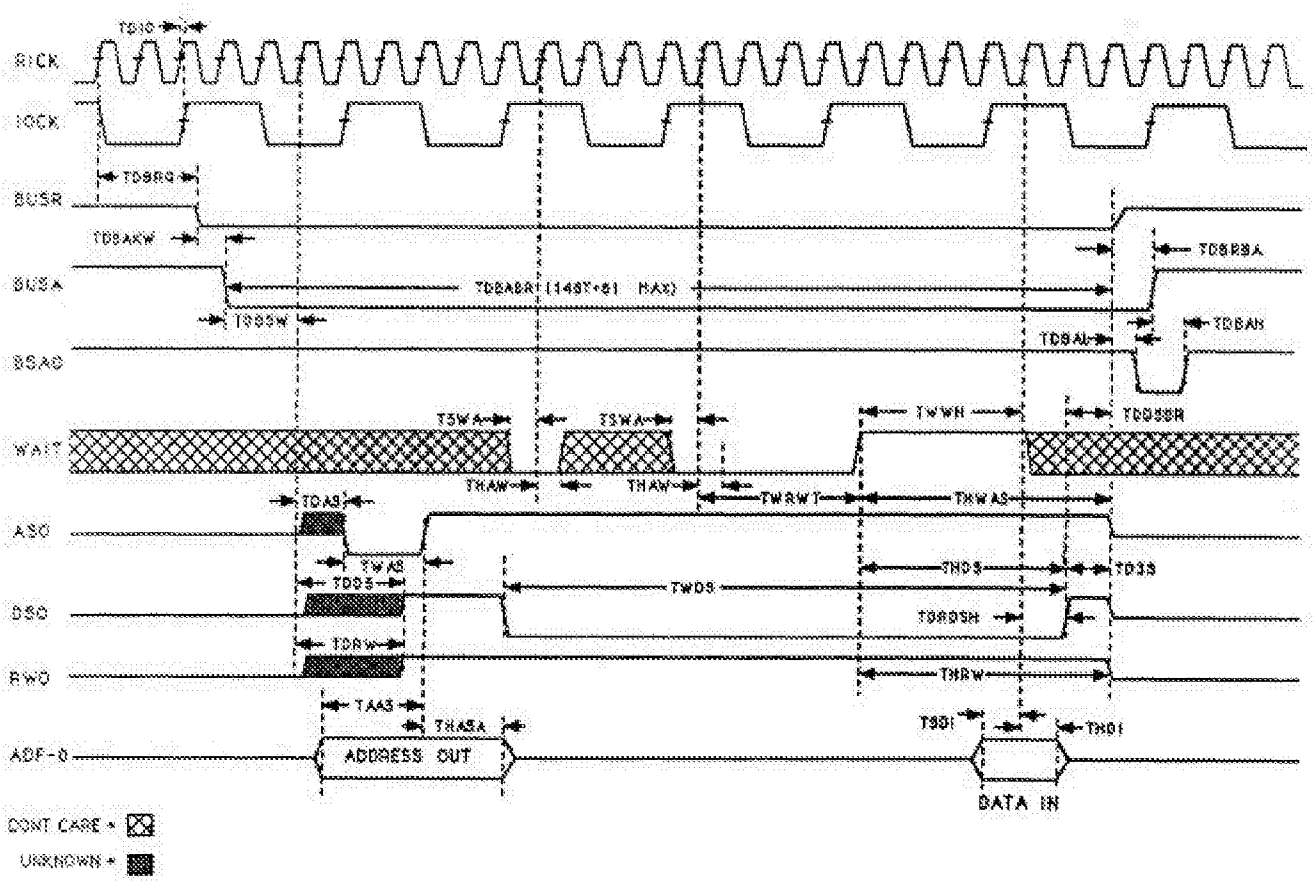
SUBSYSTEM INTERFACE READ CYCLE TIMING - NO WAIT STATES

FIGURE 4. Timing waveforms.



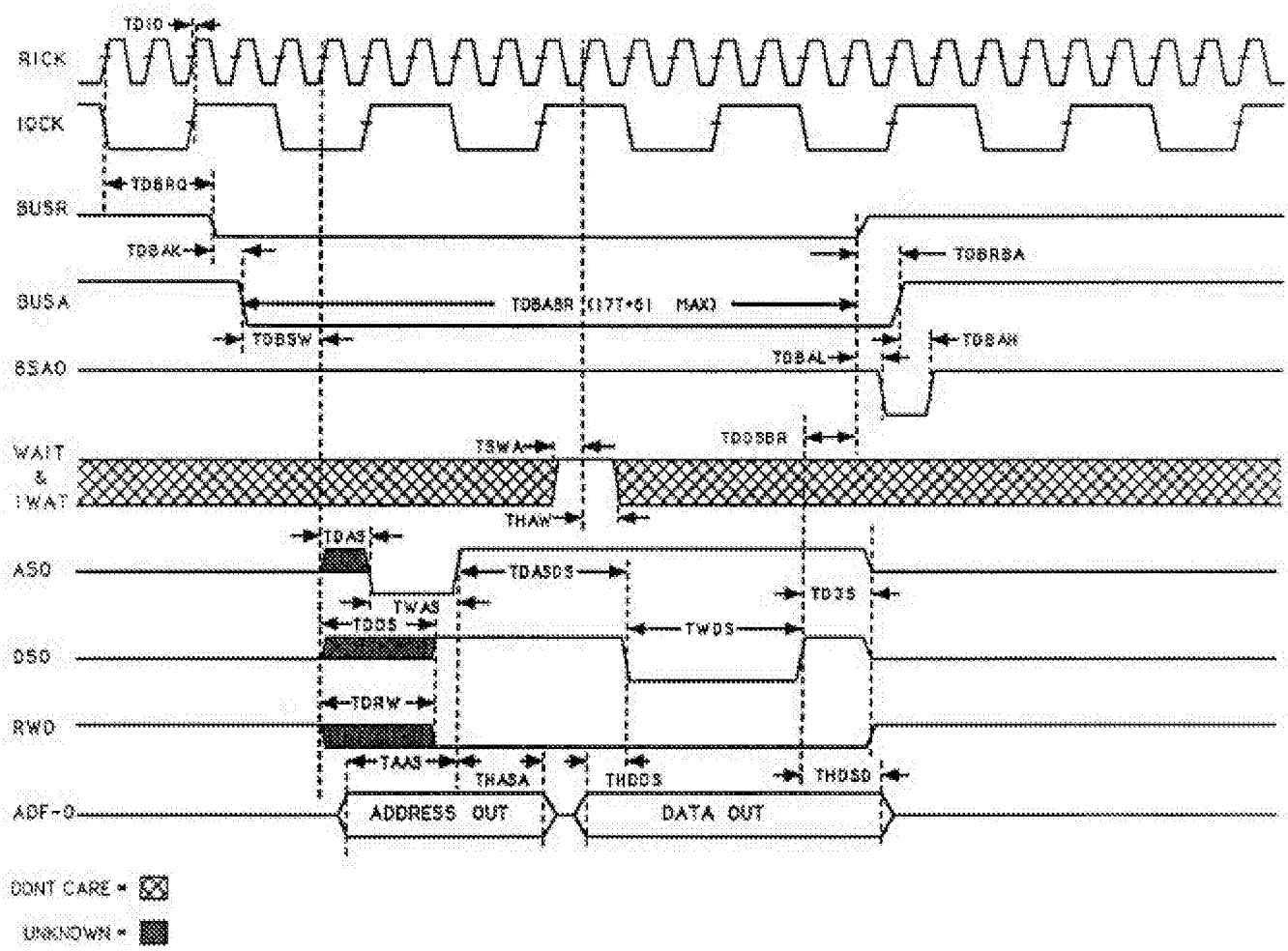
SUBSYSTEM INTERFACE READ CYCLE TIMING - 1 WAIT STATE

FIGURE 4. Timing waveforms - Continued.



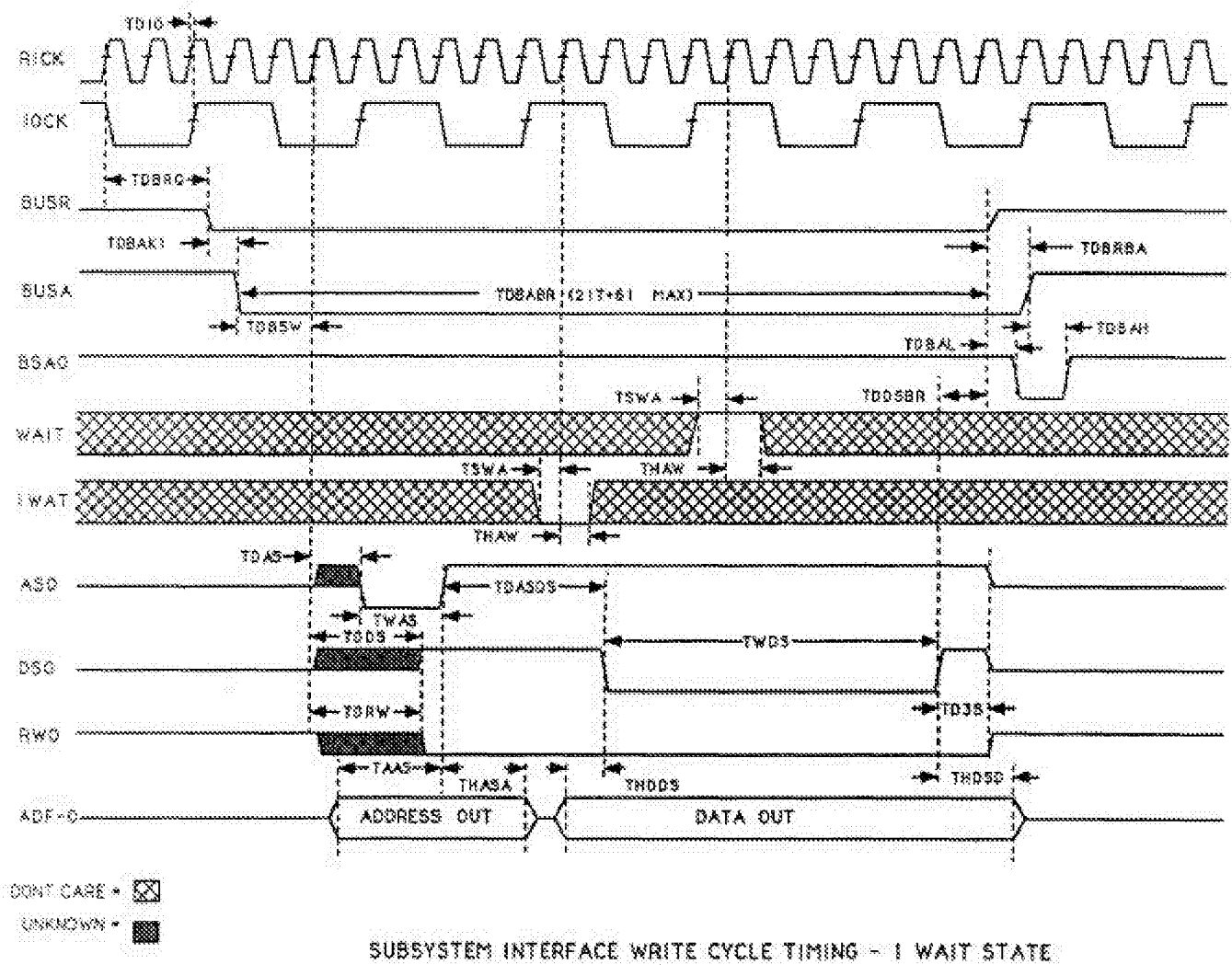
SUBSYSTEM INTERFACE READ CYCLE TIMING - WAIT

FIGURE 4. Timing waveforms - Continued.



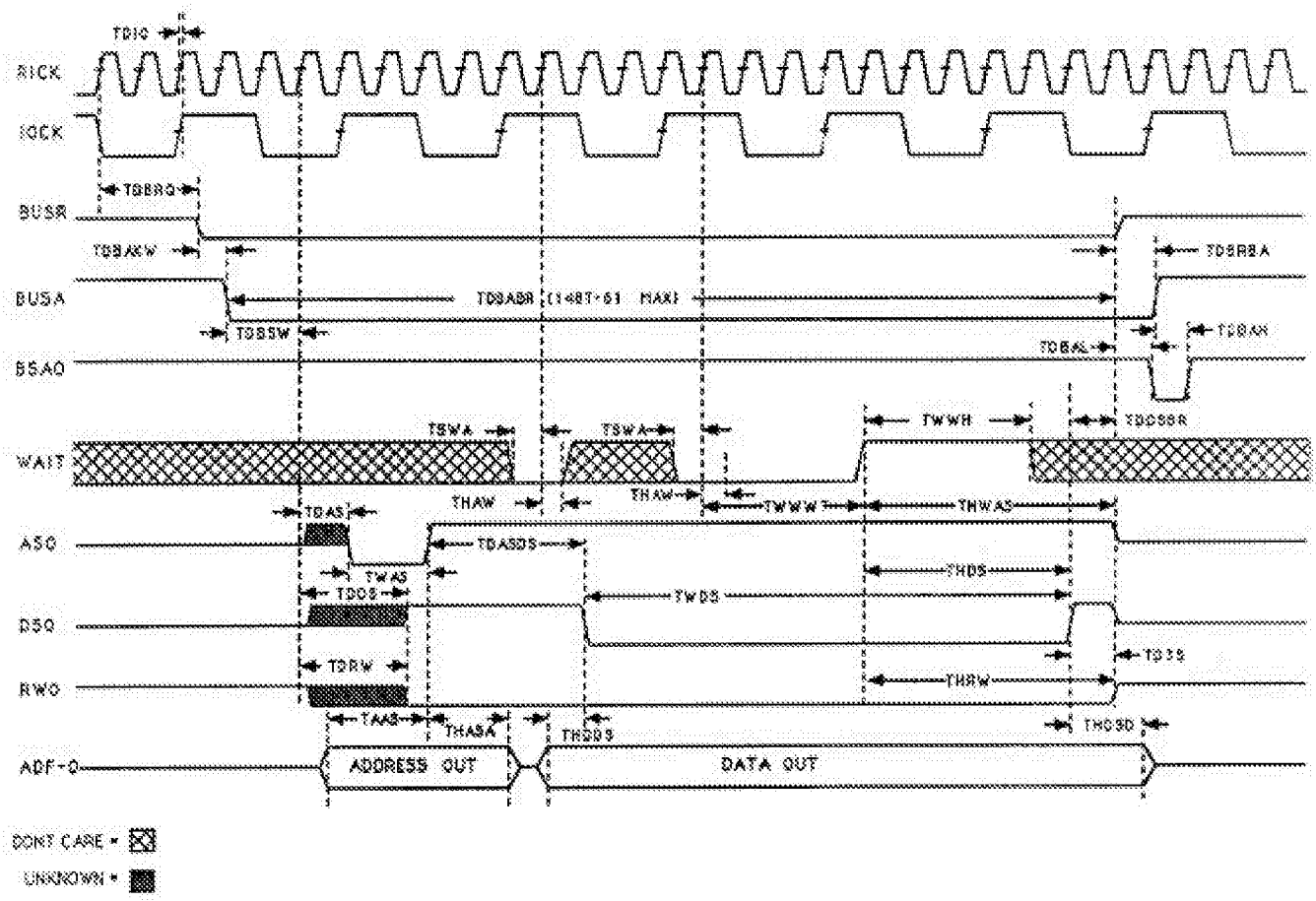
SUBSYSTEM INTERFACE WRITE CYCLE TIMING - NO WAIT STATES

FIGURE 4. Timing waveforms - Continued.



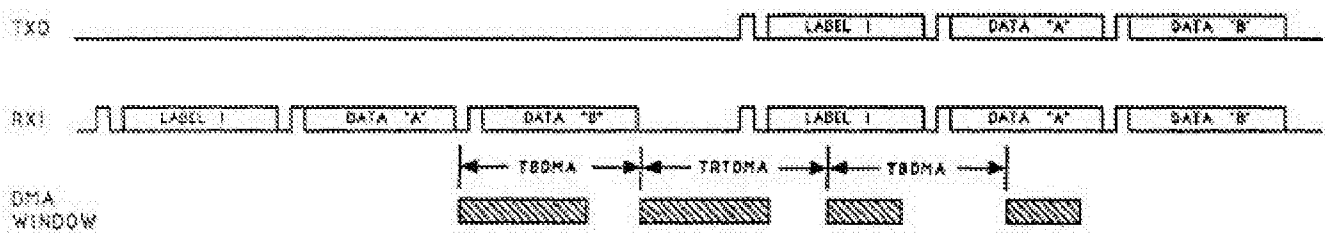
SUBSYSTEM INTERFACE WRITE CYCLE TIMING - 1 WAIT STATE

FIGURE 4. Timing waveforms - Continued.

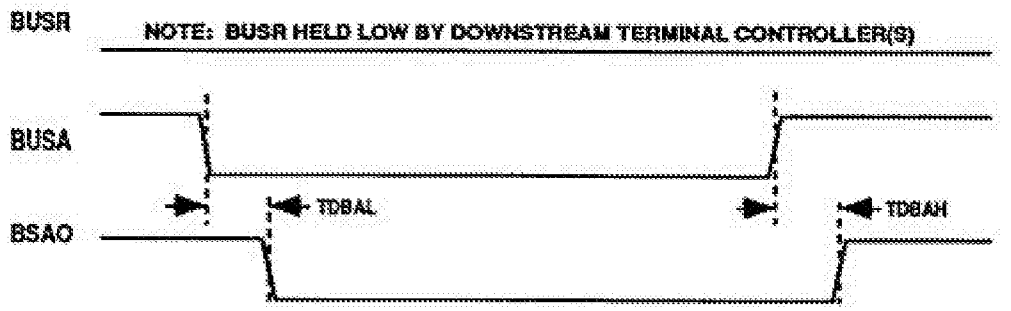


SUBSYSTEM INTERFACE WRITE CYCLE TIMING - WAIT

FIGURE 4. Timing waveforms - Continued.

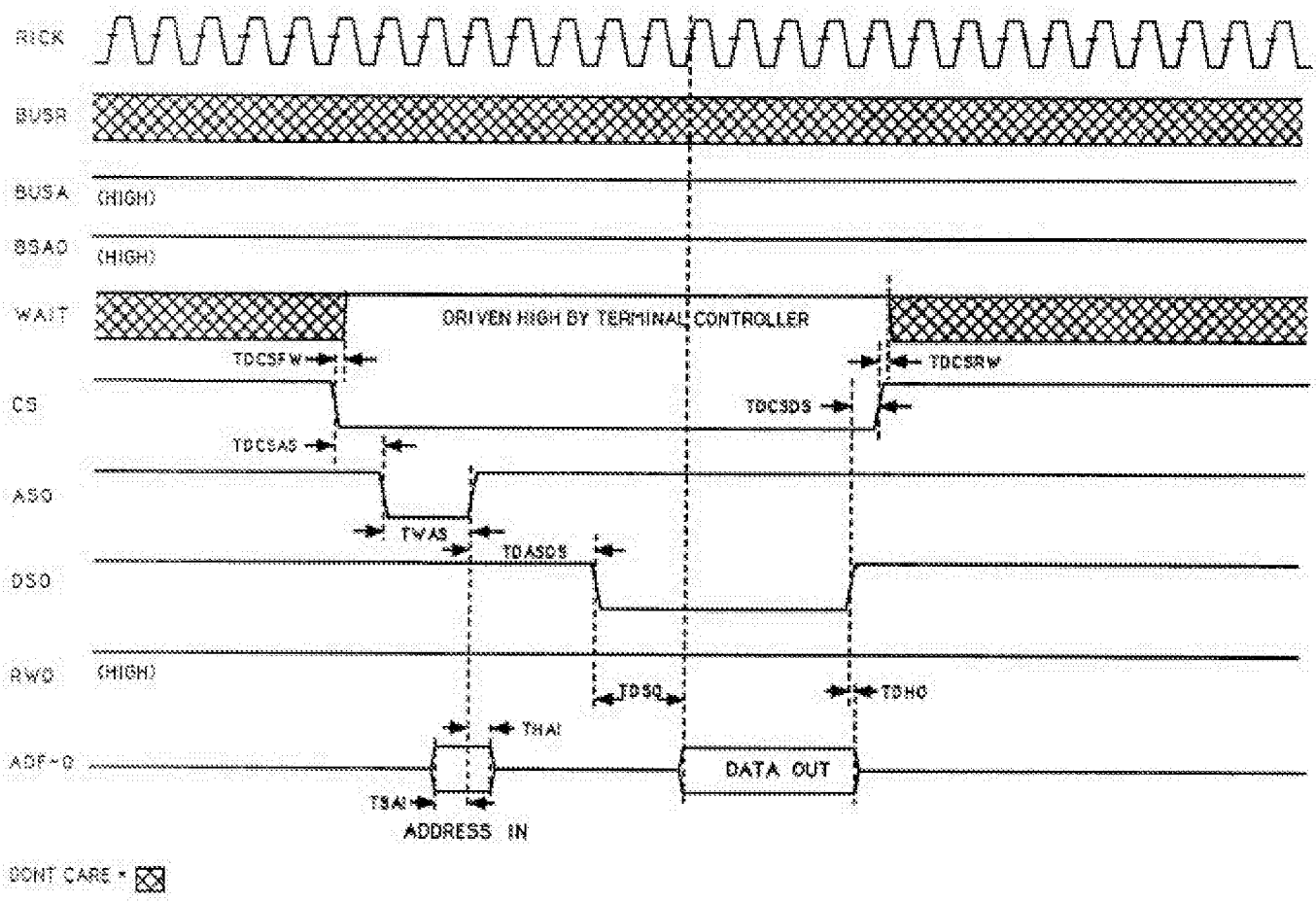


DMA WINDOWS



Bus Acknowledge Out Strobe Throughput Timing

FIGURE 4. Timing waveforms - Continued.



SUBSYSTEM INTERFACE - READ INTERNAL REGISTER CYCLE TIMING

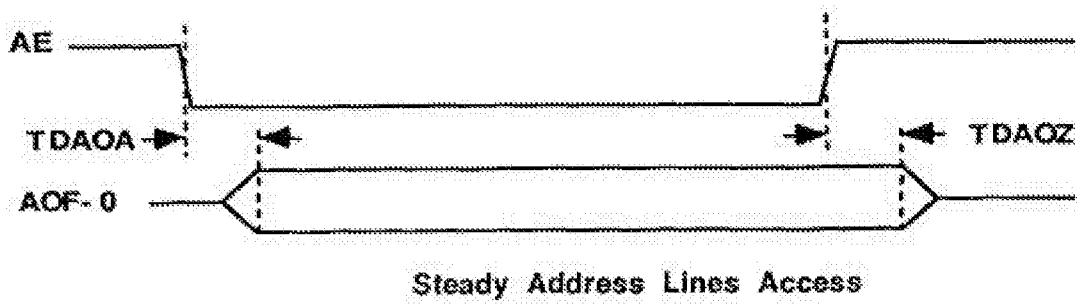
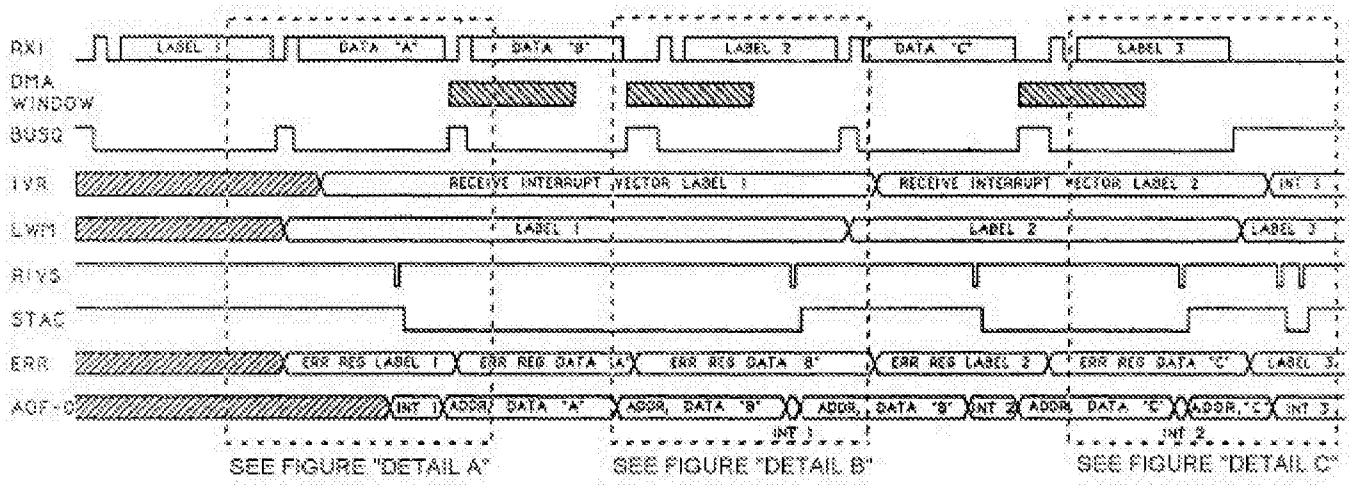
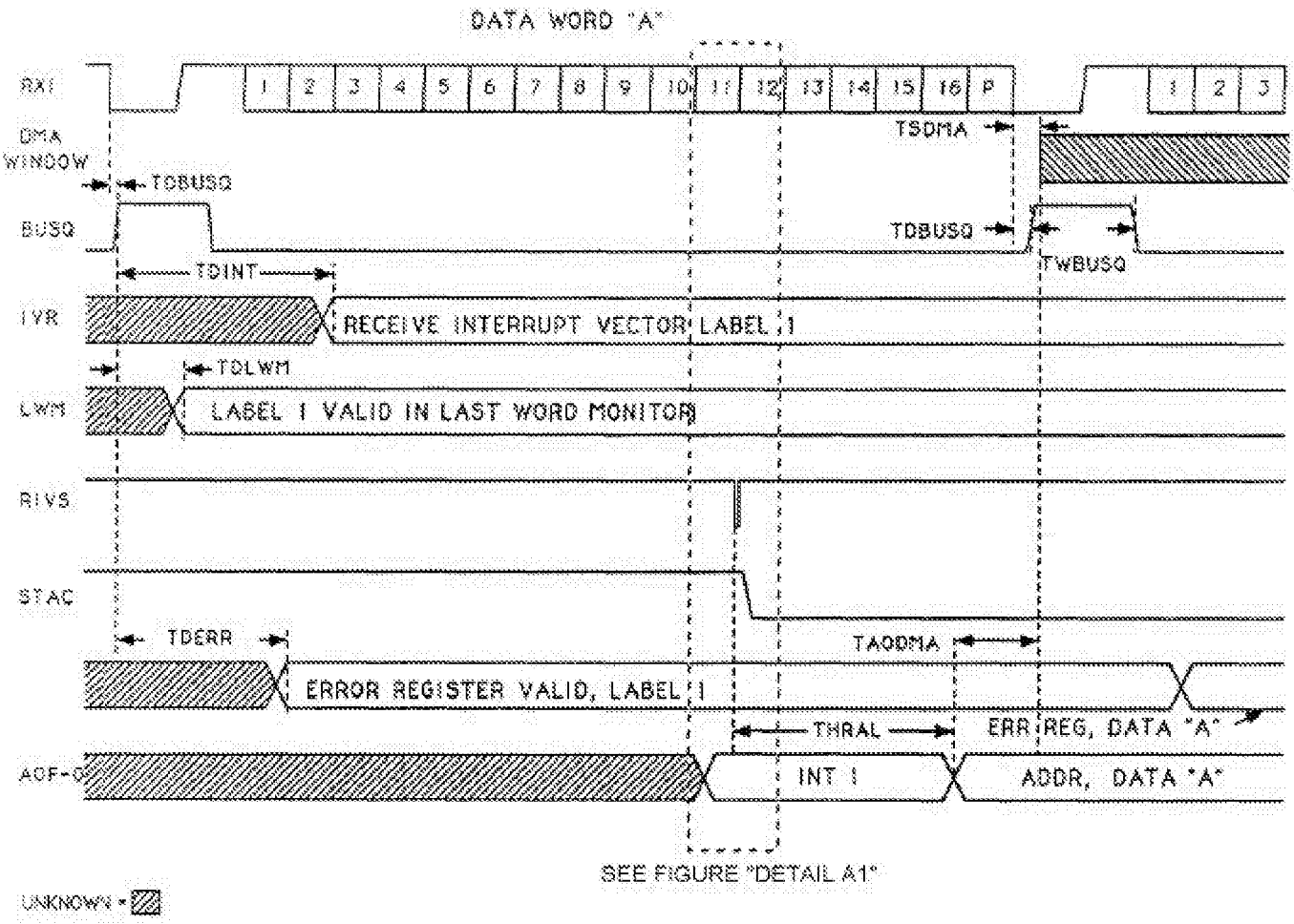


FIGURE 4. Timing waveforms - Continued.



INTERNAL REGISTER TIMING, RECEIVE

FIGURE 4. Timing waveforms - Continued.



INTERNAL REGISTER TIMING, RECEIVE - "DETAIL A"

FIGURE 4. Timing waveforms - Continued.

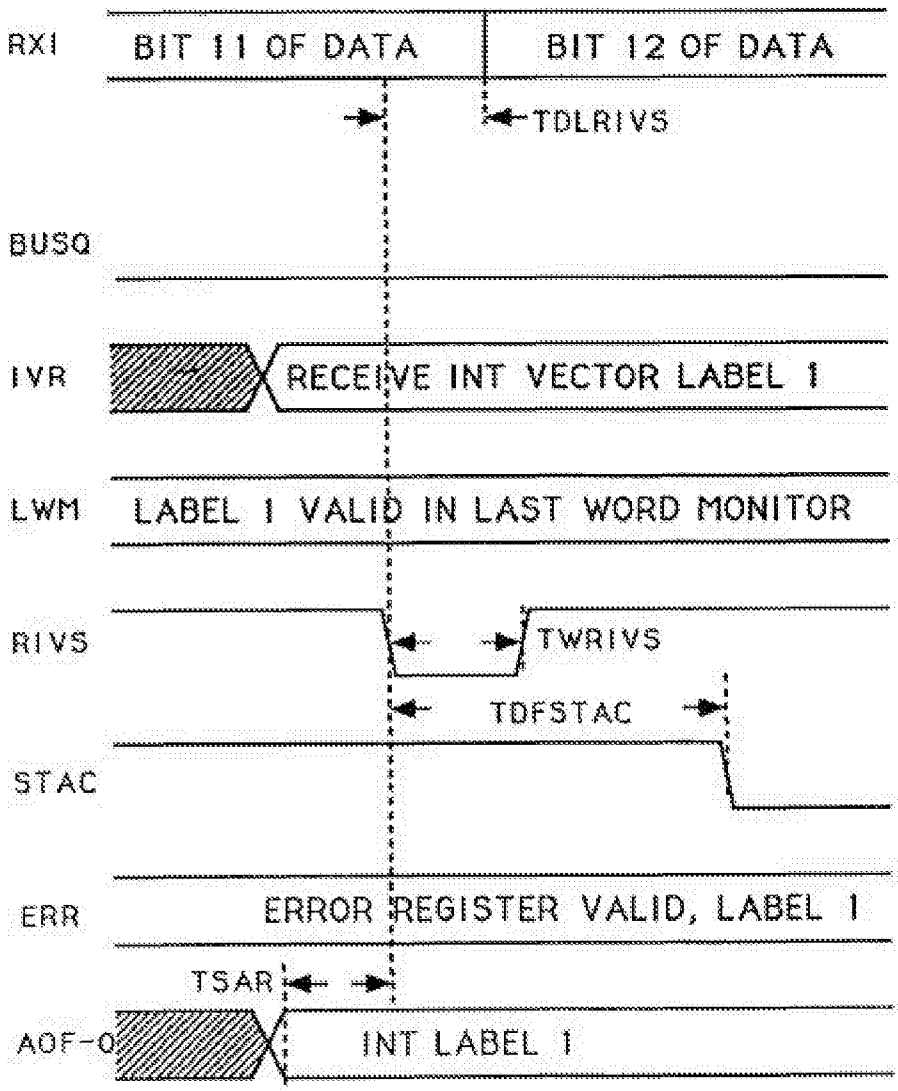
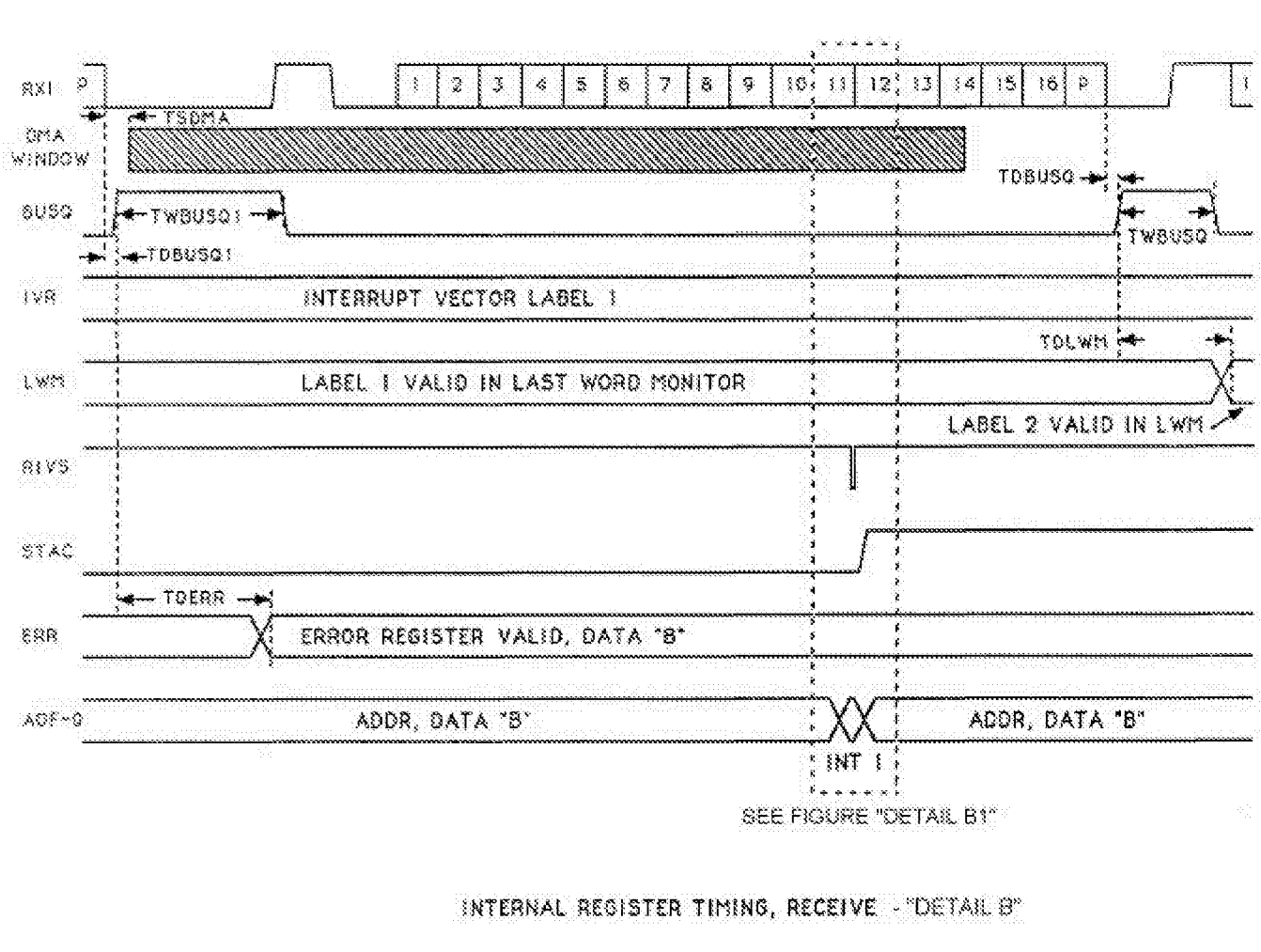


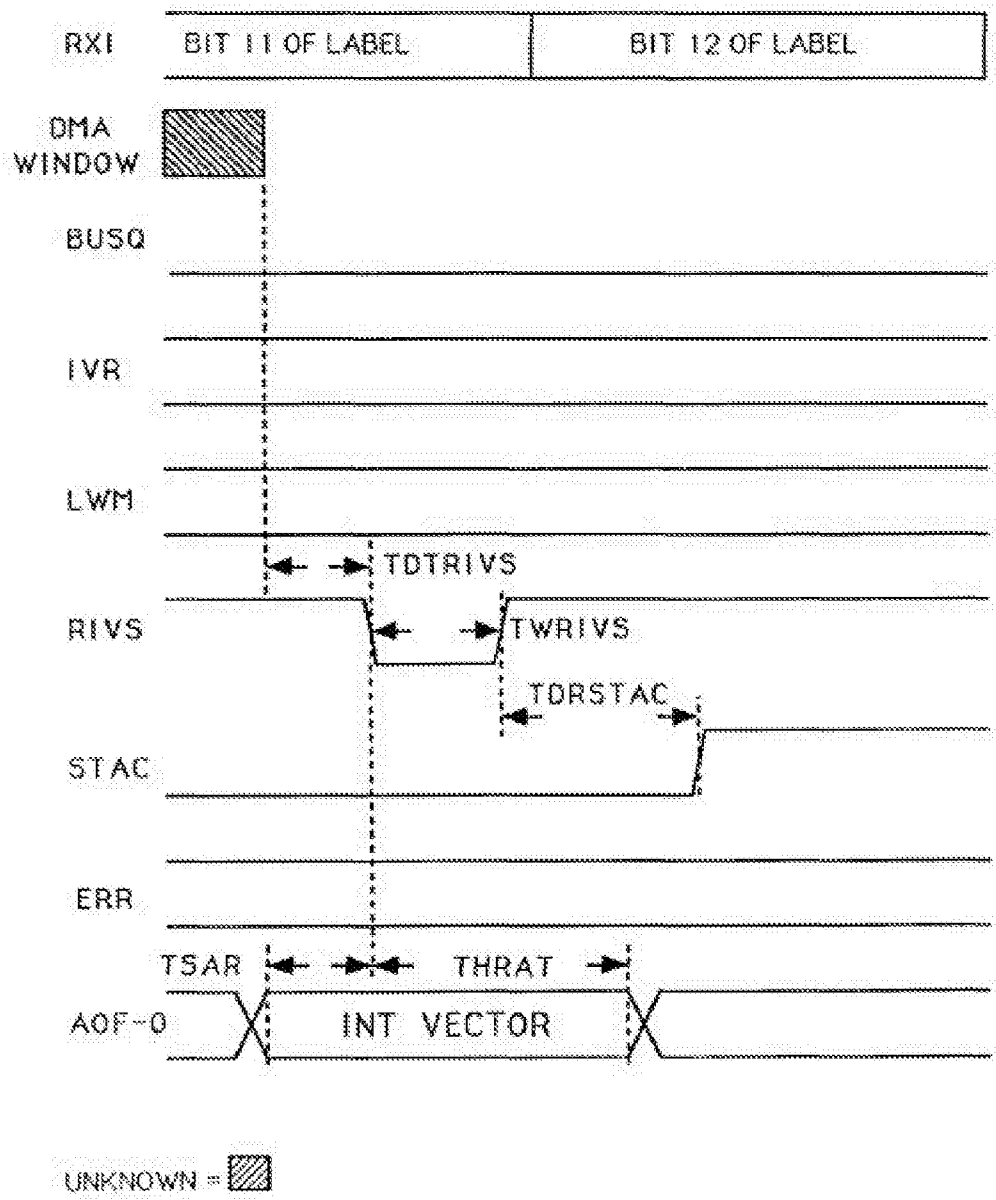
FIGURE 4. Timing waveforms - Continued.



INTERNAL REGISTER TIMING, RECEIVE - "DETAIL B"

FIGURE 4. Timing waveforms - Continued.

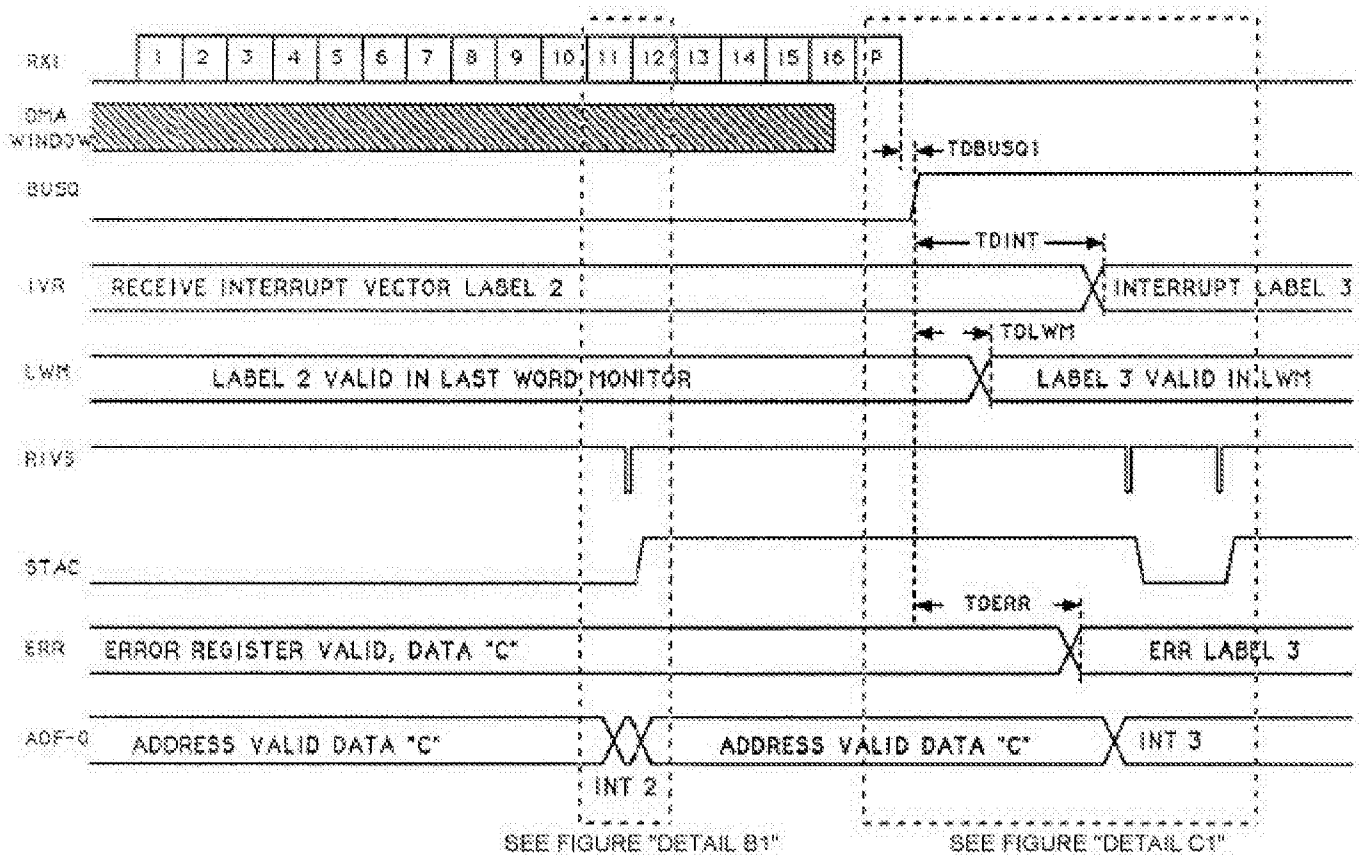
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-99581
		REVISION LEVEL	SHEET 32



TRAILING INTERRUPT/STAC

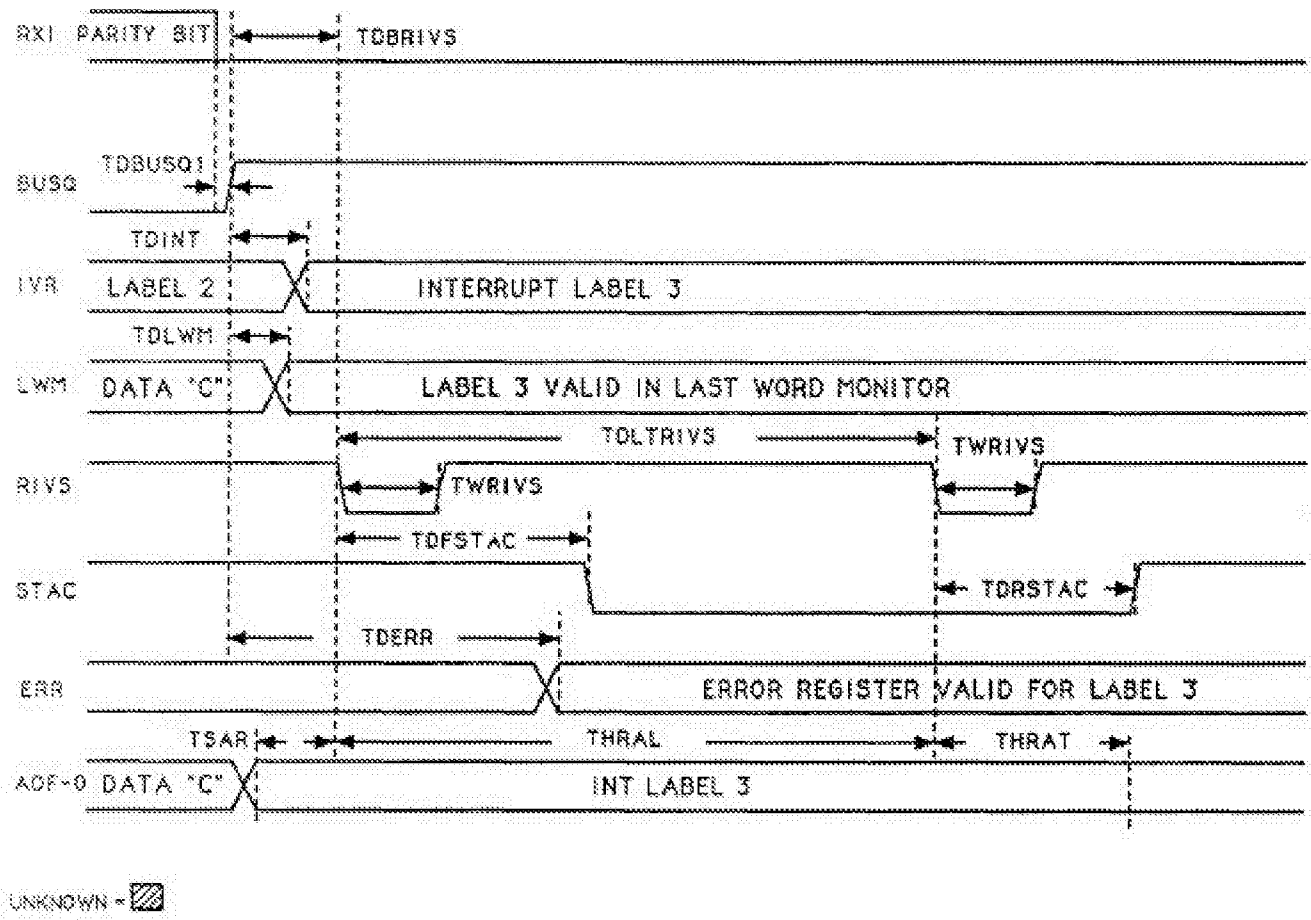
INTERNAL REGISTER TIMING, RECEIVE - "DETAIL B1"

FIGURE 4. Timing waveforms - Continued.



INTERNAL REGISTER TIMING, RECEIVE - "DETAIL C"

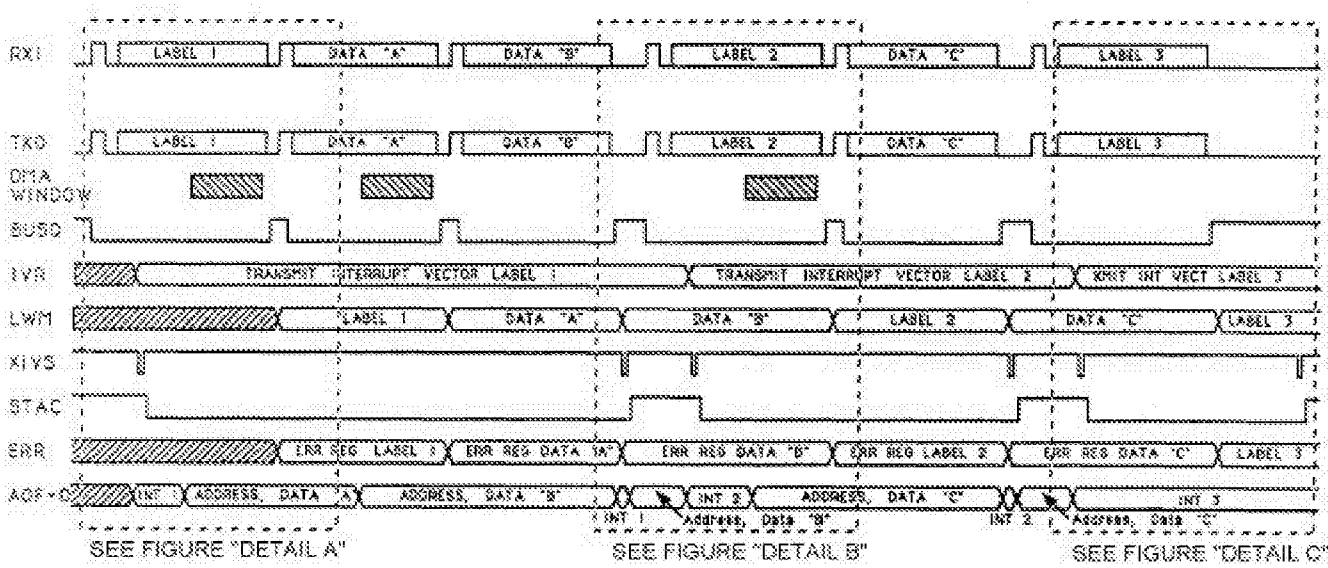
FIGURE 4. Timing waveforms - Continued.



LEADING/TRAILING INTERRUPTS/STAC

INTERNAL REGISTER TIMING, RECEIVE - "DETAIL C1"

FIGURE 4. Timing waveforms - Continued.



INTERNAL REGISTER TIMING, TRANSMIT

FIGURE 4. Timing waveforms - Continued.

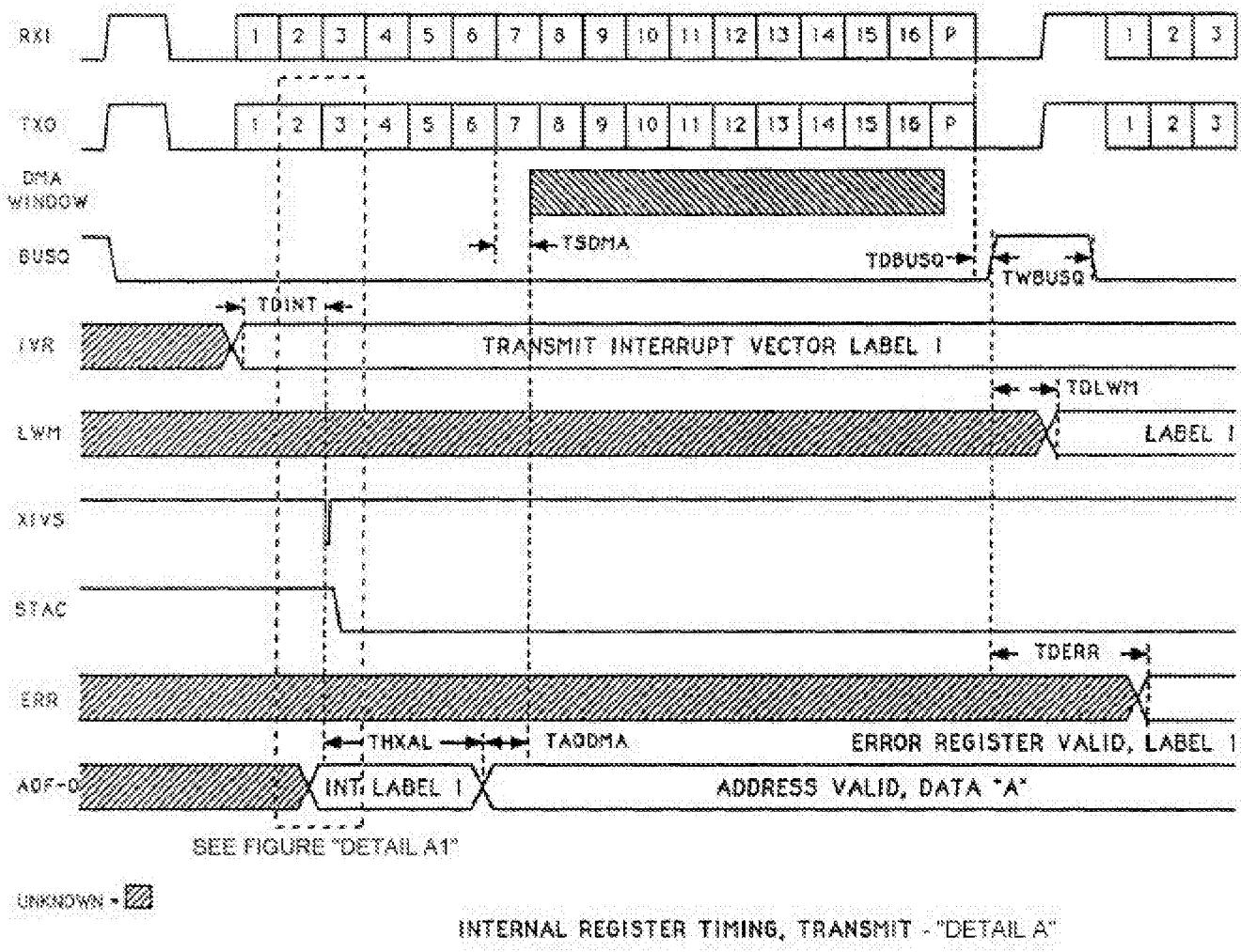
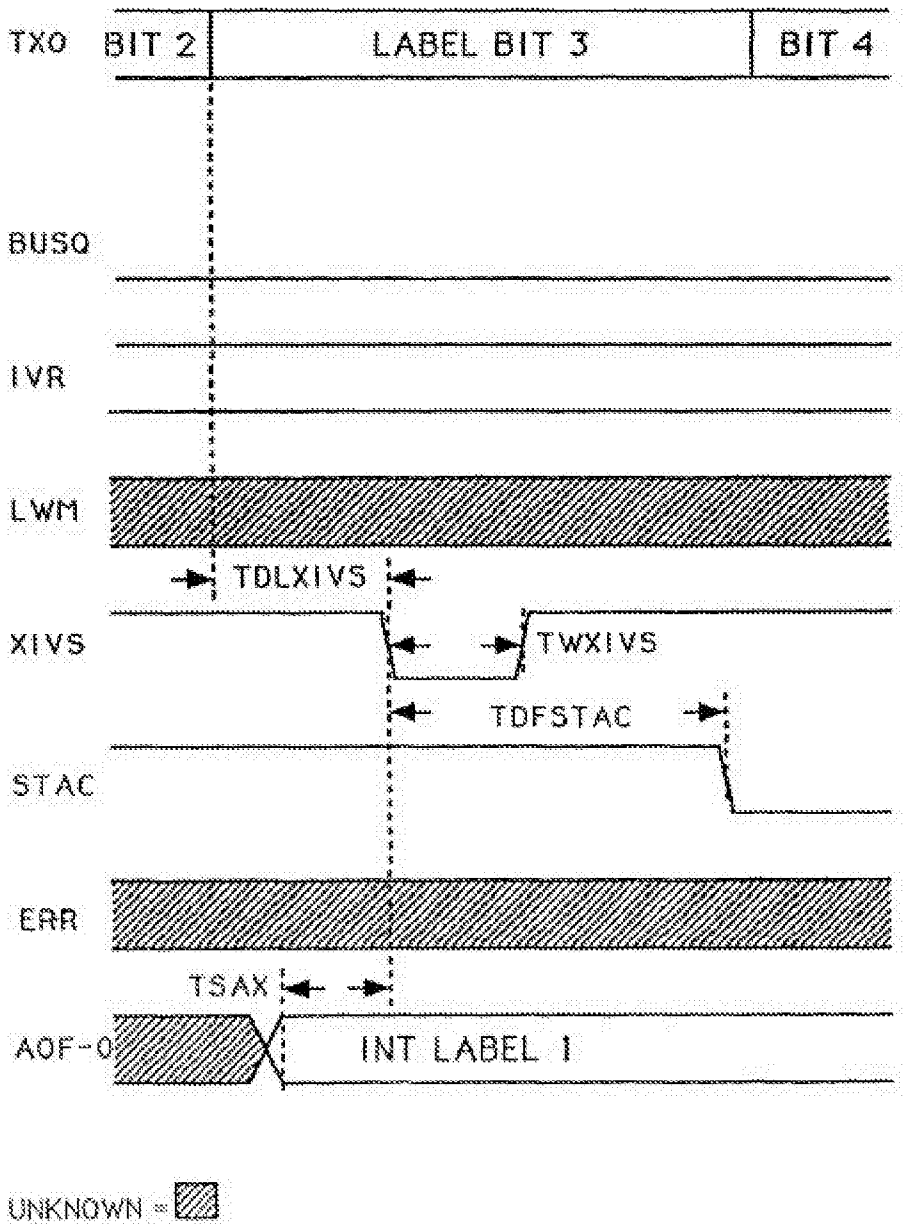


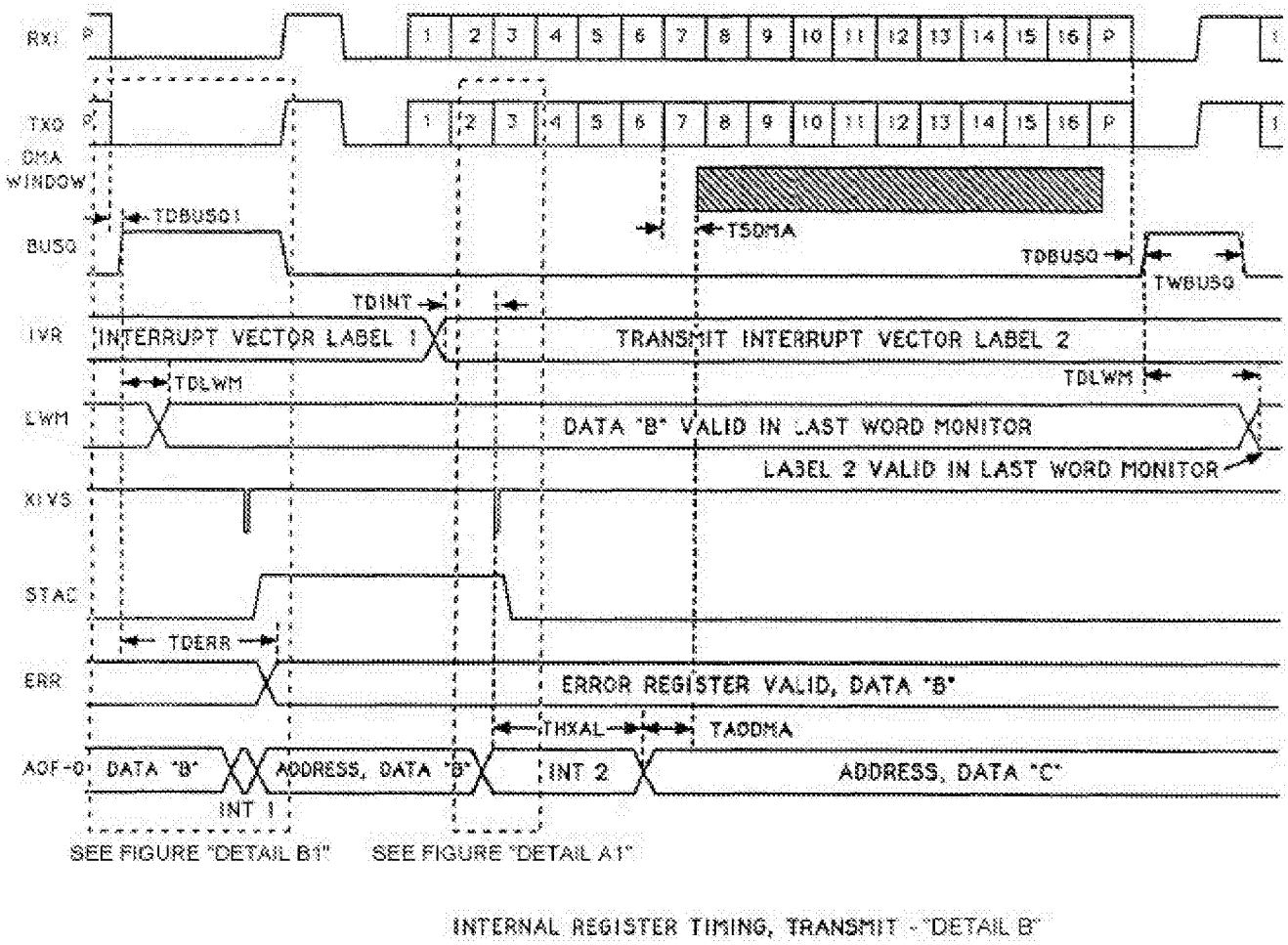
FIGURE 4. Timing waveforms - Continued.



LEADING INTERRUPT/STAC

INTERNAL REGISTER TIMING, TRANSMIT - "DETAIL A1"

FIGURE 4. Timing waveforms - Continued.



INTERNAL REGISTER TIMING, TRANSMIT - "DETAIL B"

FIGURE 4. Timing waveforms - Continued.

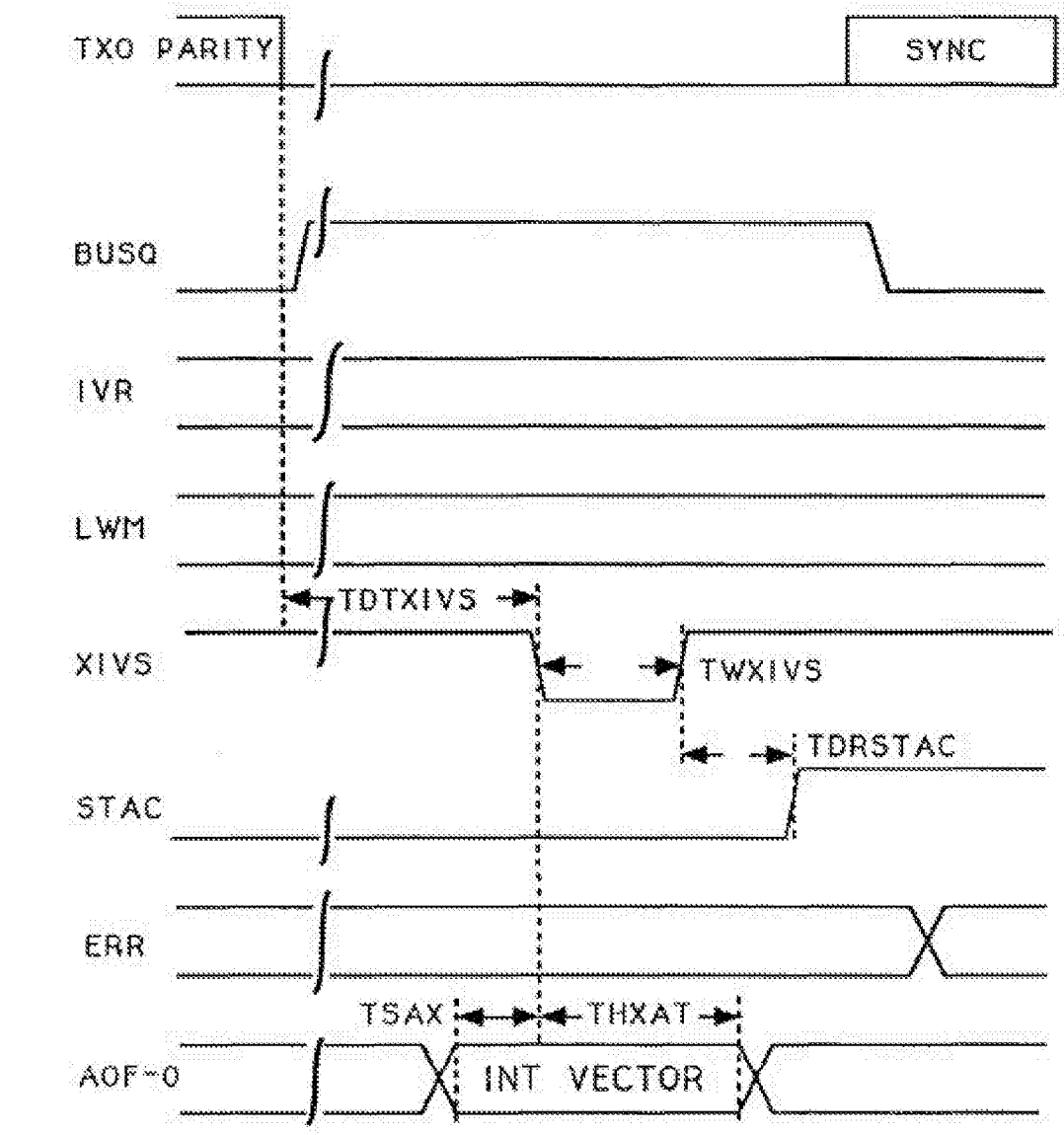
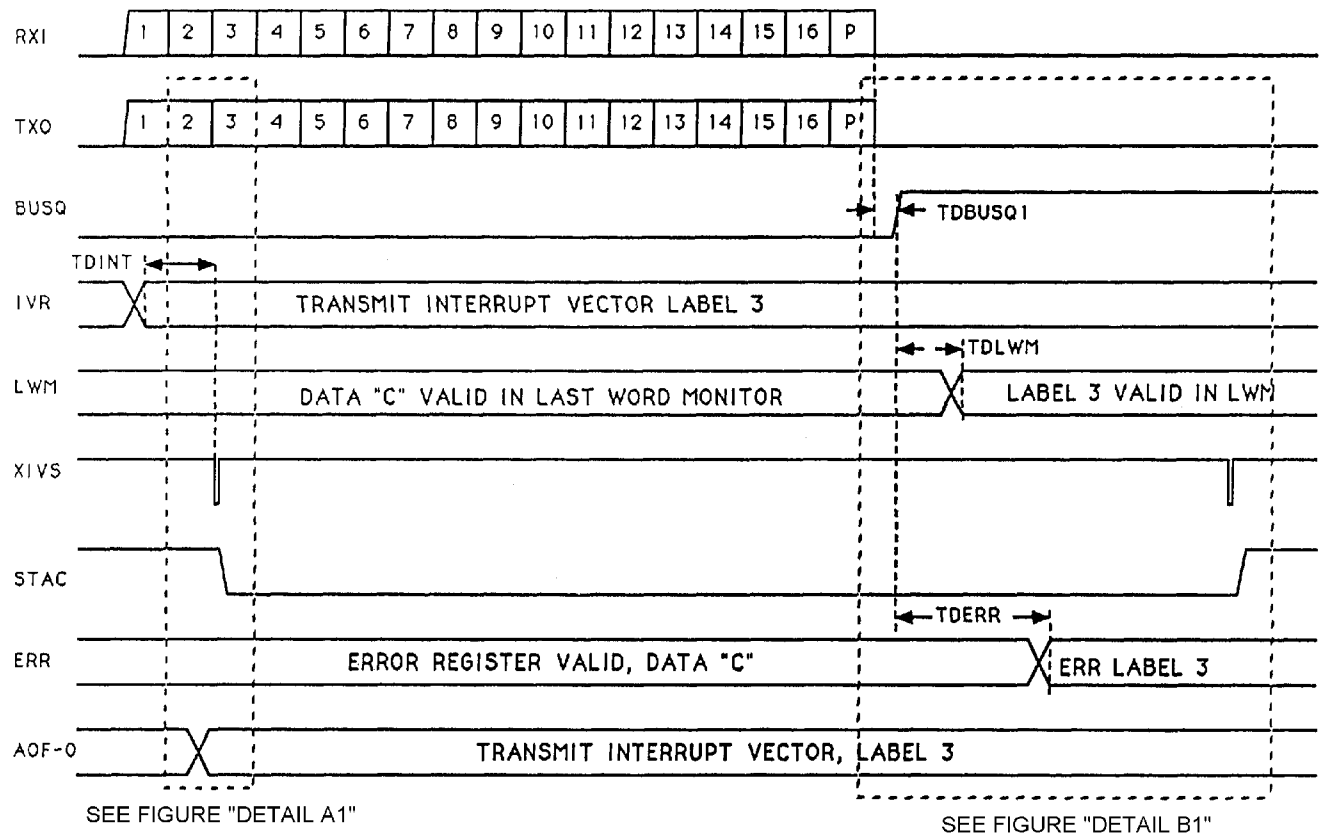
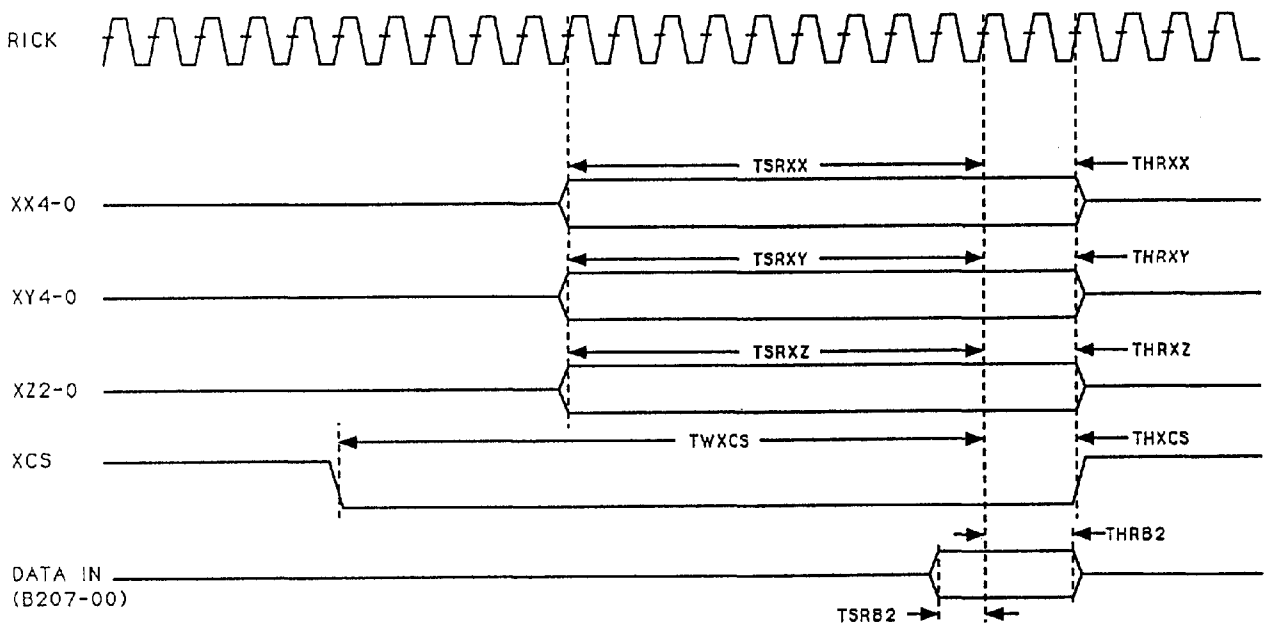


FIGURE 4. Timing waveforms - Continued.

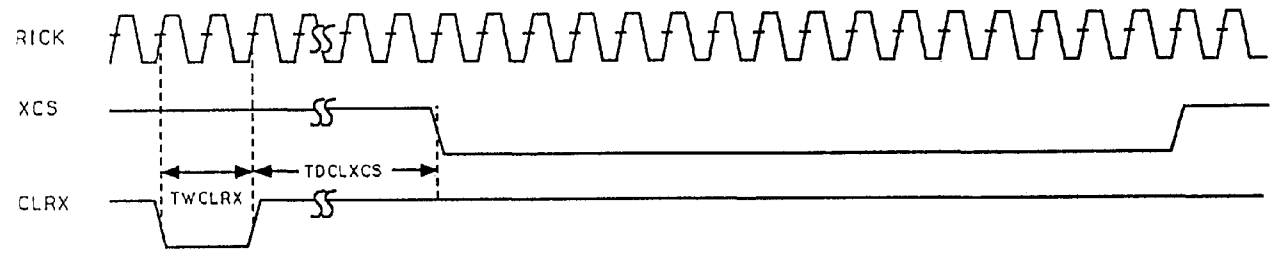


INTERNAL REGISTER TIMING, TRANSMIT - "DETAIL C"

FIGURE 4. Timing waveforms - Continued.



TRANSMIT PERSONALITY PROM READ CYCLE TIMING



XX4-0 ADDRESS LINES ZEROED TIMING

FIGURE 4. Timing waveforms - Continued.

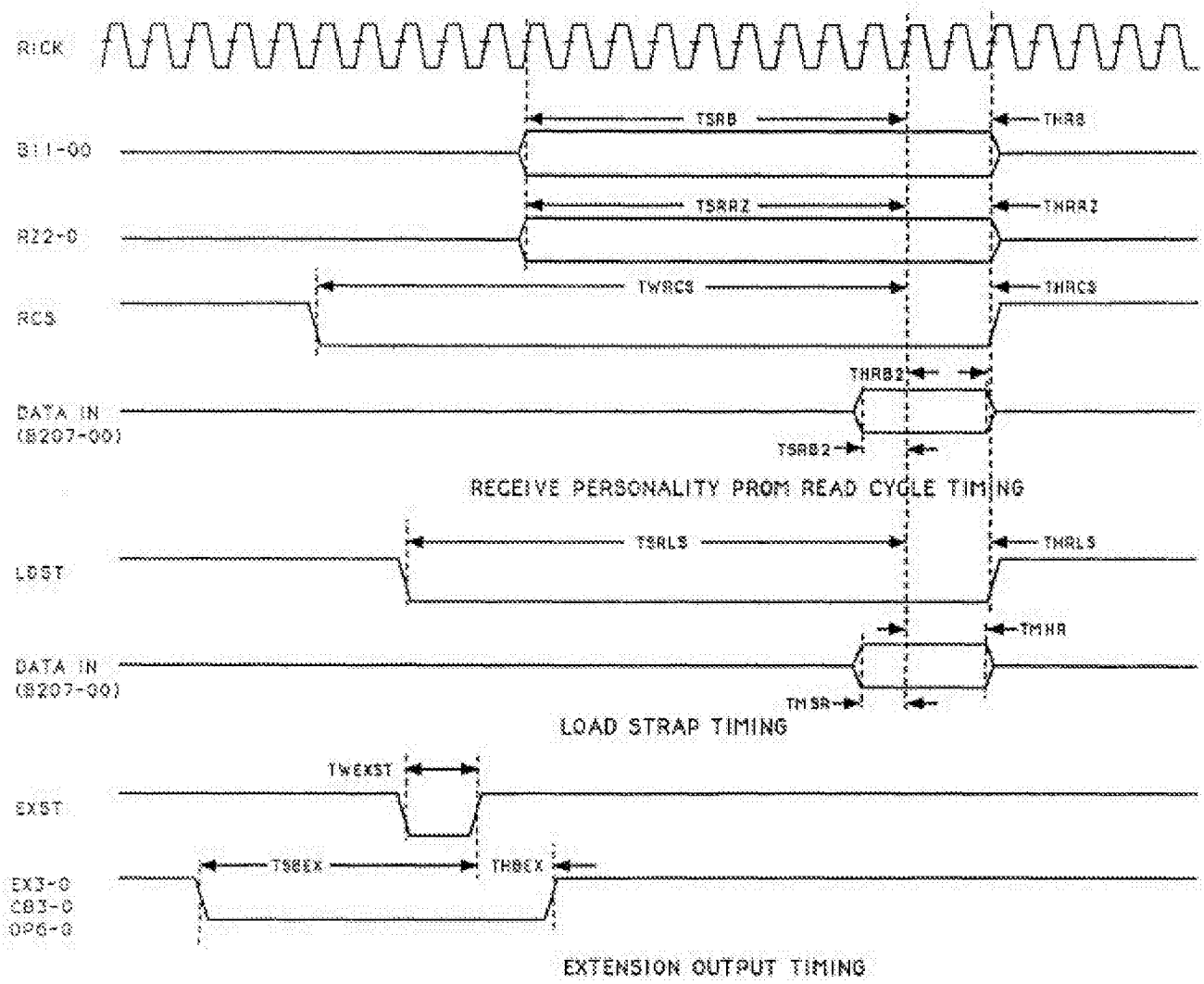
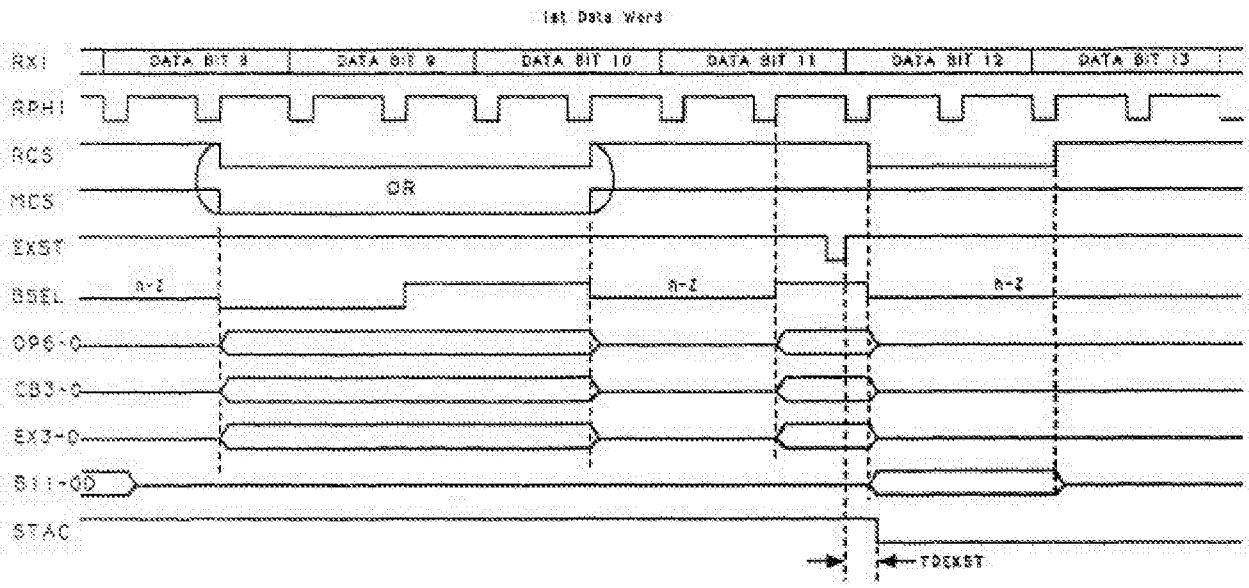
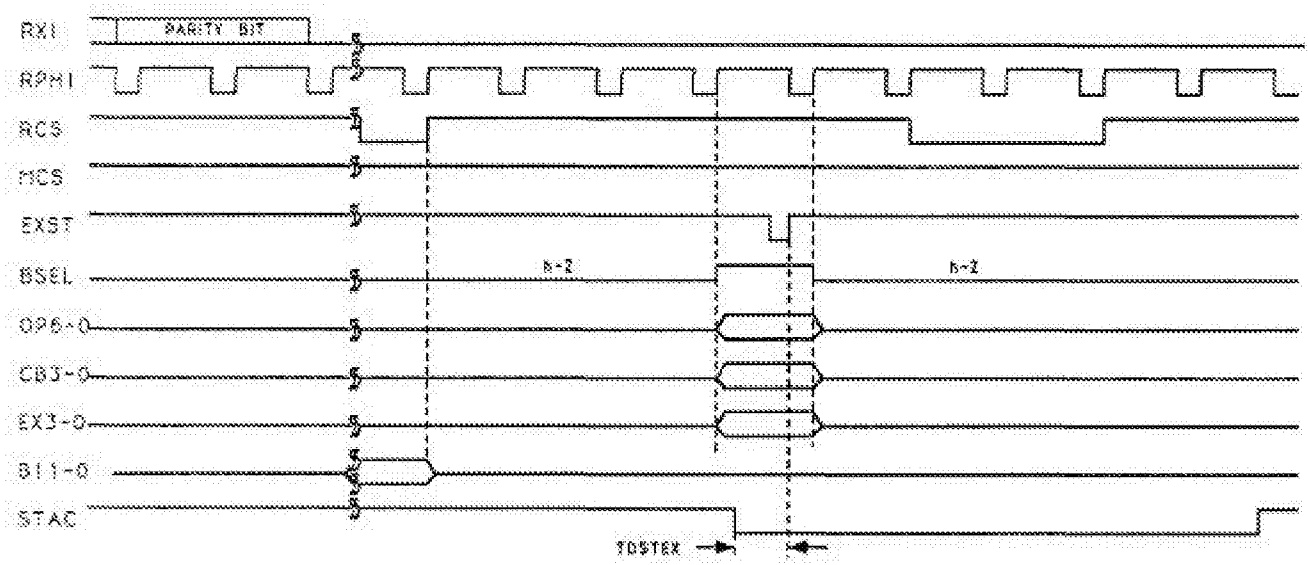


FIGURE 4. Timing waveforms - Continued.



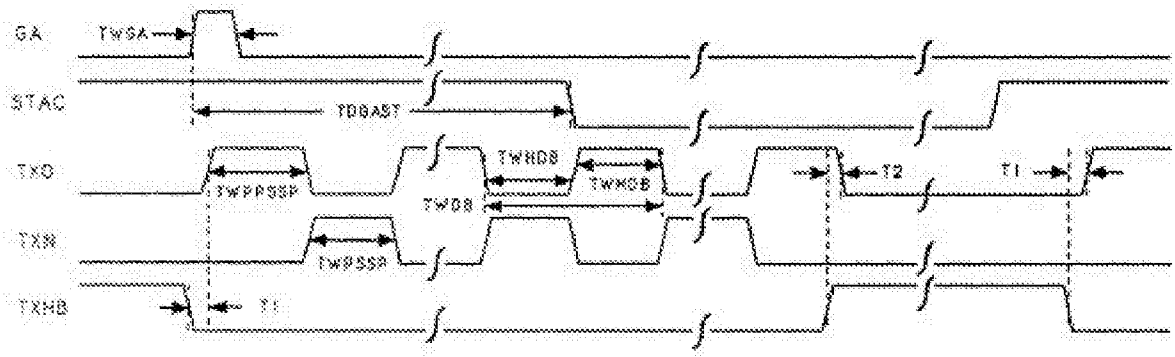
EXST TIMING, WORD STRING WITH DATA

FIGURE 4. Timing waveforms - Continued.

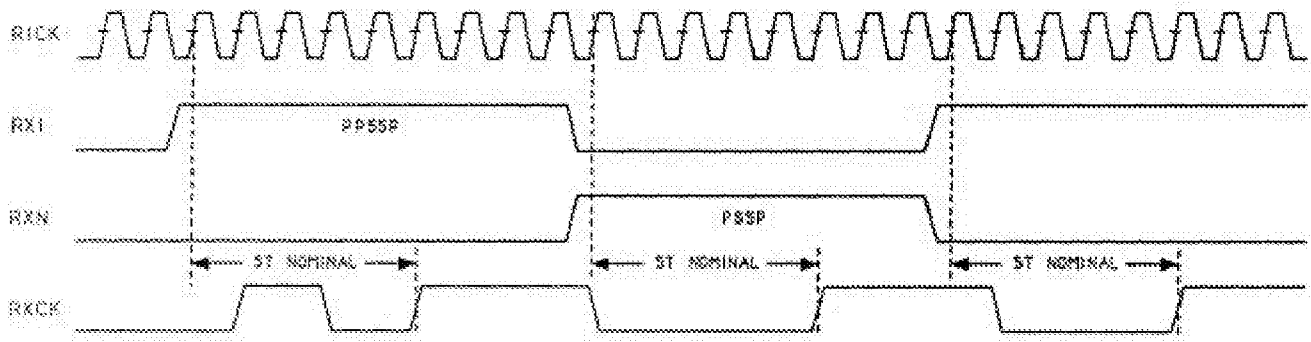


EXST TIMING, LABEL ONLY

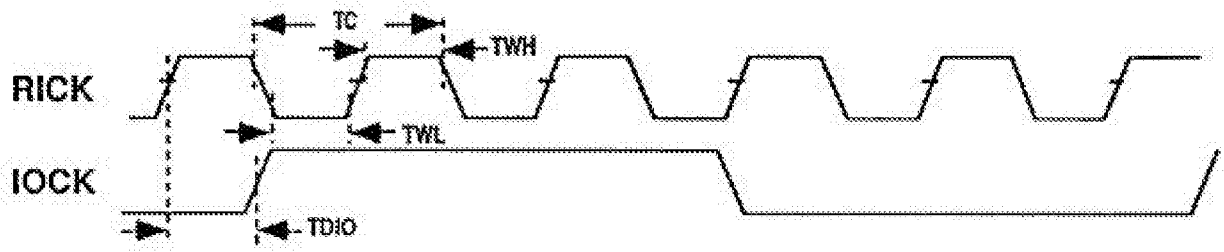
FIGURE 4. Timing waveforms - Continued.



TRANSMIT TIMING



RECEIVE TIMING



XICK/RICK AC Characteristics

FIGURE 4. Timing waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity qualification inspection . Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2	1, 2	1, 2
Group D end-point electrical parameters (see 4.4)	1, 2	1, 2	1, 2
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0674.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as specified herein.

General Input Signals

PWRS - POWER-UP RESET
Initializes Terminal Controller when held low for a minimum of 500 nsec. Low active Schmitt trigger. Mandatory input.

RICK - RECEIVE INPUT CLOCK
Receive/Monitor oscillator input, Schmitt trigger. Nominally 32Mhz @ 2Megabit/Second (Mps). This clock is used for all circuits except the Transmit Protocol Access Module (XPAM). Mandatory input.

XICK - TRANSMIT INPUT CLOCK
Transmit oscillator input, Schmitt trigger. Nominally 32Mhz @ 2Megabit/Second (Mps). This clock is used only for the Transmit Protocol Access Module (XPAM). Mandatory input (may be tied high for Receive-only operation).

Protocol Related Signals

TI6 – TI0 - TRANSMIT INTERVAL
7 bit strap for TI parameter in access protocol. TI = (binary value + 1.001125) X ΔTI msec. TI6 = most significant bit. Internal pull-up resistor. Mandatory input.

$$\Delta TI = \frac{16}{f(CLK)\ (MHz)}$$

TG6 – TG0 - TERMINAL GAP
7 bit strap for TG parameter in access protocol. TG = (3.0+(2 X binary value)) X ΔTG μsec. TG6= most significant bit.
Note: This equation gives the minimum TG value. Internal pull-up resistor. Mandatory input.

$$\Delta TG = \frac{16}{f(CLK)\ (MHz)}$$

SG1, SG0 - SYNC GAP
2 bit strap for SG parameter in access protocol. The 2 bit strap selects one of four SG values. Each SG strap combination and its equivalent TG binary value is shown in the table below.

SG1	SG0	TG BINARY VALUE
0	0	16
0	1	32
1	0	64
1	1	127

SG = (2.75+(2 X TG binary value)) x ΔSG μsec. SG1 = most significant bit.
Note: This equation gives the minimum SG value. Internal pull-up resistor. Mandatory input.
Note: The SG selected must be greater than any TG on the bus.

$$\Delta SG = \frac{16}{f(CLK)\ (MHz)}$$

LDST - LOAD STRAP
Output strobe that indicates the loading protocol monitor with TI, TG and SG parameters. Low active. Optional use output.

CMDP - C-MODE PULSE
Input pulsed low periodically to maintain C-mode operation. Terminal will remain in C-mode if the CMDP interval < 2TI-500 μsec. Low active. Internal pull-up resistor. Mandatory input.

MIFS - MINOR FRAME SYNC
Input which synchronizes timing during C-mode, initiates minor frame message. Low active. Internal pull-up resistor. Mandatory input.

Serial Interface Signals

RXI - RECEIVE INPUT
Receiver serial data input – true (automatic complementation if RXI and RXN reversed). Internal pull-up resistor. Mandatory input.

RXN - RECEIVE NOT
Receiver serial data input – false (automatic complementation if RXI and RXN reversed). Internal pull-up resistor. Mandatory input.

TXO - TRANSMIT OUTPUT
Transmitter serial output – true (receivers complement automatically if TXO and TXN reversed). Mandatory input.

TXN - TRANSMIT NOT
Transmitter serial data output – false (receivers complement automatically if TXO and TXN reversed). Optional use output.

TXHB - TRANSMITTER HIGH IMPEDANCE (ON) BUS
Transmission enable. Low when data is on the bus. May be used to enable line drivers. High active (high = inhibit drivers). Mandatory output.

Personality PROM Interface

B207 – B200 - BUS TWO
Personality EPROM data bus. 8 bits wide. B207 = most significant bit. Internal pull-up resistor. Mandatory input.

B11 – B00 - BUS ONE (BONE)
Personality EPROM address bus. 12 bits wide. B11 = most significant bit. Internal pull-up resistor, tri-state output. Mandatory output.

RZ2 – RZ0 - RECEIVE Z (VECTOR)
Personality EPROM address lines (3 bits). Least significant 3 bits of RPP address. RZ2 = most significant bit. Internal pull-up resistor, tri-state output. Mandatory output.

BSL - BYTE SELECT
Output used in addressing the Multiple Personality PROM (MPP) when employing direct subsystem programming. Internal pull-up resistor, tri-state output. Optional use output.

CID3 – CID0 - CHANNEL IDENTIFICATION
Used as channel identification code (0-15), when multiple versions of the same terminal are on the same bus. Used to address Protocol Access Module (PAM) values. CID3 = most significant bit. Internal pull-up resistor. Mandatory input.

CIDB3 – CIDB0 - CHANNEL ID BUFFERED
Latched outputs of the CIDx inputs. Used to address the MPP. CIDB3 = most significant bit. Internal pull-up resistor, tri-state output. Optional use output.

EX3 – EX0 - EXTENSION
A portion of the address to the MPP, derived from the received label extension. Can also be used as flags. EX3 = most significant bit. Internal pull-up resistor, tri-state output. Optional use output.

OP6 – OP0 - OFFSET POINTER
MPP address outputs, 7 bits. OP6 = most significant bit. Internal pull-up resistor, tri-state output. Optional use output.

XX4 – XX0 - TRANSMIT X (VECTOR)
Most significant portion of the transmit personality PROM (XPP) address lines (5 bits). XX4 = most significant bit. Internal pull-up resistor, tri-state output. Mandatory output.

XY4 – XY0 - TRANSMIT Y (VECTOR)
Part of the XPP address lines (5 bits). XY4 = most significant bit. Internal pull-up resistor, tri-state output. Mandatory output.

XZ2 – XZ0 - TRANSMIT Z (VECTOR)
Least significant portion of the XPP address (3 bits). XZ2 = most significant bit. Internal pull-up resistor, tri-state output. Mandatory output.

MCS - MULTIPLE PERSONALITY CHIP SELECT
MPP output enable. Low active. Internal pull-up resistor, tri-state output. Optional use output.

RCS - RECEIVE CHIP SELECT
Receive/monitor personality EPROM output enable. Low active. Internal pull-up resistor, tri-state output. Mandatory output.

XCS - TRANSMIT CHIP SELECT
Transmit personality EPROM output enable. Low active. Internal pull-up resistor, tri-state output. Mandatory output.

EXST - EXTENSION STROBE
Output strobe from the Terminal Controller to clock OPx, CIDBx, and EXx into external latches. Low active. Optional use output.

Transmit Schedule Related Signals

ALT - ALTERNATE
Enables alternate transmission schedule if such is provided. Low active. Internal pull-up resistor. Mandatory input.

BI - BLOCK/INDEPENDENT
Strap to select transmit schedule format. The figure below illustrates a sample XPP schedule organization and the transmit sequence in both Block and Independent modes.

A	B	C		
D	E			
F				

Transmit Schedule
Labels represented by letters.

Transmit Sequence

BLOCK	INDEPENDENT
ABC	ABC
DE	DEC
F	FBC
ABC ect.	AEC
	DBC
	FEC
	ABC etc.

BI = high block schedule format
BI = low independent schedule format
Internal pull-up resistor. Mandatory input.

MAFS - MAJOR FRAME SYNC
Timing input that overrides transmit schedule sequence for global data schedule synchronization (SYNC MODE). Low active (high for normal operation). Internal pull-up resistor. Mandatory input.

Subsystem Interface

AE - ADDRESS ENABLE
Enables steady address or interrupt vector lines (AOF-AO0). Low active. Internal pull-up resistor. Optional use input.

AOF - AO0 - ADDRESS OUT (16 Bits)
Steady address or interrupt vector lines. AOF is most significant bit. Internal pull-up resistor, tri-state outputs. Optional use output.

ADF – AD0 - ADDRESS/DATA (16 Bits)
Multiplexed address/bi-directional data lines (Z-BUS). ADF is most significant bit, tri-state I/O. Mandatory input/output.

BUSR - BUS REQUEST
Bus request is asserted low when the Terminal Controller requires memory access. Low active, bi-directional. Optional use input/output.

BUSA - BUS ACKNOWLEDGE
Subsystem input response to BUSR from Terminal Controller. Must occur within 32 IOCK clock cycles for read sequence, 72 IOCK clock cycles for write sequence to avoid data loss. Low active. Internal pull-up resistor. Mandatory input.

BSAO - BUS ACKNOWLEDGE OUT
Handshake provided to subsystem subsequent to completion of memory access. Facilitates parallel access arbitration. BUSA is wired to BSAO of higher priority terminal. Low active. Optional use output.

ASO - ADDRESS STROBE OUT
Normally used as an output to indicate a valid subsystem address is present on the ADxx lines. Also used as an input to latch a valid internal register address. Low active, tri-state I/O. Mandatory input/output.

DSO - DATA STROBE OUT
Normally used as an output to strobe data in and out of the Terminal Controller. Also used as an input to access and strobe data from the internal registers. Low active, tri-state I/O. Mandatory input/output.

WAIT - WAIT
Setting WAIT low stretches out data transfer portion of Terminal controller read or write cycle until WAIT is set high. In addition, Terminal Controller drives WAIT high during internal register access. Low active, tri-state I/O. Mandatory input/output.

1WAT - ONE WAIT
Setting 1WAT low permanently stretches data transfer portion of Terminal Controller read or write cycles by one wait cycle (1 IOCK period). Low active. Internal pull-up resistor. Mandatory input.

IOCK - INPUT/OUTPUT CLOCK
Convenience clock signal for synchronization of subsystem interface handshake operations. This clock is RICK/4. Square wave (8Mhz @ 2Mps). IOCK is high during PWRS low. Optional use output.

CS - CHIP SELECT
Input used in conjunction with ASO, DSO, RWO, AD1 And AD0 to enable access to the Terminal Controller internal registers. Low active. Internal pull-up resistor. Optional use input.

ROCK - RECEIVE OUT CLOCK, BUFFERED
Convenience clock signal for operation of subsystem interface circuits. Square wave (32Mhz @ 2Mps). Optional use output.

RWO - READ/WRITE OUTPUT
Indicates data direction on ADxx lines. Read indicated by logic "1", Write by logic "0". Tri-state I/O. Mandatory input/output.

RIVS - RECEIVE INTERRUPT VECTOR STROBE
Low active pulse that indicates the presence of the interrupt vector on the AOxx lines (15 bit vector AOE-AO0, error bit AOF). Optional use output.

XIVS - TRANSMIT INTERRUPT VECTOR STROBE
Low active pulse that indicates the presence of the interrupt vector on the AOxx lines (15 bit vector AOE-AO0, error bit AOF). Optional use output.

Error Information

RERF - RECEIVE ERROR FLAG
Indicates that a receive error has occurred. Low = error. Optional use output.

TXE - TRANSMITTER ENABLE
Indicates transmitter is operational (transmit error counter is not full). High = normal operation. Low = permanent transmitter shutdown until PWRS. Mandatory output.

XERF - TRANSMIT ERROR FLAG
Soft transmit inhibit. Indicates error has occurred. Truncates word string and message string if monitor detects a transmit error. Low = inhibit. Optional use output.

Test Signals

ENC0 - TEST INPUT
For test only. For normal operation ENC4-ENC0 = high. Internal pull-up resistor. Mandatory input.

ENC1 - TEST INPUT
For test only. For normal operation ENC4-ENC0 = high. Internal pull-up resistor. Mandatory input.

ENC2 - TEST INPUT
For test only. For normal operation ENC4-ENC0 = high. Internal pull-up resistor. Mandatory input.

ENC4 - TEST INPUT
For test only. For normal operation ENC4-ENC0 = high. Internal pull-up resistor. Mandatory input.

GA - GO AHEAD
When issued, gives transmitter go ahead to begin transmission of new message. High active. Optional use output.

Optional Use Outputs - Normal Operation Only

CLRX - CLEAR-X-COUNTER
Indicates when the transmit scheduler x-counter is cleared prior to assembly of next message label. Can be used to determine timing to page XPP memory. Low active. Optional use output, multiplexed with XCT0.

STAC - STRING ACTIVE
Indicates that the Terminal Controller is actively engaged in transferring a string to or from the subsystem. Low active. Optional use output, multiplexed with XCT1.

BUSQ - BUS QUIET
Indicates that the global bus is quiet, including interstring gaps. High active. Optional use output, multiplexed with XCT2.

IXTR - I TRANSMIT
Test/Monitor signal. Internally used to indicate to the monitor circuits that the Terminal Controller transmitter is active. Low active. Optional use output, multiplexed with XCT3.

RXCK - RECEIVE/TRANSMIT CLOCK
Internal receive clock phase locked to incoming transmissions. Square wave, nominally 4Mhz @ 2Mps, 50% duty cycle. Mandatory output, multiplexed with XCT4.

XPH1 - TRANSMIT PHASE 1 CLOCK
Used internally to clock the transmit scheduler state machine. Nominally 4Mhz @ 2Mps, 75% duty cycle. Optional use output, multiplexed with XCT5.

RPH1 - RECEIVE PHASE 1 CLOCK
Used internally to clock the receive scheduler state machine. Nominally 4Mhz @ 2Mps, 75% duty cycle. Optional use output, multiplexed with XCT6.

CMD - C-MODE
Indicates that the Terminal Controller is operating in C-mode. Low active. Optional use output, multiplexed with XCT7.

RCT7 – RCT0 - RECEIVE SCHEDULER STATE MACHINE COUNTER (RPKR)
Output of the RPKR value. RCT7 = most significant bit. Optional use output.

Optional Use Outputs - Available Only In Test Mode (ENC0, ENC1, ENC2, and ENC4 =0)

XCT7 – XCT0 - TRANSMIT SCHEDULER STATE MACHINE COUNTER (XPKR)
When the ENCx pins are all grounded, the XPKR is present on CLRX, STAC, BUSQ, IXTR, RXCK, XPH1 and CMD pins. The XPKR is for test purposes only. XCT7 = most significant bit, optional use output. The following is a list of the multiplexed signals on which the XPKR is presented when in test mode:

CMD = XCT7
RPH1 = XCT6
XPH1 = XCT5
RXCK = XCT4
IXTR = XCT3
BUSQ = XCT2
STAC = XCT1
CLRX = XCT0

Signal State at Reset

The Terminal Controller shall set the following output signal to the indicated state when the PWRS input signal is at a logic low:

Signal	Output State at Reset
ADF-0	High-impedance
AOF-0	High-impedance if AE input = logic high
AOF-0	All high or all low if AE input = logic low
AS0	High-impedance
BSAO	High
BSL	High-impedance
BUSQ	High
BUSR	High-impedance
B11-00	High-impedance
CIDB3-0	High-impedance
CLRX	High
CMD	High
DSO	High-impedance
EXST	High
EX3-0	High-impedance
GA	Low
IOCK	High
IXTR	High
LDST	High
MCS	High-impedance
MFG(3-0)	Irrelevant
OP6-0	High-impedance
RCS	High-impedance
RCT(7-0)	All Low
RERF	High
RIVS	High
ROCK	Same as RICK input
RPH1	High
RWO	High-impedance
RXCK	Low
RZ2-0	High-impedance
STAC	High
TXE	High
TXHB	High
TXN	Low
TXO	Low
WAIT	High-impedance
XCS	High-impedance
XCT(7-0)	Low
XERF	High
XIVS	High
XPH1	High
XX4-0	High-impedance
XY4-0	High-impedance
XZ2-0	High-impedance

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-06-16

Approved sources of supply for SMD 5962-99581 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE Number	Vendor similar PIN 2/
5962-9958101QXC	27014	AR629AU9/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P. O. Box 58090 Santa Clara, CA 95052-8090