

# F100101

## Triple 5-Input OR/NOR Gate

### General Description

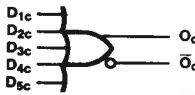
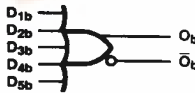
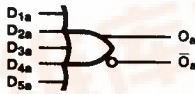
The F100101 is a monolithic triple 5-input OR/NOR gate. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Refer to the F100301 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (−4.2V to −5.7V)

**Ordering Code:** See Section 8

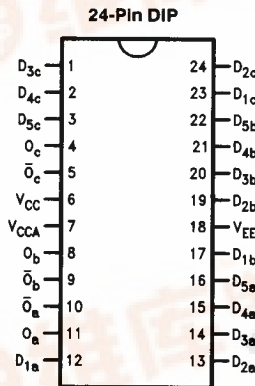
### Logic Symbol



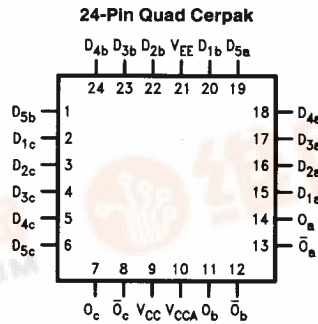
TL/F/9835-3

Pin Names	Description
$D_{1a}, D_{1b}, D_{1c}$	Data Inputs
$O_a, O_b, O_c$	Data Outputs
$\bar{O}_a, \bar{O}_b, \bar{O}_c$	Complementary Data Outputs

### Connection Diagrams



TL/F/9835-1



TL/F/9835-2

## Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
 Maximum Junction Temperature ( $T_j$ )  $+150^{\circ}\text{C}$

Case Temperature under Bias ( $T_C$ )  $0^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 $V_{EE}$  Pin Potential to Ground Pin  $-7.0\text{V}$  to  $+0.5\text{V}$   
 Input Voltage (DC)  $V_{EE}$  to  $+0.5\text{V}$   
 Output Current (DC Output HIGH)  $-50\text{mA}$   
 Operating Range (Note 2)  $-5.7\text{V}$  to  $-4.2\text{V}$

## DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$ ,  $V_{CC} = V_{CCA} = \text{GND}$ ,  $T_C = 0^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
$V_{OH}$	Output HIGH Voltage	-1025	-955	-880	mV	$V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$	Loading with $50\Omega$ to $-2.0\text{V}$
$V_{OL}$	Output LOW Voltage	-1810	-1705	-1620			
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$	Loading with $50\Omega$ to $-2.0\text{V}$
$V_{OLC}$	Output LOW Voltage			-1610			
$V_{IH}$	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
$V_{IL}$	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
$I_{IL}$	Input LOW Current	0.50			$\mu\text{A}$	$V_{IN} = V_{IL}(\text{Min})$	

## DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$ ,  $V_{CC} = V_{CCA} = \text{GND}$ ,  $T_C = 0^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
$V_{OH}$	Output HIGH Voltage	-1020		-870	mV	$V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$	Loading with $50\Omega$ to $-2.0\text{V}$
$V_{OL}$	Output LOW Voltage	-1810		-1605			
$V_{OHC}$	Output HIGH Voltage	-1030			mV	$V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$	Loading with $50\Omega$ to $-2.0\text{V}$
$V_{OLC}$	Output LOW Voltage			-1595			
$V_{IH}$	Input HIGH Voltage	-1150		-870	mV	Guaranteed HIGH Signal for All Inputs	
$V_{IL}$	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
$I_{IL}$	Input LOW Current	0.50			$\mu\text{A}$	$V_{IN} = V_{IL}(\text{Min})$	

## DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$ ,  $V_{CC} = V_{CCA} = \text{GND}$ ,  $T_C = 0^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
$V_{OH}$	Output HIGH Voltage	-1035		-880	mV	$V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$	Loading with $50\Omega$ to $-2.0\text{V}$
$V_{OL}$	Output LOW Voltage	-1830		-1620			
$V_{OHC}$	Output HIGH Voltage	-1045			mV	$V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$	Loading with $50\Omega$ to $-2.0\text{V}$
$V_{OLC}$	Output LOW Voltage			-1610			
$V_{IH}$	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
$V_{IL}$	Input LOW Voltage	-1830		-1490	mV	Guaranteed LOW Signal for All Inputs	
$I_{IL}$	Input LOW Current	0.50			$\mu\text{A}$	$V_{IN} = V_{IL}(\text{Min})$	

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Parametric values specified at  $-4.2\text{V}$  to  $-4.8\text{V}$ .

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

**Note 4:** Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

### DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-4.8V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$I_{IH}$	Input HIGH Current			350	$\mu A$	$V_{IN} = V_{IH} (Max)$
$I_{EE}$	Power Supply Current	-38	-26	-18	mA	Inputs Open

### Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-4.8V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	0.50	1.15	0.50	1.15	0.55	1.30	ns	Figures 1 and 2
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.20	ns	

### Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-4.8V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	0.50	0.95	0.50	0.95	0.55	1.10	ns	Figures 1 and 2
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	1.20	0.45	1.10	0.45	1.10	ns	

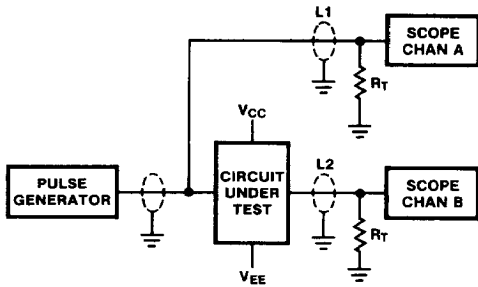


FIGURE 1. AC Test Circuit

TL/F/9835-5

**Notes:**

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- $L1$  and  $L2 =$  equal length  $50\Omega$  impedance lines
- $R_T = 50\Omega$  terminator internal to scope
- Decoupling  $0.1 \mu F$  from GND to  $V_{CC}$  and  $V_{EE}$
- All unused outputs are loaded with  $50\Omega$  to GND
- $C_L =$  Fixture and stray capacitance  $\leq 3 pF$

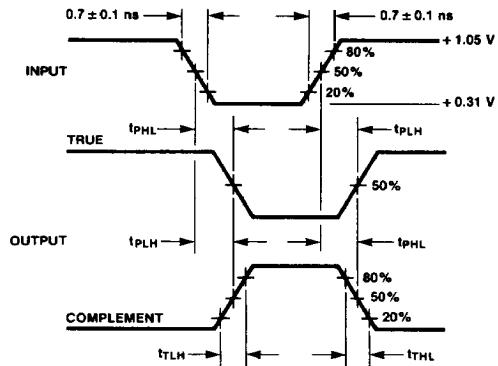


FIGURE 2. Propagation Delay and Transition Times

TL/F/9835-6