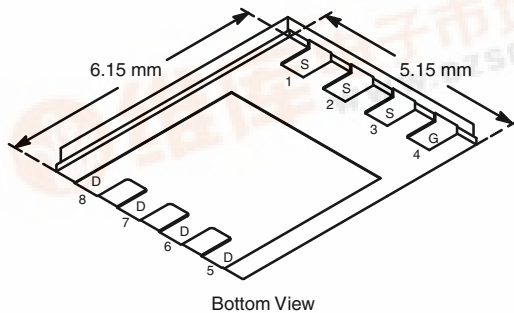


N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, g}	Q _g (Typ.)
30	0.0056 at V _{GS} = 10 V	35 ^g	12 nC
	0.0075 at V _{GS} = 4.5 V	35 ^g	

PowerPAK® SO-8



Ordering Information: SiR482DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

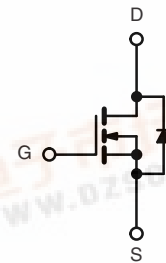
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous Rectification
- DC/DC
 - High-Side Switch
 - Notebook PC



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	35 ^g	A
		35 ^g	
		22.2 ^{b, c}	
		17.8 ^{b, c}	
Pulsed Drain Current (300 μs)	I _{DM}	70	mJ
Continuous Source-Drain Diode Current	I _S	35 ^g	
		4.5 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	20	mJ
Single Pulse Avalanche Energy	E _{AS}	20	
Maximum Power Dissipation	P _D	27.7	W
		17.7	
		5.0 ^{b, c}	
		3.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	3.4	4.5	

Notes:

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.
- Package limited.

SiR482DP


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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		34		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 5.0		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0		2.3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0046	0.0056	Ω
		V _{GS} = 4.5 V, I _D = 20 A		0.0060	0.0075	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 20 A		50		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		1575		pF
Output Capacitance	C _{oss}			335		
Reverse Transfer Capacitance	C _{rss}			113		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A		25	38	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A		12	18	
Gate-Source Charge	Q _{gs}			3.7		
Gate-Drain Charge	Q _{gd}			3.6		
Gate Resistance	R _g	f = 1 MHz	0.3	0.7	1.4	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		11	22	ns
Rise Time	t _r			8	16	
Turn-Off Delay Time	t _{d(off)}			22	40	
Fall Time	t _f			8	16	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 1 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω		16	32	
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			21	42	
Fall Time	t _f			9	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			35	A
Pulse Diode Forward Current ^a	I _{SM}				70	
Body Diode Voltage	V _{SD}	I _S = 3 A		0.73	1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C		20	40	ns
Body Diode Reverse Recovery Charge	Q _{rr}			10	20	nC
Reverse Recovery Fall Time	t _a			10		ns
Reverse Recovery Rise Time	t _b			10		

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

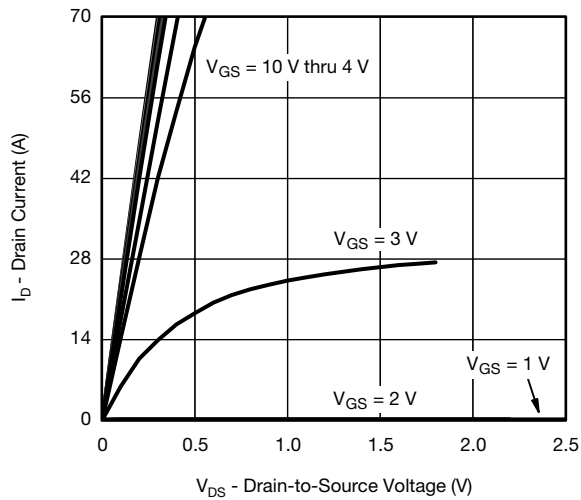
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



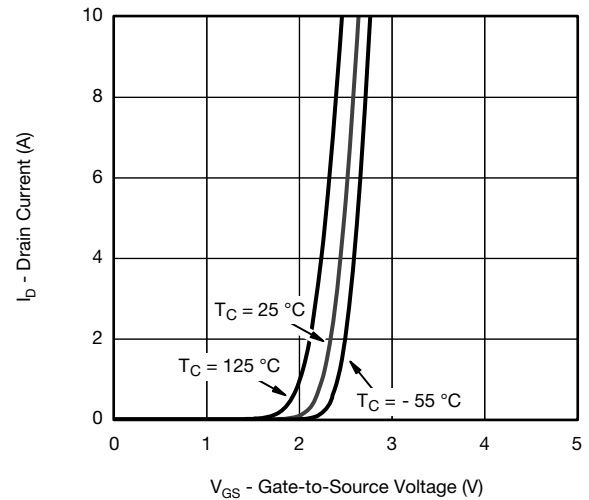
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SiR482DP
Vishay Siliconix

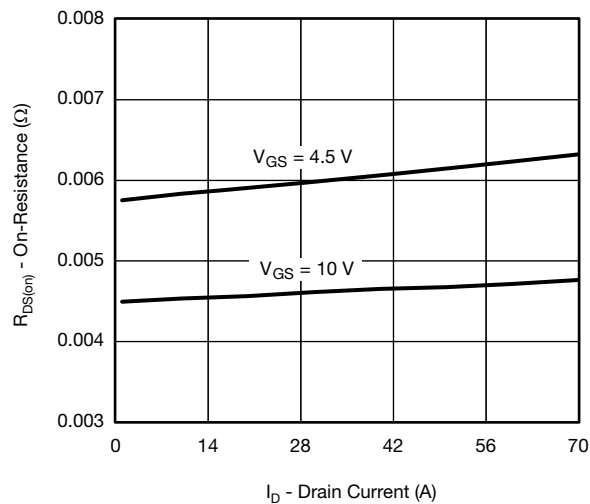
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



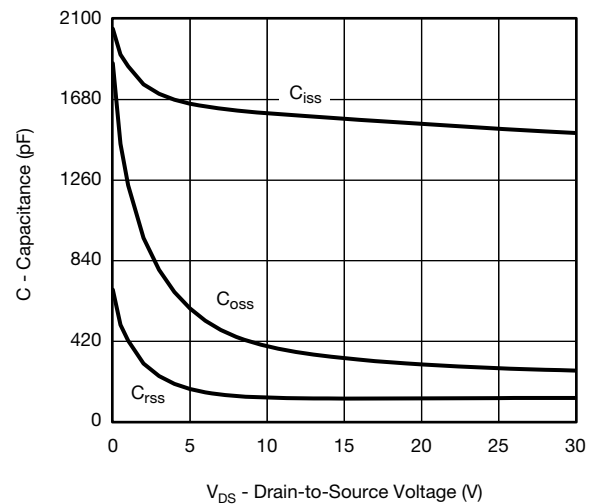
Output Characteristics



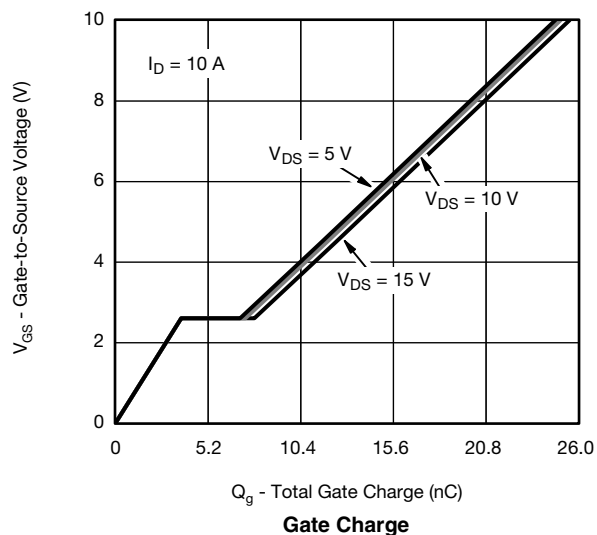
Transfer Characteristics



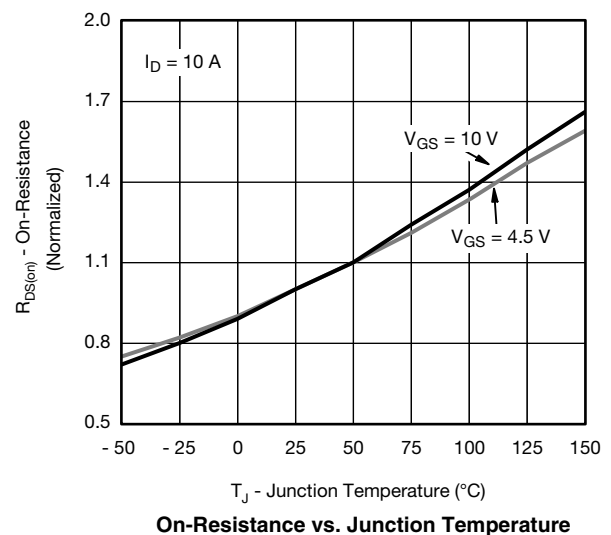
On-Resistance vs. Drain Current



Capacitance



Gate Charge



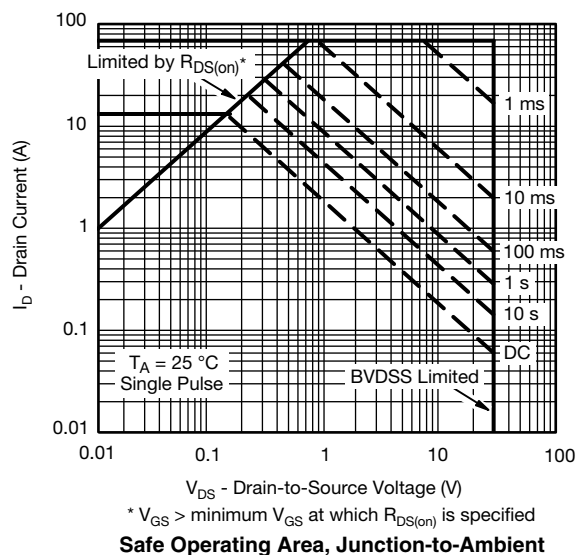
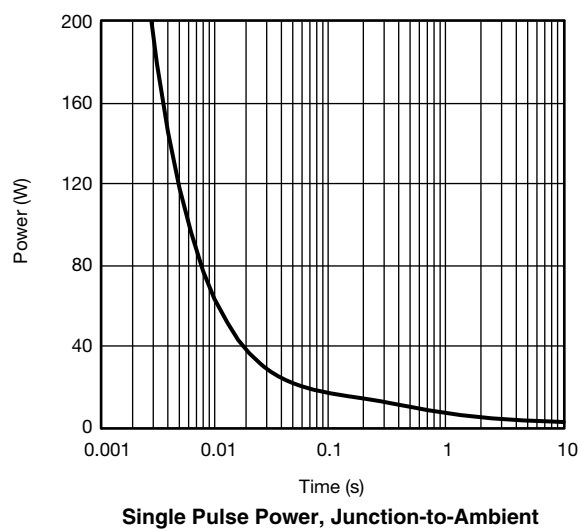
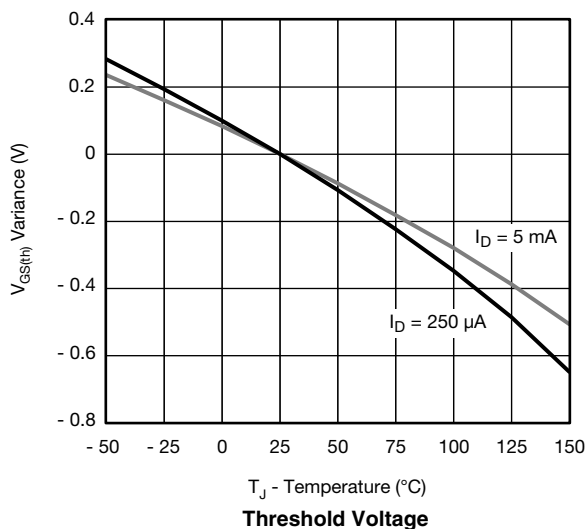
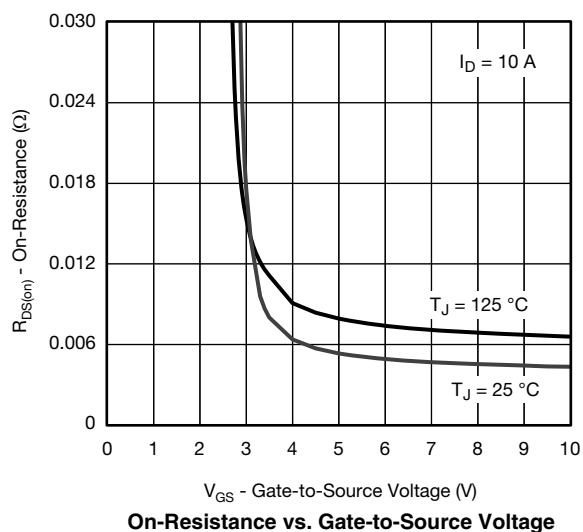
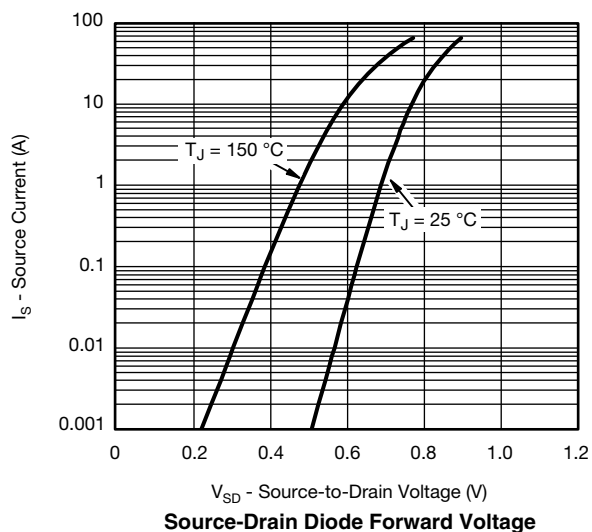
On-Resistance vs. Junction Temperature

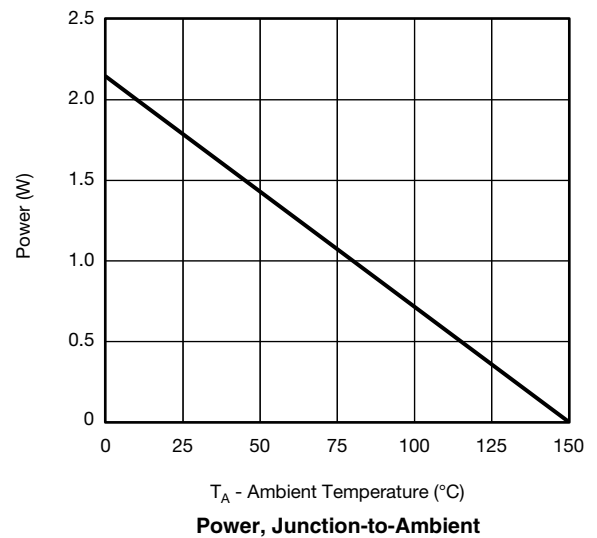
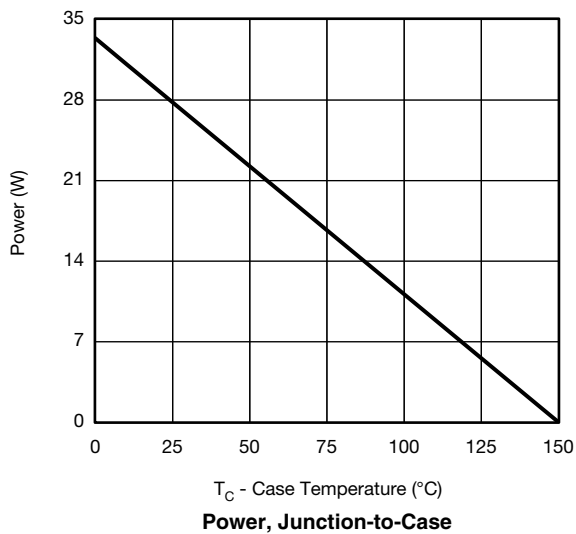
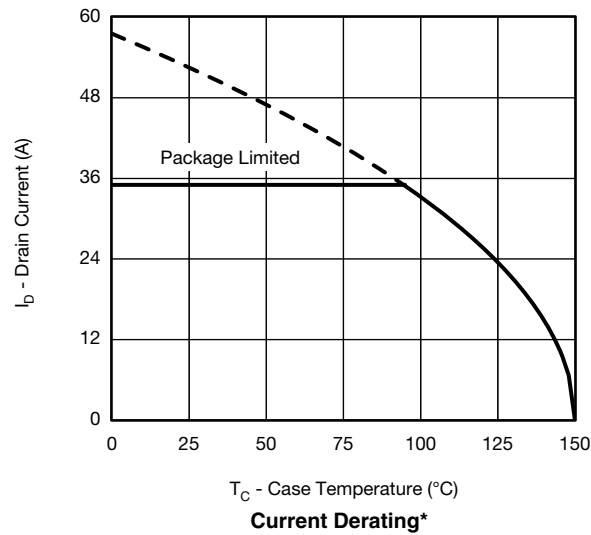
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



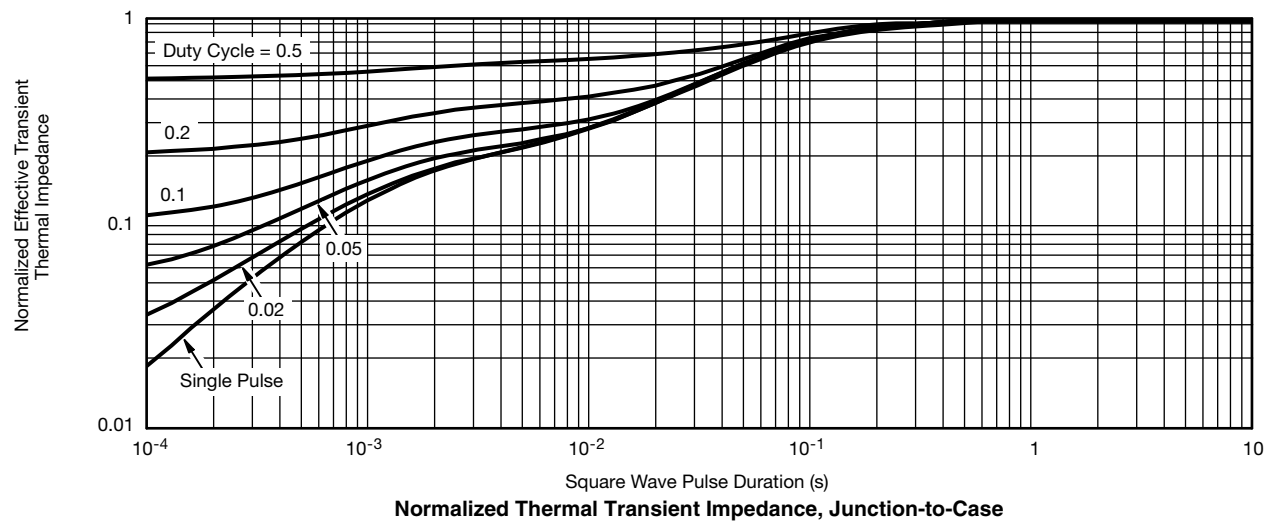
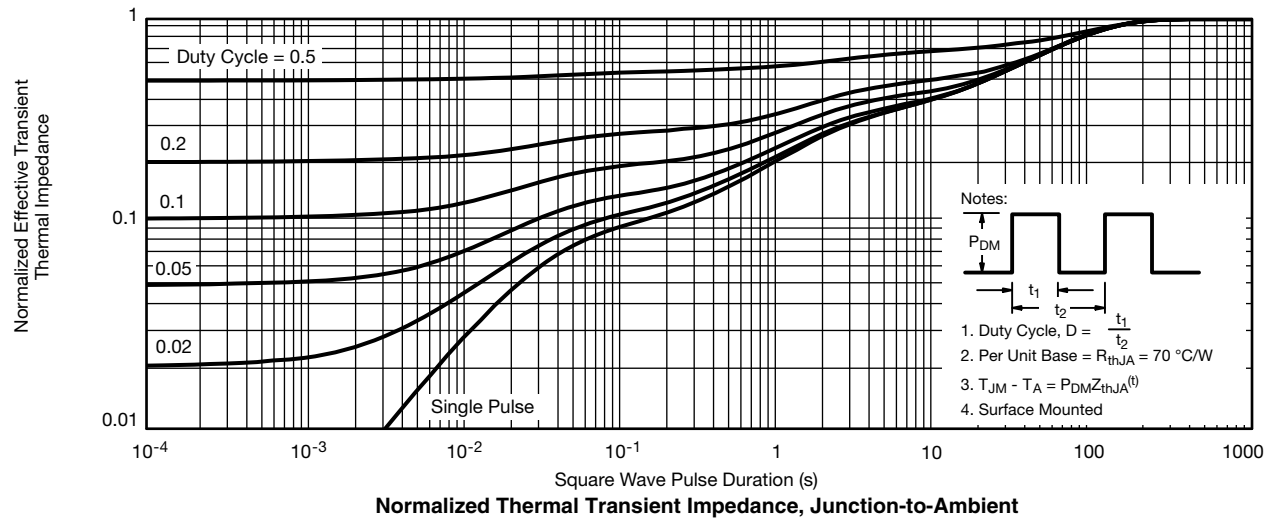

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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