National Semiconductor

August 1990

LM2240
Programmable Timer/Counter

General Description

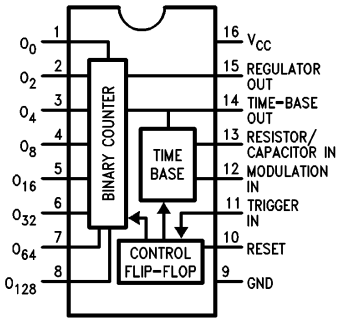
The LM2240 Programmable Timer/Counter is a monolithic controller capable of both monostable and astable operation. Monostable operation allows accurate microsecond to five day time delays. Long delays, up to three years, can easily be generated by cascading two timers. The timer consists of a time-base oscillator, programmable 8-bit counter and control flip-flop. An external resistor-capacitor (RC) network sets the oscillator frequency and allows delay times from 1 RC to 255 RC to be selected. In the astable mode of operation, a single RC network sets the base frequency. The frequencies of the squarewaves at the 8 outputs are each at different factors of 2 from the base frequency. If 2 or more of the outputs are shorted together, various pulse patterns can be generated. These frequencies or pulse patterns can also easily be synchronized to an external signal. The trigger, reset and outputs are all TTL and CMOS compatible for easy interface with digital systems. The timer's high accuracy and versatility in producing a wide range of time delays makes it ideal as a direct replacement for mechanical or electromechanical devices.

Features

- Accurate timing from microseconds to days
- Programmable delays from 1 RC to 255 RC
- TTL and CMOS compatible outputs
- Timing directly proportional to RC time constant
- High accuracy
- External sync and modulation capability
- Wide supply voltage range
- Excellent supply voltage rejection

Connection Diagram

16-Lead Molded DIP



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Top View

See NS Package Number N16E
Order Number LM2240N

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Molded DIP	−65°C to +150°C
Lead Temperature	
Molded DIP (Soldering, 10 Sec.)	265°C
Power Dissipation (Note 2)	1.8W
Junction Temperature	150°C
Supply Voltage	18V
Output Current	10 mA
Output Voltage	18V
Regulator Output Current	5.0 mA
ESD Tolerance (Note 3)	2000V

Operating Ratings

Temperature Range	0°C to 70°C
Supply Range (Note 4)	4V to 15V

LM2240

Electrical Characteristics

$T_A = +25°C$, $V_{CC} = +5.0V$, $R = 10\ k\Omega$, $C = 0.1\ \mu F$, unless otherwise specified. See Block Diagram.

Symbol	Characteristic		Conditions		Min	Typ	Max	Units
GENERAL CHARACTERISTIC								
I_{CC}	Supply Current	Total Circuit	$V_{CC} = 5.0V$, $V_{TR} = 0V$, $V_{RS} = 5.0V$			4.0	7.0	mA
			$V_{CC} = 15V$, $V_{TR} = 0V$, $V_{RS} = 5.0V$			13	18	
		Counter Only				1.5		
V_{REG}	Regulator Output		Measured at Pin 15	$V_{CC} = 5.0V$	3.9	4.4		V
				$V_{CC} = 15V$	5.8	6.3	6.8	
TIME-BASE								
t_{ACC}	Timing Accuracy (Note 5)		$V_{RS} = 0$, $V_{TR} = 5.0V$			3.5	5.0	%
$\Delta t/\Delta T$	Timing Shift with Temperature		$0°C \le T_J \le 70°C$	$V_{CC} = 5.0V$		200		ppm/°C
				$V_{CC} = 15V$		80		
$\Delta t/\Delta V$	Timing Shift with Supply		$V_{CC} \ge 8.0V$			0.08	0.3	%/V
f_{MAX}	Max Frequency		$R = 1.0\ k\Omega$, $C = 0.007\ \mu F$			130		kHz
V_{MOD}	Modulation Voltage Level		Measured at Pin 12	$V_{CC} = 5.0V$	2.80	3.50	4.20	V
				$V_{CC} = 15V$		10.5		
R_T	Recommended Range of Timing Resistor				0.001		10	MΩ
C_T	Recommended Range of Timing Capacitor (Note 6)				0.01		1000	μF

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur.

Note 2: Rating applies to ambient temperature at 25°C. Above this temperature, derate at 15 mW/°C.

Note 3: Human body model, C = 100 pF, $R_S = 1500\Omega$.

Note 4: For operation below 4.5 VDC, short pin 15 to pin 16.

Note 5: Timing error solely introduced by LM2240 measured as % of ideal time-base period of T = RC.

Note 6: Under the conditions of high supply voltages ($V_{CC} > 7.0V$) and low values of timing capacitor ($C_T < 0.1\ \mu F$), a 600 pF capacitor may need to be connected from pin 14 to ground to ensure proper operation.

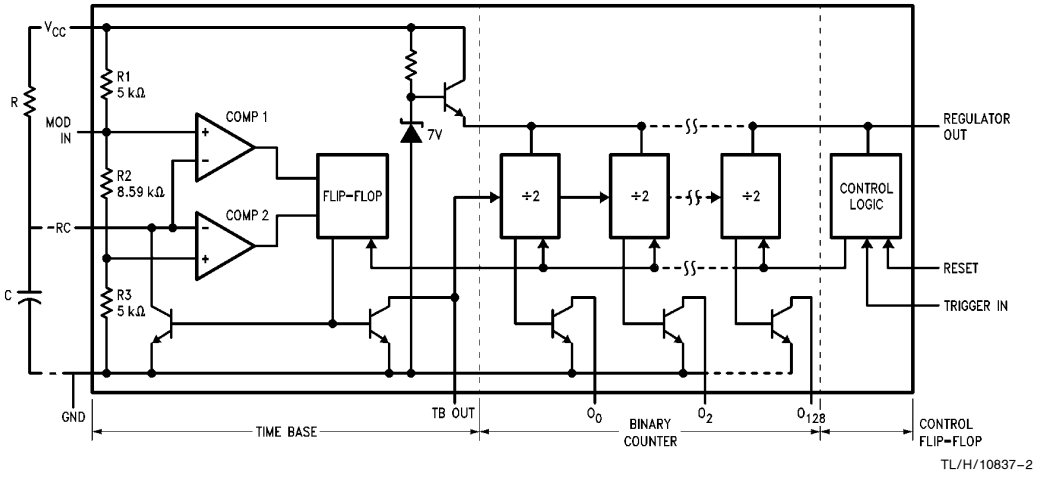
Electrical Characteristics

T_A = +25°C, V_{CC} = +5.0V, R = 10 kΩ, C = 0.1 μF, unless otherwise specified. See Block Diagram.

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
TRIGGER/RESET CONTROLS						
V_{TR}	Trigger Threshold	Measured at Pin 11, V_{RS} = 0V		1.4	2.0	V
I_{TR}	Trigger Current	V_{RS} = 0V, V_{TR} = 2.0V		10		μA
Z_T	Trigger Impedance			25		kΩ
t_{RSPT}	Trigger Response Time (Note 7)			1.0		μs
V_{RS}	Reset Threshold	Measured at Pin 10, V_{TR} = 0V		1.4	2.0	V
I_R	Reset Current	V_{TR} = 0V, V_{RS} = 2.0V		10		μA
Z_R	Reset Impedance			25		kΩ
t_{RSPT}	Reset Response Time (Note 7)			0.8		μs
COUNTER						
TR_{MAX}	Max Toggle Rate	Measured at Pin 14 V_{RS} = 0V, V_{TR} = 5.0V		1.5		MHz
Z_I	Input Impedance			20		kΩ
V_{TH}	Input Threshold		1.0	1.4		V
t_r	Output Rise Time	Measured at Pins 1 through 8 R_L = 3.0 kΩ, C_L = 10 pF		180		ns
t_f	Output Fall Time			180		
I_{O-}	Sink Current	$V_{OL} \leq$ 0.4V	2.0	4.0		mA
I_{CEX}	Leakage Current	V_{OH} = 15V		0.01	15	μA

Note 7: Propagation delay from application of trigger or reset input to corresponding state change in counter output at Pin 1.

Block Diagram



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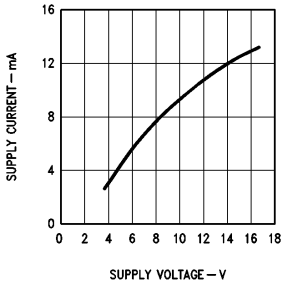
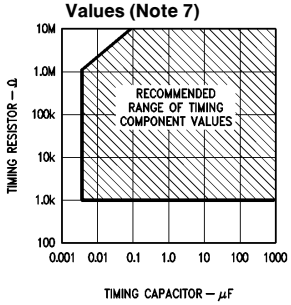
Typical Performance Characteristics

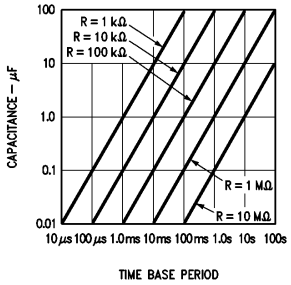
Supply Current vs Supply Voltage in Reset Condition



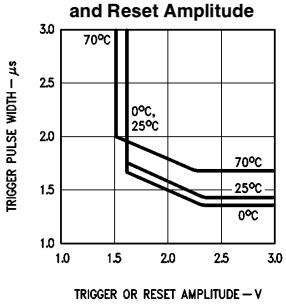
Recommended Range of Timing Component Values (Note 7)



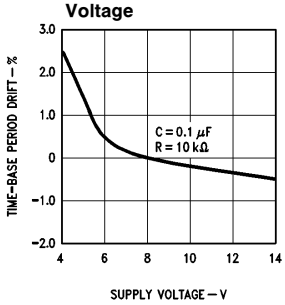
Time-Base Period vs External RC



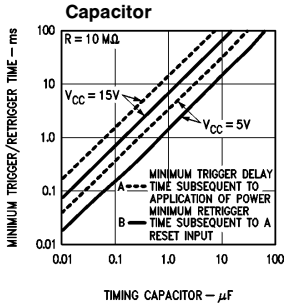
Minimum Trigger and Reset Pulse Widths vs Trigger and Reset Amplitude



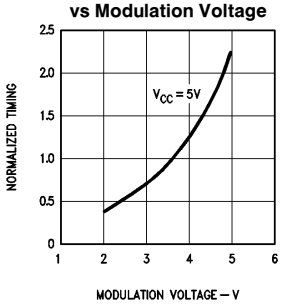
Time-Base Period Drift vs Supply Voltage



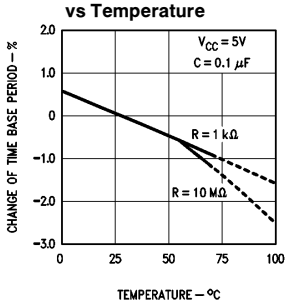
Minimum Trigger/Retrigger Timing vs Timing Capacitor



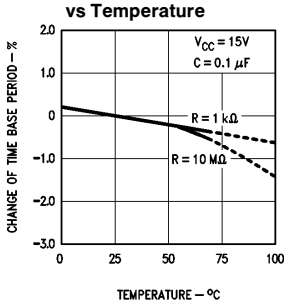
Normalized Change in Time-Base Period vs Modulation Voltage



Time-Base Period vs Temperature



Time-Base Period vs Temperature



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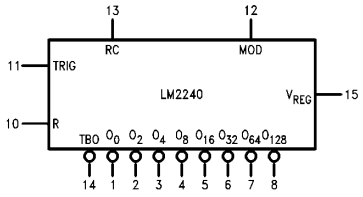
Functional Description



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V_{CC} = Pin 16
GND = Pin 9

FIGURE 1. Logic Symbol

When power is applied to the LM2240 with no trigger or reset inputs activated, the circuit starts with all outputs HIGH. Application of a positive going trigger pulse to the trigger pin initiates the timing cycle. The trigger input activates the time-base oscillator, enables the counter section and sets the counter outputs LOW. The time-base oscillator generates timing pulses with a period T = 1 RC; this is the period of the waveform appearing at pin 14. These clock pulses are counted by the binary counter section. The timing sequence is completed when a positive going reset pulse is applied to the Reset pin.

Once triggered, the circuit is immune from additional trigger inputs until the timing cycle is completed or a reset input is applied. If both the reset and trigger are activated simultaneously, the trigger takes precedence.

Figure 2 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is in a reset state, both the time-base and the counter sections are disabled and all the counter outputs are HIGH.

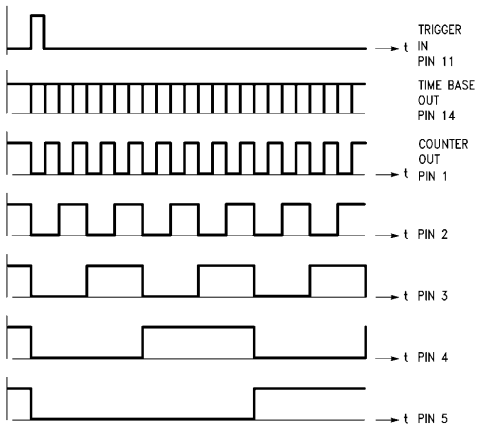

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FIGURE 2. Timing Diagram of Output Waveforms

In monostable applications, one or more of the counter outputs are connected to the reset terminal with S1 closed *(Figure 3)*. The circuit starts timing when a trigger is applied and automatically resets itself to complete the timing cycle when a programmed count is completed. Each of the various multiplies of T shown at the LM2240's outputs in *Figure 3* represent the duration of time, after a trigger pulse, that that particular output is low (it's *not* the period of the waveform) if the output is not tied to any other outputs. T_O represents the duration of time that the circuit output, which is the common point of all the counter outputs which are shorted together, is low. If none of the counter outputs are connected back to the reset terminal (switch S1 open), the circuit operates in an astable or free running mode, following a trigger input.

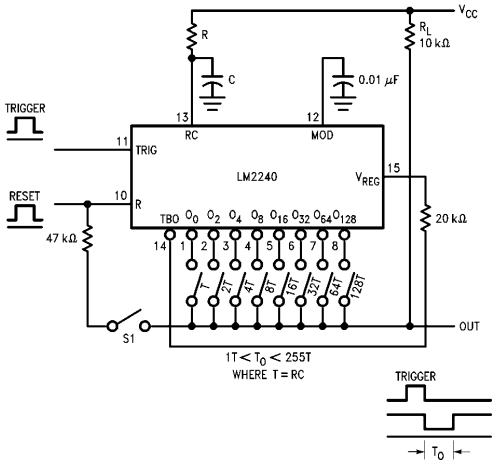

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FIGURE 3. Basic Circuit Connection for Timing Applications (Monostable: S1 Closed; Astable: S1 Open)

Important Operating Information

Ground connection is pin 9.

Reset (R) (pin 10) sets all outputs HIGH.

Trigger (TRIG) (pin 11) sets all outputs LOW.

Time-base output (TBO) (pin 14) can be disabled by bringing the RC input (pin 13) LOW via a 1.0 kΩ resistor.

Normal TBO (pin 14) is a negative going pulse greater than 500 ns.

NOTE: Under the conditions of high supply voltages (V_{CC} > 7.0V) and low values of timing capacitor (C_T < 0.1 μF), the pulse width of TBO may be too narrow to trigger the counter section. This can be corrected by connecting a 600 pF capacitor from TBO (pin 14) to ground (pin 9).

Reset (pin 10) stops the time-base oscillator.

Outputs (O_0 . . . O_{128}) (pins 1–8) sink 2.0 mA current with $V_{OL} \leq 0.4V$.

For use with external clock, minimum clock pulse amplitude should be 3.0V, with greater than 1.0 μs pulse duration.

Circuit Controls

Counter Outputs (O_0 . . . O_{128}, Pins1 thru 8)

The binary counter outputs are buffered open collector type stages, as shown in the block diagram. Each output is capable of sinking 2.0 mA at 0.4V V_{OL}. In the reset condition, all the counter outputs are HIGH or in the nonconducting state. Following a trigger input, the outputs change state in accordance with the timing diagram of *Figure 2*. The counter outputs can be used individually, or can be connected together in a wired-OR configuration, as described in the programming segment of this datasheet.

Reset and Trigger Inputs (R and TRIG, Pins 10 and 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11 respectively. The threshold level for these controls is approximately two diode drops ($\approx$ 1.4V) above ground. Minimum pulse widths for reset and trigger inputs are shown in the Performance Curves. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Modulation and Sync Input (MOD, Pin 12)

The oscillator time-base period (T) can be modulated by applying a DC voltage to MOD, pin 12 (see Performance Curves). Also, the time-base oscillator can be synchronized to an external clock by applying a sync pulse to MOD, pin 12 as shown in *Figure 4*. Recommended sync pulse widths and amplitudes are also given.

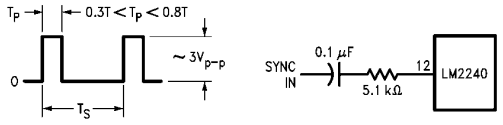

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FIGURE 4. Operation with External Sync Signal

The time-base can be synchronized by setting the sync pulse period (T_S) to be an integer multiple of T. This can be done by choosing the timing components R and C at pin 13 such that:

$T = RC = (T_S/m)$

where:

m is an integer, $1 \leq m \leq 10$

Figure 5 gives the typical pull-in range for harmonic synchronization for various harmonic modulus, m. For $m < 10$, typical pull-in range is greater than $\pm 4\%$ of the time-base frequency.

RC Terminal (Pin 13)

The time-base period T is determined by the external RC network connected to RC, pin 13. When the time-base is triggered, the waveform at pin 13 is an exponential ramp with a period $T = 1$ RC.

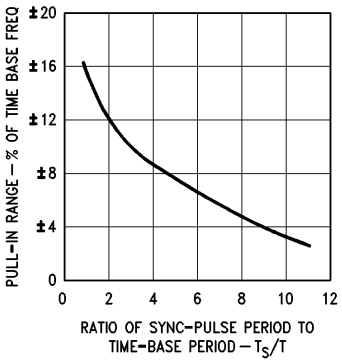

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FIGURE 5. Typical Pull-in Range for Harmonic Synchronization

Time-Base Output (TBO, Pin 14)

The time-base output is an open-collector type stage as shown in the block diagram, and requires a 20 kΩ pull-up resistor to pin 15 for proper circuit operation. In the reset state, the time-base output is HIGH. After triggering, it produces a negative-going pulse train with a period $T = RC$, as shown in the diagram of *Figure 2*. The time-base output is internally connected to the binary counter section and can also serve as the input for the external clock signal when the circuit is operated with an external time base. The counter section triggers on the negative-going edge of the timing or clock pulses generated at TBO, pin 14. The trigger threshold for the counter section is $\approx +1.4$V. The counter section can be disabled by clamping the voltage level at pin 14 to ground.

When using high supply voltage ($V_{CC} > 7.0$V) and a small value timing capacitor ($C_T < 0.1$ μF), the pulse width at TBO pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 600 pF capacitor from pin 14 to ground.

Regulator Output (V_{REG}, Pin 15)

The regulator output V_{REG} is used internally to power the binary counter and the control logic. This terminal can also be used as a supply to additional LM2240 circuits when several timer circuits are cascaded (see *Figure 6*) to minimize power dissipation. For circuit operation with an external clock, V_{REG} can be used as the V_{CC} input terminal so that the internal time-base circuitry is not powered, thus reducing power dissipation. When supply voltages less than 4.5V are used with the internal time-base, pin 15 should be shorted to pin 16.

Circuit Controls (Continued)

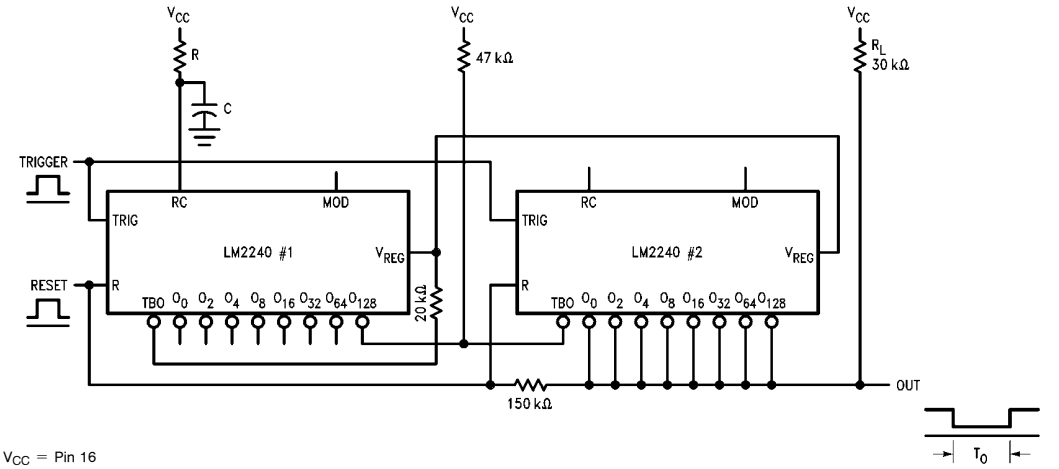


FIGURE 6. Low Power Operation of Cascaded Timers

Monostable Operation

Precision Timing

In precision timing applications, the LM2240 is used in its monostable, or self-resetting, mode. The generalized circuit connection for this application is shown in *Figure 3* (S1 closed). The output is normally HIGH and goes LOW following a trigger input. It remains LOW for the time duration (T_O) and then returns to a HIGH state. The duration of the timing cycle T_O is given as:

$T_O = nT = NRC$

where $T = RC$ is the time-base period as set by the choice of timing components at RC pin 13 (see Performance Curves) and n is an integer in the range of $1 \leq n \leq 255$ as determined by the combination of counter outputs ($O_0 \ldots O_{128}$), pins 1 through 8 connected to the output bus.

Counter Output Programming

The binary counter outputs, $O_0 \ldots O_{128}$, pins 1 through 8 are open collector type stages and can be shorted together to a common pull-up resistor to form a wired-OR connection; the combined output will be LOW as long as any one of the outputs is LOW The time delays associated with each counter output can thus be added together. This is done by simply shorting the outputs together to form a common output bus as shown in *Figure 3*. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, is 32T. Similarly, if pins 1, 5, and 6 are shorted to the output bus, the total time delay is $T_O = (1 + 16 + 32)\ T = 49T$. In this manner, by proper choice of counter terminals connected to the output bus, the timing cycle can be programmed to be $1T \leq T_O \leq 255T$.

Ultra Long Time Delay Application

Two LM2240 units can be cascaded as shown in *Figure 7* to generate extremely long time delays. Total timing cycle of two cascaded units can be programmed from $T_O = 256$ RC to $T_O = 65{,}280$ RC in 256 discrete steps by selectively shorting one or more of the counter outputs from Unit 2 to the output bus. In this application, the reset and the trigger terminals of both units are tied together and the Unit 2 time base is disabled. Normally, the output is HIGH when the system is reset. On triggering, the output goes LOW where it remains for a total of 256 (255) or 65,280 cycles of the time-base oscillator.

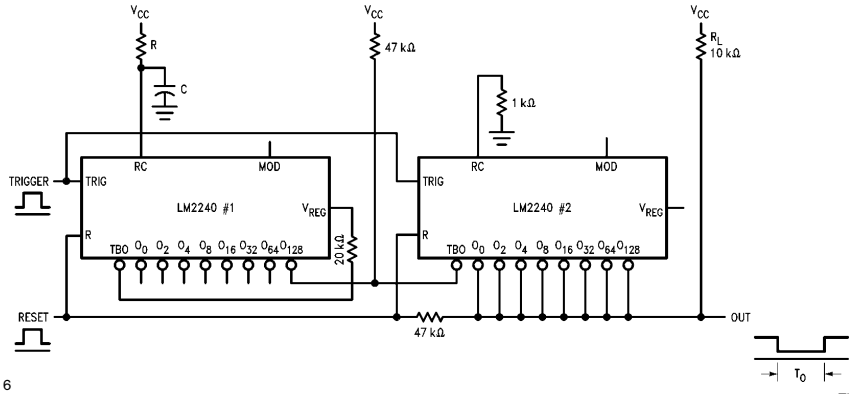
In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption by using the circuit connection of *Figure 6*. In this case, the V_{CC} terminal (pin 16) of Unit 2 is left open, and the second unit is powered from the regulator output of Unit 1 by connecting the V_{REG} (pin 15) of both units together.

Astable Operation

The LM2240 can be operated in its astable or free running mode by disconnecting the reset terminal (pin 10) from the counter outputs. Two typical circuits are shown in *Figures 8* and *9*. The circuit in *Figure 8* operates in its free running mode with external trigger and reset signals. It starts counting and timing following a trigger input until an external reset pulse is applied. Upon application of a positive going reset signal to pin 10, the circuit reverts back to its reset state. This circuit is essentially the same as that of *Figure 3* with the feedback switch S1 open.

The circuit of *Figure 9* is designed for continuous operation. It self triggers automatically when the power supply is turned on, and continues to operate in its free running mode indefinitely. In astable or free running operation, each of the counter outputs can be used individually as synchronized oscillators, or they can be interconnected to generate complex pulse patterns.

Astable Operation (Continued)



V_{CC} = Pin 16
GND = Pin 9

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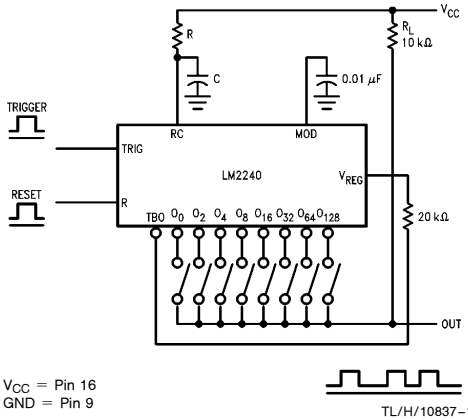
FIGURE 7. Cascaded Operation for Long Delays

Binary Pattern Generation

In astable operation, as shown in *Figures 8* and *9*, the output of the LM2240 appears as a complex pulse pattern if more than one of its switches is closed. The waveform of the output pulse train can be determined directly from the timing diagram of *Figure 2*, which shows the phase relations between the counter outputs. *Figures 10* and *11* show some of the complex pulse patterns that can be generated. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.



V_{CC} = Pin 16
GND = Pin 9

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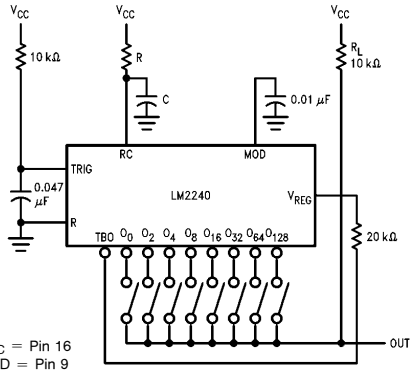
FIGURE 8. Astable Operation with Trigger and Reset Inputs



V_{CC} = Pin 16
GND = Pin 9

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FIGURE 9. Free Running Astable Operation

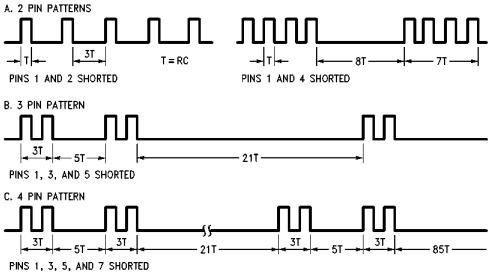

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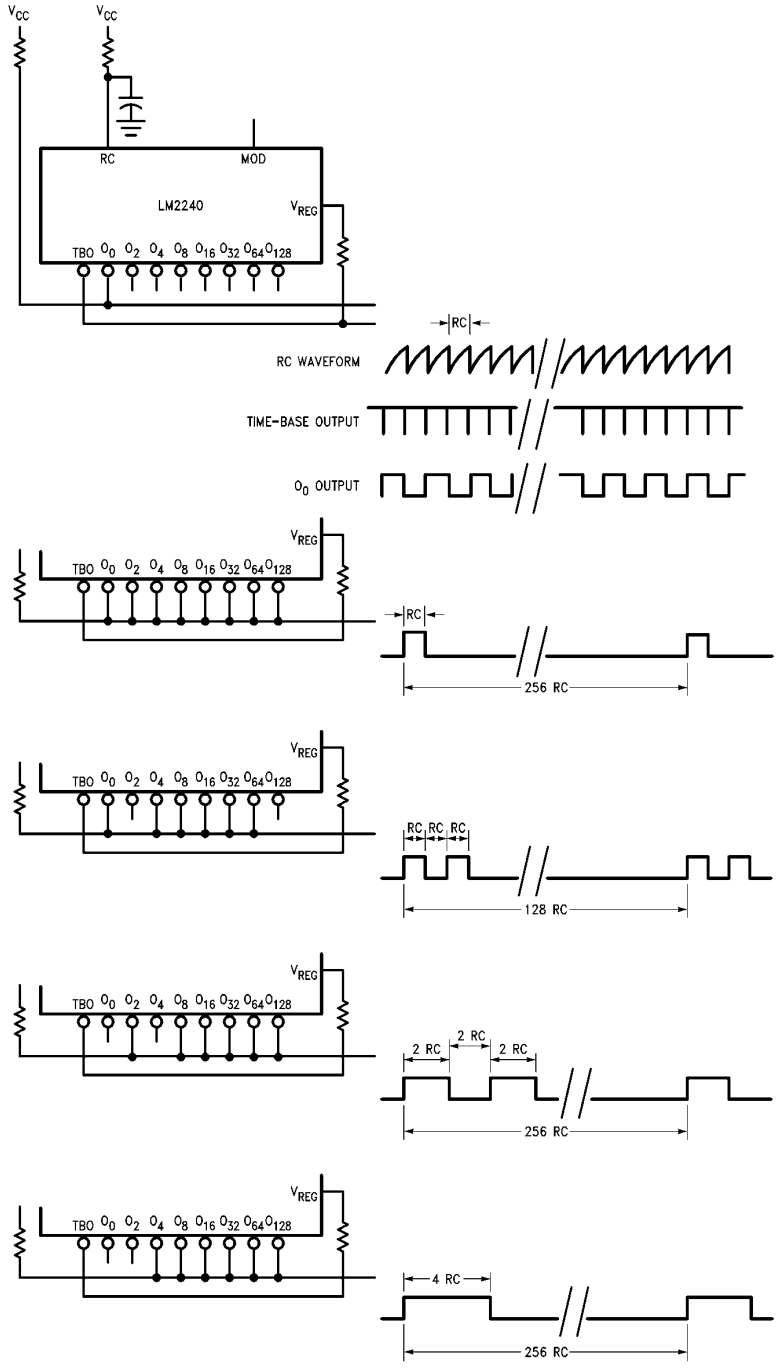
FIGURE 10. Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

Astable Operation (Continued)



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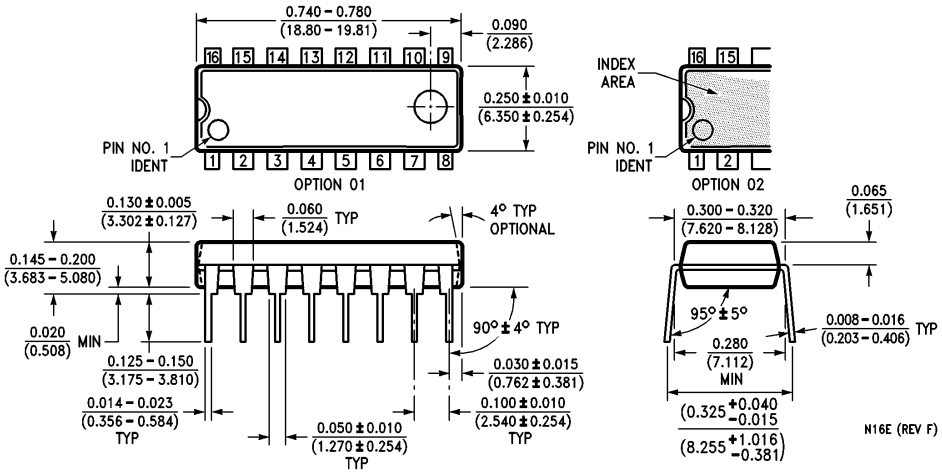
V_{CC} = Pin 16
GND = Pin 9

FIGURE 11. Astable Operation Examples of Output

Physical Dimensions inches (millimeters)



16-Lead Molded DIP LM2240 (N)
NS Package Number N16E

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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