REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET	55	56	57	58	59	60	61	62	63	64										
REV																				
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV															
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
97-06-10

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, 3 VOLT, MULTIMEDIA VIDEO PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-96791

SHEET 1 OF 64

DSCC FORM 2233
APR 97

5962-E186-97

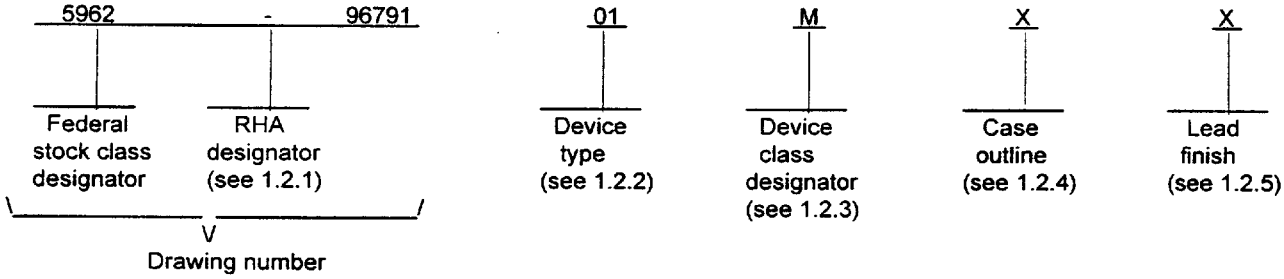
DISTRIBUTION STATEMENT A Approved for public release; distribution is unlimited.

9004708 0031680 951

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320C80-50	Multimedia video processor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	P-CK	305	Pin grid array
Y	(See figure 1)	320 1/	Ceramic quad flatpack with non-conductive tie bar

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ This case outline contains capacitor pads located on top of the package. The terminals are referenced clockwise starting at the index corner. See Figure 2 for terminal values.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.3 V dc to +4.0 V dc
Input voltage range (V_{IN})	-0.3 V dc to + 4.0 V dc
Output voltage range (V_{OUT})	-0.3 V dc to + 4.0 V dc
Storage temperature range (T_{STG})	-55°C to +150°C
Thermal resistance, junction-to-case (θ_{JC})	
Case X	1.4 °C/W
Case Y	2°C/W
Maximum power dissipation (P_D)	8.6 W
Junction temperature (T_J)	175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	3.135 V dc to 3.465 V dc
Supply voltage range (V_{SS})	0 V dc to 0 V dc
Case operating temperature range (T_C)	-55°C to +125°C
High level output current (I_{OH})	-400 µA
Low level output current (I_{OL})	2 mA

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, bulletin, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electrons Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations which prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.2.5 Boundary scan instruction code. For device 01 the boundary scan instruction codes shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. Device type 01 shall be compliant with IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage	V_{IH}		1,2,3	All	2	V_{DD}+0.3	V
Low level input voltage	V_{IL}		1,2,3	All	-0.3	0.8	V
High level output voltage	V_{OH}	V_{DD} = min, I_{OH} = max	1,2,3	All	1.85		V
Low level output voltage	V_{OL}	V_{DD} = max, I_{OL} = max	1,2,3	All		0.9	V
Output current, leakage (high-impedance) (except EMU0, & EMU1)	I_O	V_{DD} = max, V_O = 2.8 V	1,2,3	All		20	µA
		V_{DD} = max, V_O = 0.6 V				-20	
Input current (except TCK, TDI, & TMS, TRST)	I_I	$V_I = V_{SS}$ to V_{DD}	1,2,3	All		±20	µA
Supply current 1/	I_{DD}	V_{DD} = max, 50 MHz	1,2,3	All		2.5	A
Input capacitance	C_I	See 4.4.1c	4	All		15	pF
Output capacitance	C_O	See 4.4.1c	4	All		15	pF
Functional test		See 4.4.1b	7,8	All			
Period of CLKIN (t_H)	1	($t_{C(CKI)}$	9,10,11	All	10		ns
Pulse duration of CLKIN high	2		9,10,11	All	4.2		ns
Pulse duration of CLKIN low	3		9,10,11	All	4.2		ns
Transition time of CLKIN 2/	4		9,10,11	All		1.5	ns
Period of CLKOUT	5		9,10,11	All	$2t_{c(CKI)}$ 3/		ns
Pulse duration of CLKOUT high	6		9,10,11	All	t_H-4.5		ns
Pulse duration of CLKOUT low	7		9,10,11	All	t_H-4.5		ns
Transition time of CLKOUT	8		9,10,11	All		2.5 2/	ns
Duration of RESET low	9	Initial reset during power-up	9,10,11	All	$6t_H$		ns
		Reset during active operation			$6t_H$		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time of $\overline{FREQ}$ low to $\overline{RESET}$ high to configure self-bootstrap mode	10		9,10,11	All	$4t_H$		ns
Hold time $\overline{FREQ}$ low to $\overline{RESET}$ high to configure self-bootstrap mode	11		9,10,11	All	0		ns
Setup time of $\overline{UTIME}$ low to $\overline{RESET}$ high to configure big endian operation	12		9,10,11	All	$4t_H$		ns
Hold time $\overline{UTIME}$ low after $\overline{RESET}$ high to configure big endian operation	13		9,10,11	All	0		ns
Setup time, AS, BS, CT, PS, and $\overline{UTIME}$ valid to CLKOUT no longer low	14		9,10,11	All	8		ns
Hold time, AS, BS, CT, PS, and $\overline{UTIME}$ valid to CLKOUT high	15		9,10,11	All	2		ns
Access time, AS, BS, CT, PS, and $\overline{UTIME}$ valid after memory identification (A, STATUS) valid	16		9,10,11	All		$3t_H$-10	ns
Access time, $\overline{RETRY}$, READY, $\overline{FAULT}$ valid after memory inden-tification (A, STATUS) valid	17		9,10,11	All		nt_H-8	ns
Setup time, $\overline{RETRY}$, READY, $\overline{FAULT}$ valid to CLKOUT no longer high	18		9,10,11	All	7.5		ns
Hold time, $\overline{RETRY}$, READY, $\overline{FAULT}$ valid to CLKOUT low	19		9,10,11	All	1.2		ns
Access time $\overline{RETRY}$, READY, valid from $\overline{RAS}$ low	20		9,10,11	All		nt_H-7.5	ns
Access time $\overline{RETRY}$, READY, valid from $\overline{RC}$ low	21		9,10,11	All		nt_H-7.5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Access time , READY valid from $\overline{CAS}$ low	22	2cyc/col accesses	9,10,11	All		t_H-12	ns
		3cyc/col accesses				$2t_H$-8	
Hold time, CLKOUT high after output valid	23	D(63:0)	9,10,11	All	nt_H-5.6		ns
		A(31:0), STATUS(5:0), $\overline{CAS}$/DQM(7:0), 4/			nt_H-5.0		
		$\overline{DBEN}$, $\overline{DDTN}$ DSF, $\overline{RAS}$ $\overline{TRG}$/$\overline{CAS}$,W,RL			nt_H-4.3		
Hold time, CLKOUT low after output valid	24	D(63:0)	9,10,11	All	nt_H-5.6		ns
		A(31:0), STATUS(5:0), $\overline{CAS}$/DQM(7:0), 4/			nt_H-5.0		
		$\overline{DBEN}$, $\overline{DDTN}$ DSF, $\overline{RAS}$ $\overline{TRG}$/$\overline{CAS}$,W, RL			nt_H-4.3		
Hold time, output valid after CLKOUT low	25		9,10,11	All	nt_H-5.5		ns
Hold time, output valid after CLKOUT high	26		9,10,11	All	nt_H-5.0		ns
Hold time, output valid after output valid	27	D(63:0)	9,10,11	All	nt_H-6.5		ns
		A(31:0), STATUS(5:0), $\overline{CAS}$/DQM(7:0), 4/	9,10,11		nt_H-6.0		
		$\overline{DBEN}$, $\overline{DDTN}$ DSF, $\overline{RAS}$ $\overline{TRG}$/$\overline{CAS}$,W, RL	9,10,11		nt_H-5.0		
Delay time, CLKOUT no longer low to output valid	28	D(63:0)	9,10,11	All		nt_H+6.5	ns
		A(31:0), STATUS(5:0), $\overline{CAS}$/DQM(7:0), 4/				nt_H+5.5	
		$\overline{DBEN}$, $\overline{DDTN}$ DSF, $\overline{RAS}$ $\overline{TRG}$/$\overline{CAS}$,W, RL				nt_H+5	
Delay time, CLKOUT no longer high to output valid	29	D(63:0)	9,10,11	All		nt_H+6.5	ns
		A(31:0), STATUS(5:0), $\overline{CAS}$/DQM(7:0), RL 4/				nt_H+5.5	
		$\overline{DBEN}$, $\overline{DDTN}$ DSF, $\overline{RAS}$ $\overline{TRG}$/$\overline{CAS}$,W, RL				nt_H+5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, output no longer valid to CLKOUT high	30		9,10,11	All		nt_H+5.0	ns
Delay time, output no longer valid to CLKOUT low	31		9,10,11	All		nt_H+5.5	ns
Delay time, output no longer valid to output valid	32	D(63:0)	9,10,11	All		nt_H+6.5	ns
		A(31:0), STATUS(5:0), $\overline{CAS}$/DQM(7:0), 4/				nt_H+6.0	
		$\overline{DBEN}$, $\overline{DDTN}$ DSF, $\overline{RAS}$ $\overline{TRG/CAS}$,W, $\overline{RL}$				nt_H+5	
Pulse width, output valid	33	D(63:0)	9,10,11	All	nt_H-6.5		ns
		A(31:0), STATUS(5:0), $\overline{CAS}$/DQM(7:0), 4/			nt_H-6.0		
		$\overline{DBEN}$, $\overline{DDTN}$ DSF, $\overline{RAS}$ $\overline{TRG/CAS}$,W, $\overline{RL}$			nt_H-5.0		
Access time, CLKOUT high to D(63:0) valid	34		9,10,11	All		nt_H-5.3	ns
Access time, CLKOUT low to D(63:0) valid	35		9,10,11	All		nt_H-6.5	ns
Setup time, D(63:0) valid to CLKOUT no longer low	36		9,10,11	All	6.1		ns
Setup time, D(63:0) valid to CLKOUT no longer high	37		9,10,11	All	6.1		ns
Hold time, D(63:0) valid to CLKOUT no longer low	38		9,10,11	All	2		ns
Hold time, D(63:0) valid to CLKOUT no longer high	39		9,10,11	All	2		ns
Access time, output valid to D(63:0) inputs valid	40	A(31:0), STATUS(5:0), $\overline{CAS}$/DQM(7:0) 4/, $\overline{RL}$	9,10,11	All		nt_H-7	ns
		$\overline{DBEN}$, $\overline{DDTN}$ DSF, $\overline{RAS}$ $\overline{TRG/CAS}$,W				nt_H-6.5	
Hold time, D(63:0) valid after output valid	41 5/	$\overline{RAS}$, $\overline{CAS}$/DQM(7:0)	9,10,11	All	3		ns
		A(31:0)			3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Pulse duration, CAS/DQM high	42		9,10,11	All	t_H-2		ns
Pulse duration, CAS/DQM low	43		9,10,11	All	$3t_H$-9.5		ns
Hold time, CAS/DQM high after output valid	44	D(63:0)	9,10,11	All	nt_H-4.5		ns
		A(31:0), STATUS(5:0), CAS/DQM(7:0),			nt_H-4.0		
		DBEN, DDTN DSF, RAS TRG/CAS ,W, RL			nt_H-3.0		
Hold time, output valid CAS/DQM low	45		9,10,11	All	nt_H-9.5		ns
Access time, data valid from CAS/DQM low	46		9,10,11	All		$3t_H$-12	ns
Hold time, data valid after CAS/DQM high	47		9,10,11	All	2		ns
Pulse duration, EINTx low 7/	48	6/	9,10,11	All	6		ns
Setup time, EINTx high before CLKOUT no longer low 8/	49	6/	9,10,11	All	9.5		ns
Pulse duration, EINTx high 7/	50	6/	9,10,11	All	6		ns
Setup time, LINTx low before CLKOUT no longer high 8/	51	6/	9,10,11	All	9.5		ns
Pulse duration, XPTx valid 9/	52		9,10,11	All	$12t_H$		ns
Setup time, XPT(2:0) valid before CLKOUT no longer low 10/	53		9,10,11	All	12		ns
Hold time, XPT(2:0) valid after CLKOUT high	54		9,10,11	All	5		ns
Hold time, XPT(2:0) valid after RL low 11/	55		9,10,11	All		$6t_H$	ns
Setup time REQ1 - REQ0 valid to CLKOUT no longer low	56		9,10,11	All	t_H-7		ns
Hold time, REQ(1:0) valid after CLKOUT high	57		9,10,11	All	t_H-7		ns
Hold time, HACK high after HREQ low 9/	58		9,10,11	All	$4t_H$-12		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, HACK low to output hi-z 7/	59	All signals except D(63:0)	9,10,11	All		1	ns
		D(63:0)				1	
Delay time, HREQ high to HACK no longer low	60		9,10,11	All		10	ns
Delay time, HACK high to outputs driven 9/	61		9,10,11	All	$6t_H$		ns
Setup time, HREQ low to CLKOUT no longer low	62		9,10,11	All	8.5		ns
SCLK period	63		9,10,11	All	13		ns
Pulse width, SCLK high	64		9,10,11	All	5		ns
Pulse width, SCLK low	65		9,10,11	All	5		ns
Transition time, SCLK (rise and fall) 2/	66		9,10,11	All		2	ns
FCLK period	67		9,10,11	All	25		ns
Pulse width, FCLK high	68		9,10,11	All	8		ns
Pulse width, FCLK low	69		9,10,11	All	8		ns
Transition time, FCLK (rise and fall) 2/	70		9,10,11	All		2	ns
Hold time, HSYNC, VSYNC, CSYNC/HBLNK CBLNK/VBLNK or CAREA high after FCLK low	71		9,10,11	All	0		ns
Hold time, HSYNC, VSYNC, CSYNC/HBLNK CBLNK/VBLNK or CAREA low after FCLK low	72		9,10,11	All	0		ns
Delay time, FCLK low to HSYNC, VSYNC, CSYNC/HBLNK CBLNK/VBLNK or CAREA low	73		9,10,11	All		20	ns
Delay time, FCLK low to HSYNC, VSYNC, CSYNC/HBLNK CBLNK/VBLNK or CAREA high	74		9,10,11	All		20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, $\overline{HSYNC}$, $\overline{VSYNC}$, or $\overline{CSYNC}$ low to FCLK no longer low 12/	75		9,10,11	All	5		ns
Hold time, $\overline{HSYNC}$, $\overline{VSYNC}$, or $\overline{CSYNC}$ high after FCLK high 13/	76		9,10,11	All	7		ns
Setup time, $\overline{HSYNC}$, $\overline{VSYNC}$, or $\overline{CSYNC}$ high to FCLK no longer low 14/	77		9,10,11	All	5		ns
Hold time, $\overline{HSYNC}$, $\overline{VSYNC}$, or $\overline{CSYNC}$ low after FCLK high 15/	78		9,10,11	All	7		ns
JTAG							
TMS/TDI setup to TCK high	t_{su}		9, 10, 11	All	20		ns
TMS/TDI hold from TCK high	t_h		9, 10, 11	All	15		ns
TCK low to TDO valid	t_d		9, 10, 11	All		30	ns

1/ Unless otherwise specified, all testing to be performed using worst-case test conditions. t_H is one half of the output period, or equal to the input clock (parameter 1). $t_{C(CKI)}$ is equal to parameter 1. AC timing waveforms are as specified in figure 4.
2/ This parameter is verified by computer simulation and is not tested.
3/ This is a functional minimum and is not tested. This parameter may also be specified as $2t_H$.
4/ Except for $\overline{CAS}$/DQM(7:0) during nonuser-timed 2 cycle/column accesses.
5/ Applies to $\overline{RAS}$, $\overline{CAS}$/DQM(7:0) and A(31:0) transitions that occur on CLKOUT edge coincident with input data sampling.
6/ In order to guarantee recognition, $\overline{LINT4}$ must remain low until cleared by the interrupt service routine.
7/ This parameter is guaranteed by characterization and is not tested.
8/ This parameter must only be met to ensure that the interrupt is recognized on the indicated cycle.
9/ This parameter is a functional minimum guaranteed by logic and is not tested.
10/ This parameter must only be met to ensure that the $\overline{XPT}$ input is recognized on the indicated cycle.
11/ This parameter must be met to ensure that a second $\overline{XPT}$ request does not occur. This parameter is a functional maximum guaranteed by logic and is not tested.
12/ This parameter must only be met to ensure the input is recognized as low at FCLK edge B.
13/ This parameter must only be met to ensure the input is recognized as low at FCLK edge A.
14/ This parameter must only be met to ensure the input is recognized as low at FCLK edge D.
15/ This parameter must only be met to ensure the input is recognized as low at FCLK edge C.

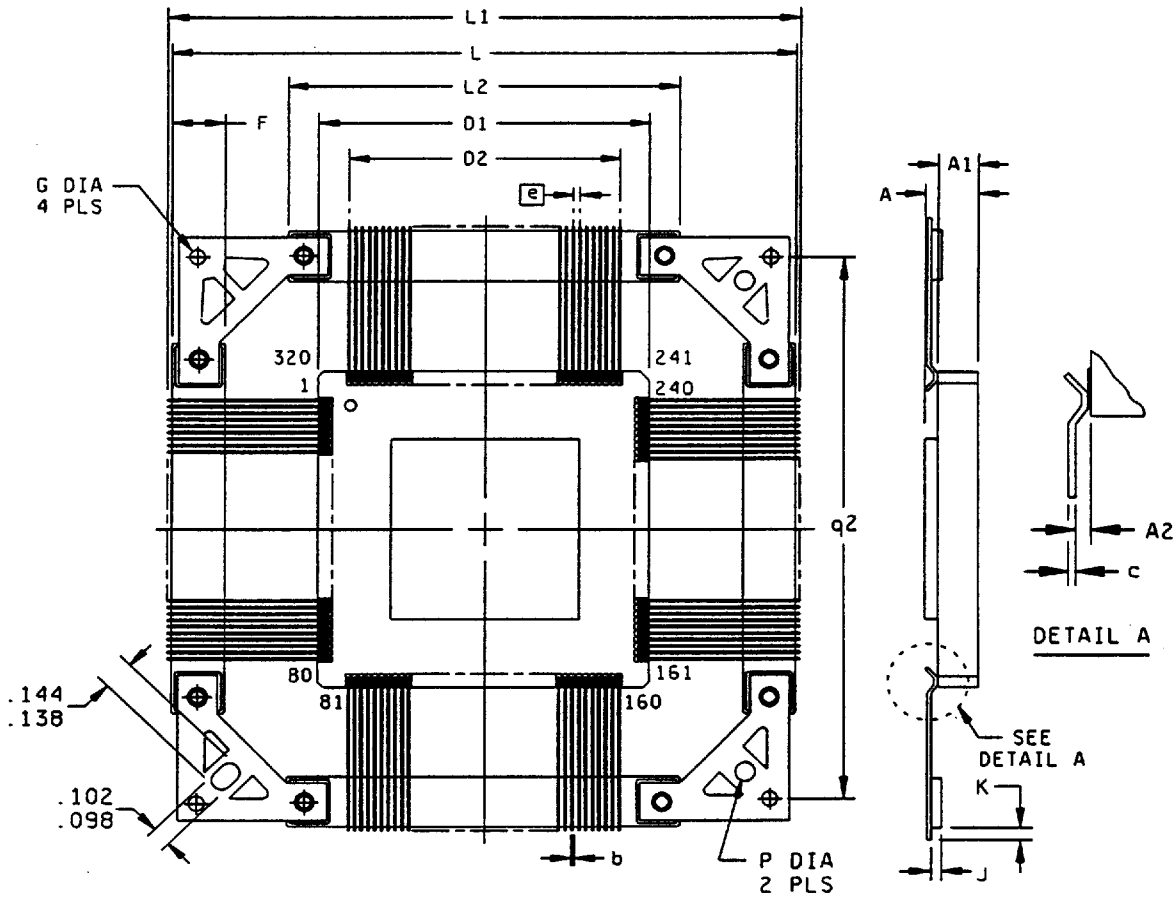


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216	SIZE A		5962-96791
		REVISION LEVEL	SHEET 13

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.55		0.179
A1		4.00		0.157
A2	0.05	0.35	0.002	0.013
b	0.18	0.25	0.007	0.010
c	0.10	0.20	0.004	0.008
D1	43.56	44.44	1.714	1.749
D2	39.50 BSC		1.555 BSC	
e	0.50 BSC		0.019 BSC	
F	4.50	5.50	0.177	0.216
G	1.45	1.55	0.057	0.061
J	0.75	1.05	0.029	0.041
K		0.50		0.019
L	74.60	75.40	2.937	2.968
L1	74.85	76.40	2.946	3.007
P	2.50	2.60	0.098	0.102
q2	70.00 BSC		2.755 BSC	

FIGURE 1. Case outline - Continued.

Device type	01	Device type	01	Device type	01	Device type	01
Case outline	X	Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A5	CT1	C3	V_{SS}	D32	V_{DD}	F26	V_{SS}
A7	V_{DD}	C5	STATUS3	D34	$\overline{VSYNC0}$	F28	V_{DD}
A9	$\overline{HACK}$	C7	AS2	E1	AS1	F32	V_{SS}
A11	V_{SS}	C9	V_{SS}	E3	$\overline{FAULT}$	F34	V_{DD}
A13	$\overline{CAS7}$	C11	CT0	E5	V_{SS}	G1	V_{DD}
A15	$\overline{CAS5}$	C13	PS2	E7	STATUS2	G3	A2
A17	V_{DD}	C15	V_{DD}	E9	READY	G5	A1
A19	V_{SS}	C17	CLKIN	E11	BS0	G31	$\overline{EINT2}$
A21	$\overline{RAS}$	C19	$\overline{CAS2}$	E13	V_{SS}	G33	$\overline{CBLNK1}$/$\overline{VBLNK1}$
A23	DSF	C21	V_{DD}	E15	$\overline{HREQ}$	G35	V_{DD}
A25	V_{SS}	C23	$\overline{W}$	E17	$\overline{CAS4}$	H2	STATUS0
A27	SCLK1	C25	$\overline{DBEN}$	E19	$\overline{RL}$	H4	A3
A29	V_{DD}	C27	V_{SS}	E21	STATUS5	H32	$\overline{CSYNC1}$/$\overline{HBLNK1}$
A31	$\overline{EINT1}$	C29	CAREA0	E23	V_{SS}	H34	TD1
B2	NC	C31	$\overline{CBLNK0}$/$\overline{VBLNK0}$	E25	CLKOUT	J1	STATUS1
B4	BS1	D2	$\overline{RETRY}$	E27	$\overline{LINT4}$	J3	V_{SS}
B6	V_{DD}	D4	V_{DD}	E29	$\overline{EINT3}$	J5	V_{DD}
B8	PS1	D6	V_{SS}	E31	V_{SS}	J31	V_{DD}
B10	REQ1	D8	AS0	E33	$\overline{HSYNC0}$	J33	V_{SS}
B12	V_{DD}	D10	$\overline{UTIME}$	E35	TCK	J35	EMU1
B14	$\overline{CAS6}$	D12	V_{SS}	F2	V_{DD}	K2	STATUS4
B16	$\overline{CAS3}$	D14	$\overline{RESET}$	F4	V_{SS}	K4	A6
B18	V_{DD}	D16	REQ0	F10	V_{DD}	K32	$\overline{VSYNC1}$
B20	$\overline{CAS1}$	D18	V_{SS}	F12	V_{SS}	K34	$\overline{HSYNC1}$
B22	$\overline{TRG}$	D20	$\overline{CAS0}$	F14	PS0	L1	A0
B24	V_{DD}	D22	FCLK1	F16	V_{SS}	L3	A7
B26	$\overline{DDIN}$	D24	V_{SS}	F18	CT2	L5	V_{SS}
B28	FCLK0	D26	CAREA1	F20	V_{DD}	L31	V_{SS}
B30	V_{DD}	D28	SCLK0	F22	V_{SS}	L33	$\overline{TRST}$
B32	$\overline{CSYNC0}$/$\overline{HBLNK0}$	D30	V_{SS}	F24	V_{DD}	L35	$\overline{XPT1}$

FIGURE 2. Terminal connections.

Device type	01	Device type	01	Device type	01	Device type	01
Case outline	X	Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
M2	V_{DD}	V2	V_{DD}	AD2	V_{DD}	AK2	V_{DD}
M4	V_{SS}	V4	V_{SS}	AD4	V_{SS}	AK4	V_{SS}
M32	V_{SS}	V32	V_{SS}	AD32	V_{SS}	AK8	V_{DD}
M34	V_{DD}	V34	V_{DD}	AD34	V_{DD}	AK10	V_{SS}
N1	V_{DD}	W1	A11	AE1	A15	AK12	V_{DD}
N3	A8	W3	A18	AE3	A26	AK14	V_{SS}
N5	V_{SS}	W5	V_{SS}	AE5	V_{SS}	AK16	V_{DD}
N31	V_{SS}	W31	V_{SS}	AE31	V_{SS}	AK18	NC
N33	TMS	W33	D59	AE33	D51	AK20	V_{SS}
N35	V_{DD}	W35	D63	AE35	D58	AK22	D27
P2	A4	Y2	A12	AF2	A17	AK24	V_{DD}
P4	A9	Y4	A19	AF4	A28	AK26	V_{SS}
P32	TDO	Y32	$\overline{XPT2}$	AF32	D46	AK28	V_{DD}
P34	$\overline{XPT0}$	Y34	D56	AF34	D49	AK32	V_{SS}
R1	V_{SS}	AA1	V_{SS}	AG1	A16	AK34	V_{DD}
R3	V_{DD}	AA3	V_{DD}	AG3	V_{SS}	AL1	A23
R5	V_{DD}	AA5	V_{DD}	AG5	V_{DD}	AL3	A25
R31	V_{DD}	AA31	V_{DD}	AG31	V_{DD}	AL5	V_{SS}
R33	V_{DD}	AA33	V_{DD}	AG33	V_{SS}	AL7	D3
R35	V_{SS}	AA35	V_{SS}	AG35	D57	AL9	D4
T2	A5	AB2	A14	AH2	A20	AL11	D10
T4	A13	AB4	A21	AH4	A30	AL13	V_{SS}
T32	D62	AB32	D55	AH32	D44	AL15	D16
T34	EMU0	AB34	D60	AH34	D54	AL17	D20
U1	V_{DD}	AC1	V_{DD}	AJ1	V_{DD}	AL19	D21
U3	A10	AC3	A22	AJ3	A31	AL21	D24
U5	P53	AC5	V_{SS}	AJ5	V_{SS}	AL23	V_{SS}
U31	NC	AC31	V_{SS}	AJ31	V_{SS}	AL25	D29
U33	D61	AC33	D52	AJ33	D42	AL27	D32
U35	V_{DD}	AC35	V_{DD}	AJ35	V_{DD}	AL29	D38

FIGURE 2. Terminal connection - Continued.

Device type	01	Device type	01	Device type	01
Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
AL31	V_{SS}	AN25	D37	AR25	V_{SS}
AL33	D48	AN27	V_{SS}	AR27	D40
AL35	D53	AN29	D35	AR29	V_{DD}
AM2	A24	AN31	D45	AR31	D43
AM4	V_{DD}	AN33	V_{DD}		
AM6	V_{SS}	AP4	A27	Top Side Capacitor Pads	
AM8	D2	AP6	V_{DD}	CP1	V_{SSD} V_{DDD}
AM10	D6	AP8	D5	CP2	V_{SSI} V_{DDI}
AM12	V_{DD}	AP10	D8	CP3	V_{DDD} V_{SSD}
AM14	D14	AP12	V_{DD}	CP4	V_{DDC} V_{SSC}
AM16	D19	AP14	D13	CP5	V_{DDD} V_{SSD}
AM18	V_{SS}	AP16	D17	CP6	V_{DDI} V_{SSI}
AM20	D23	AP18	V_{DD}	CP7	V_{SSD} V_{DDD}
AM22	D25	AP20	D26	CP8	V_{SSI} V_{DDI}
AM24	V_{SS}	AP22	D34		
AM26	D31	AP24	V_{DD}		
AM28	D33	AP26	D39		
AM30	V_{SS}	AP28	D41		
AM32	V_{DD}	AP30	V_{DD}		
AM34	D50	AP32	D47		
AN5	A29	AR5	D0		
AN7	D1	AR7	V_{DD}		
AN9	V_{SS}	AR9	D7		
AN11	D9	AR11	V_{SS}		
AN13	D12	AR13	D11		
AN15	V_{DD}	AR15	D15		
AN17	D18	AR17	V_{SS}		
AN19	D22	AR19	V_{DD}		
AN21	V_{DD}	AR21	D30		
AN23	D28	AR23	D36		

FIGURE 2. Terminal connection - Continued.

Device type	01	Device type	01	Device type	01	Device type	01
Case outline	Y	Case outline	Y	Case outline	Y	Case outline	Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	STATUS(3)	31	V_{DD}	61	V_{DD}	91	V_{DD}
2	V_{SS}	32	V_{SS}	62	V_{DD}	92	$\overline{CSYNC0}$/$\overline{HBLNK0}$
3	STATUS(2)	33	V_{DD}	63	W	93	$\overline{VSYNCT}$
4	STATUS(1)	34	V_{SS}	64	STATUS(5)	94	$\overline{VSYNC0}$
5	V_{DD}	35	V_{SS}	65	V_{DD}	95	V_{SS}
6	STATUS(0)	36	UCLK	66	DSF1	96	V_{SS}
7	AS(2)	37	V_{SS}	67	V_{SS}	97	$\overline{HSYNCT}$
8	AS(1)	38	$\overline{CAS}$(7)	68	$\overline{DBEN}$	98	V_{DD}
9	AS(0)	39	V_{DD}	69	V_{DD}	99	V_{DD}
10	$\overline{FAULT}$	40	V_{DD}	70	$\overline{DDTN}$	100	V_{DD}
11	READY	41	$\overline{CAS}$(6)	71	CLKOUT	101	$\overline{HSYNC0}$
12	$\overline{RETRY}$	42	V_{SS}	72	CAREA1	102	$\overline{TRST}$
13	$\overline{UTIME}$	43	$\overline{CAS}$(5)	73	V_{SS}	103	TCK
14	BS(1)	44	V_{DD}	74	SCLK1	104	TMS
15	BS(0)	45	$\overline{CAS}$(4)	75	V_{DD}	105	TDI
16	CT(1)	46	$\overline{CAS}$(3)	76	FCLK0	106	TDO
17	CT(0)	47	CT(2)	77	V_{SS}	107	EMU1
18	PS(2)	48	$\overline{CAS}$(2)	78	SCLK0	108	$\overline{XPT0}$
19	PS(1)	49	V_{SS}	79	V_{DD}	109	$\overline{XPT1}$
20	PS(0)	50	$\overline{CAS}$(1)	80	CAREA0	110	V_{SS}
21	V_{DD}	51	V_{DD}	81	$\overline{ETNT4}$	111	V_{SS}
22	$\overline{RESET}$	52	$\overline{CAS}$(0)	82	$\overline{ETNT3}$	112	EMU0
23	V_{SS}	53	$\overline{RL}$	83	$\overline{ETNT2}$	113	V_{DD}
24	$\overline{HREQ}$	54	$\overline{RAS}$	84	$\overline{ETNT1}$	114	D(63)
25	$\overline{HACK}$	55	V_{SS}	85	$\overline{CBLNKT}$/$\overline{VBLNKT}$	115	D(62)
26	V_{SS}	56	V_{SS}	86	$\overline{CBLNK0}$/$\overline{VBLNK0}$	116	V_{SS}
27	V_{SS}	57	V_{SS}	87	V_{SS}	117	D(61)
28	REQ(1)	58	$\overline{TRG}$	88	V_{SS}	118	V_{SS}
29	REQ(0)	59	V_{DD}	89	$\overline{CSYNCT}$/$\overline{HBLNKT}$	119	D(60)
30	V_{DD}	60	FCLK1	90	V_{DD}	120	V_{DD}

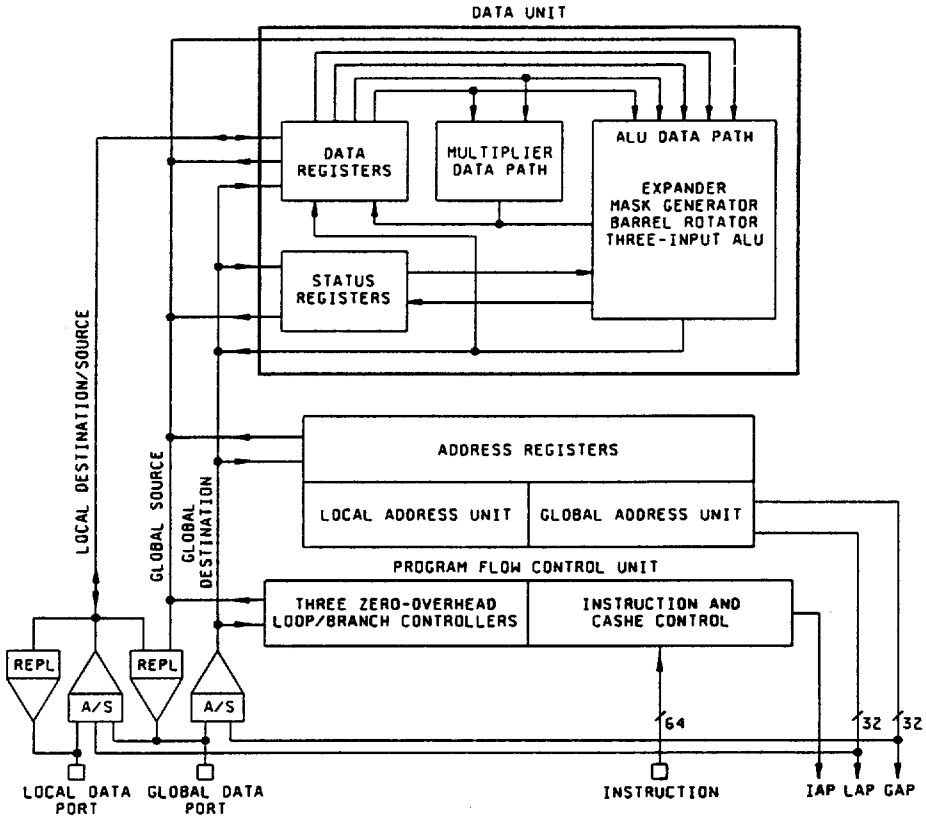
FIGURE 2. Terminal connections.

Device type	01	Device type	01	Device type	01	Device type	01
Case outline	Y	Case outline	Y	Case outline	Y	Case outline	Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
121	V_{DD}	151	D(46)	181	D(30)	211	D(16)
122	D(59)	152	D(45)	182	D(29)	212	V_{DD}
123	V_{SS}	153	V_{SS}	183	V_{SS}	213	D(15)
124	D(58)	154	V_{SS}	184	V_{SS}	214	D(14)
125	V_{DD}	155	D(44)	185	V_{SS}	215	D(13)
126	D(57)	156	V_{DD}	186	D(28)	216	V_{SS}
127	$\overline{XPT2}$	157	V_{DD}	187	V_{DD}	217	V_{DD}
128	V_{SS}	158	V_{DD}	188	V_{DD}	218	D(12)
129	D(56)	159	D(43)	189	D(27)	219	V_{DD}
130	V_{DD}	160	D(42)	190	D(26)	220	V_{DD}
131	V_{DD}	161	D(41)	191	D(25)	221	V_{DD}
132	D(55)	162	V_{SS}	192	V_{SS}	222	D(11)
133	V_{SS}	163	V_{SS}	193	D(24)	223	D(10)
134	D(54)	164	D(40)	194	V_{DD}	224	D(9)
135	V_{DD}	165	V_{DD}	195	V_{DD}	225	V_{SS}
136	D(53)	166	D(39)	196	D(23)	226	D(8)
137	V_{SS}	167	D(38)	197	D(22)	227	V_{DD}
138	V_{SS}	168	D(37)	198	V_{SS}	228	V_{DD}
139	D(52)	169	V_{SS}	199	D(21)	229	D(7)
140	V_{DD}	170	D(35)	200	V_{SS}	230	D(6)
141	D(51)	171	V_{SS}	201	D(20)	231	D(5)
142	D(50)	172	V_{DD}	202	V_{DD}	232	V_{SS}
143	D(49)	173	D(35)	203	V_{DD}	233	V_{SS}
144	V_{SS}	174	D(34)	204	D(19)	234	D(4)
145	V_{SS}	175	D(33)	205	V_{DD}	235	V_{DD}
146	D(48)	176	V_{SS}	206	D(18)	236	D(3)
147	V_{DD}	177	D(32)	207	V_{SS}	237	D(2)
148	V_{DD}	178	V_{DD}	208	D(17)	238	V_{SS}
149	V_{DD}	179	V_{DD}	209	V_{SS}	239	D(1)
150	D(47)	180	D(31)	210	V_{SS}	240	V_{SS}

FIGURE 2. Terminal connection - Continued.

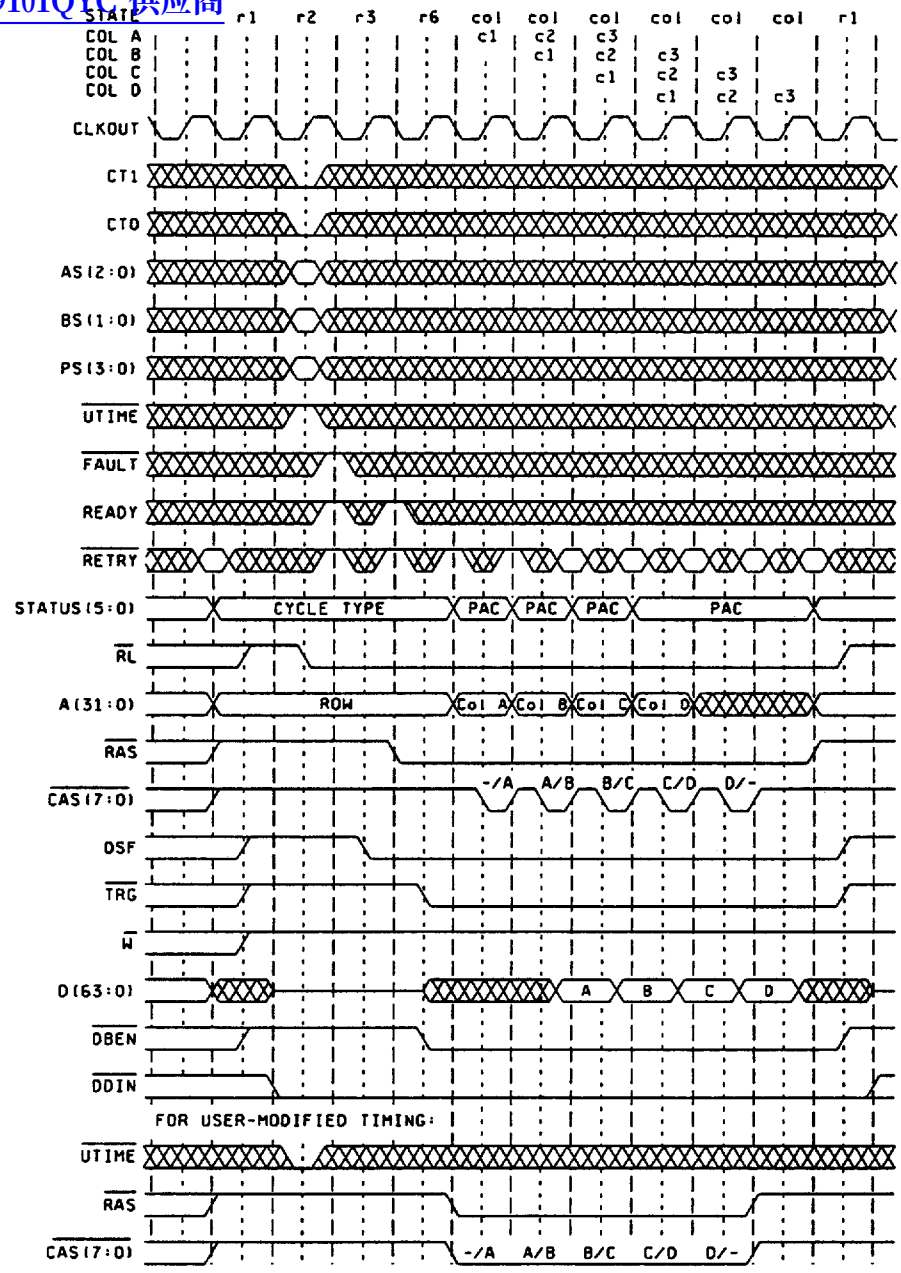
Device type	01	Device type	01	Device type	01
Case outline	Y	Case outline	Y	Case outline	Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
241	D(0)	271	V_{DD}	301	V_{DD}
242	V_{DD}	272	V_{DD}	302	A(7)
243	V_{DD}	273	A(19)	303	A(6)
244	A(31)	274	V_{SS}	304	V_{SS}
245	V_{SS}	275	A(18)	305	V_{SS}
246	A(30)	276	A(17)	306	A(5)
247	A(29)	277	V_{SS}	307	V_{SS}
248	V_{SS}	278	V_{SS}	308	A(4)
248	V_{SS}	279	V_{SS}	309	V_{DD}
250	A(28)	280	A(16)	310	V_{DD}
251	V_{DD}	281	V_{DD}	311	V_{DD}
252	V_{DD}	282	V_{DD}	312	A(3)
253	V_{DD}	283	V_{DD}	313	V_{DD}
254	A(27)	284	A(15)	314	A(2)
255	A(26)	285	PS(3)	315	V_{SS}
256	A(25)	286	A(14)	316	A(1)
257	V_{SS}	287	V_{SS}	317	A(0)
258	V_{SS}	288	V_{DD}	318	V_{DD}
259	V_{SS}	289	A(13)	319	STATUS(4)
260	A(24)	290	V_{SS}	320	V_{SS}
261	V_{DD}	291	V_{SS}		
262	V_{DD}	292	A(12)		
263	V_{DD}	293	V_{DD}		
264	A(23)	294	A(11)		
265	A(22)	295	V_{SS}		
266	V_{DD}	296	A(10)		
267	A(21)	297	V_{DD}		
268	V_{SS}	298	A(9)		
269	V_{SS}	299	V_{SS}		
270	A(20)	300	A(8)		

FIGURE 2. Terminal connection - Continued.



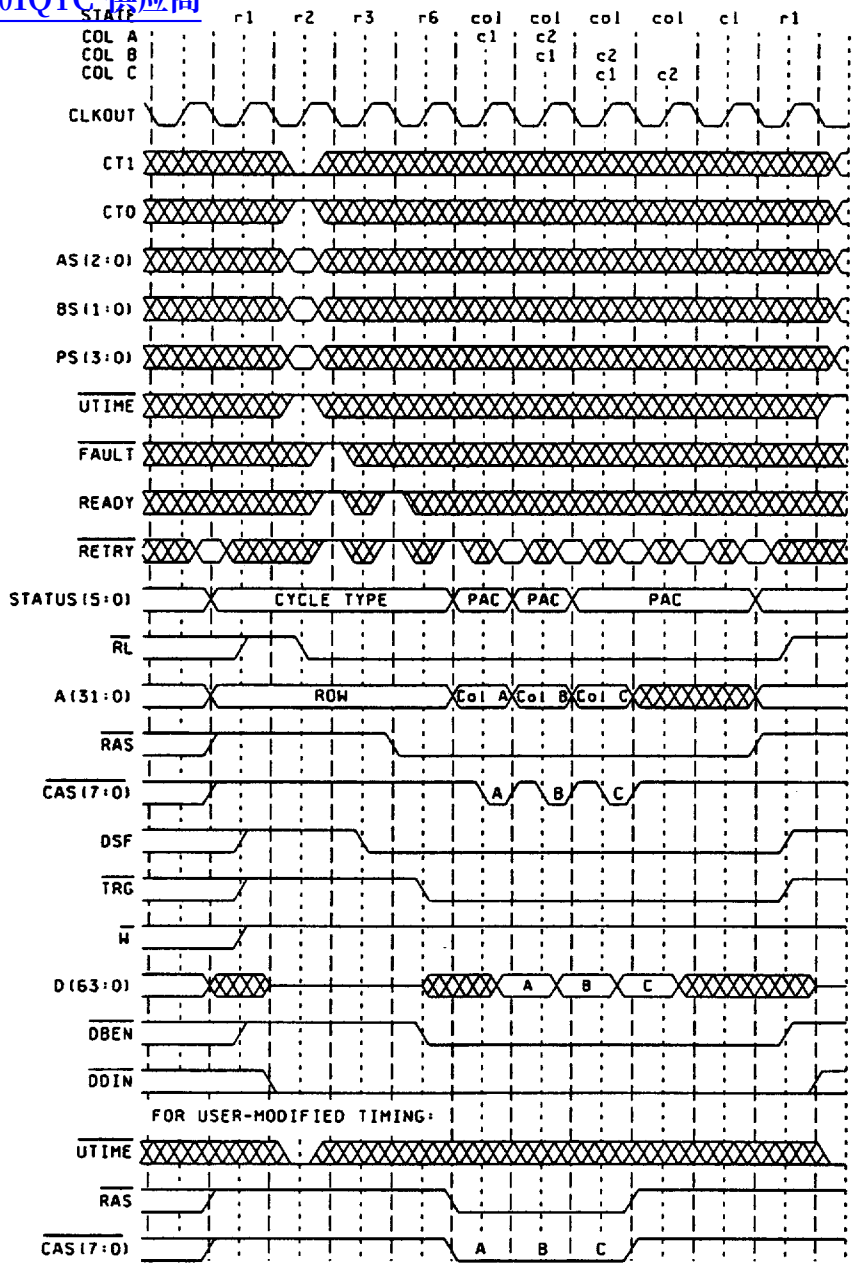
NOTE:
IAP = Instruction address port
LAP = Local address port
GAP = Global address port
REPL = Replicate hardware
A/S = Align-/sign-extend hardware

FIGURE 3. Block diagram.



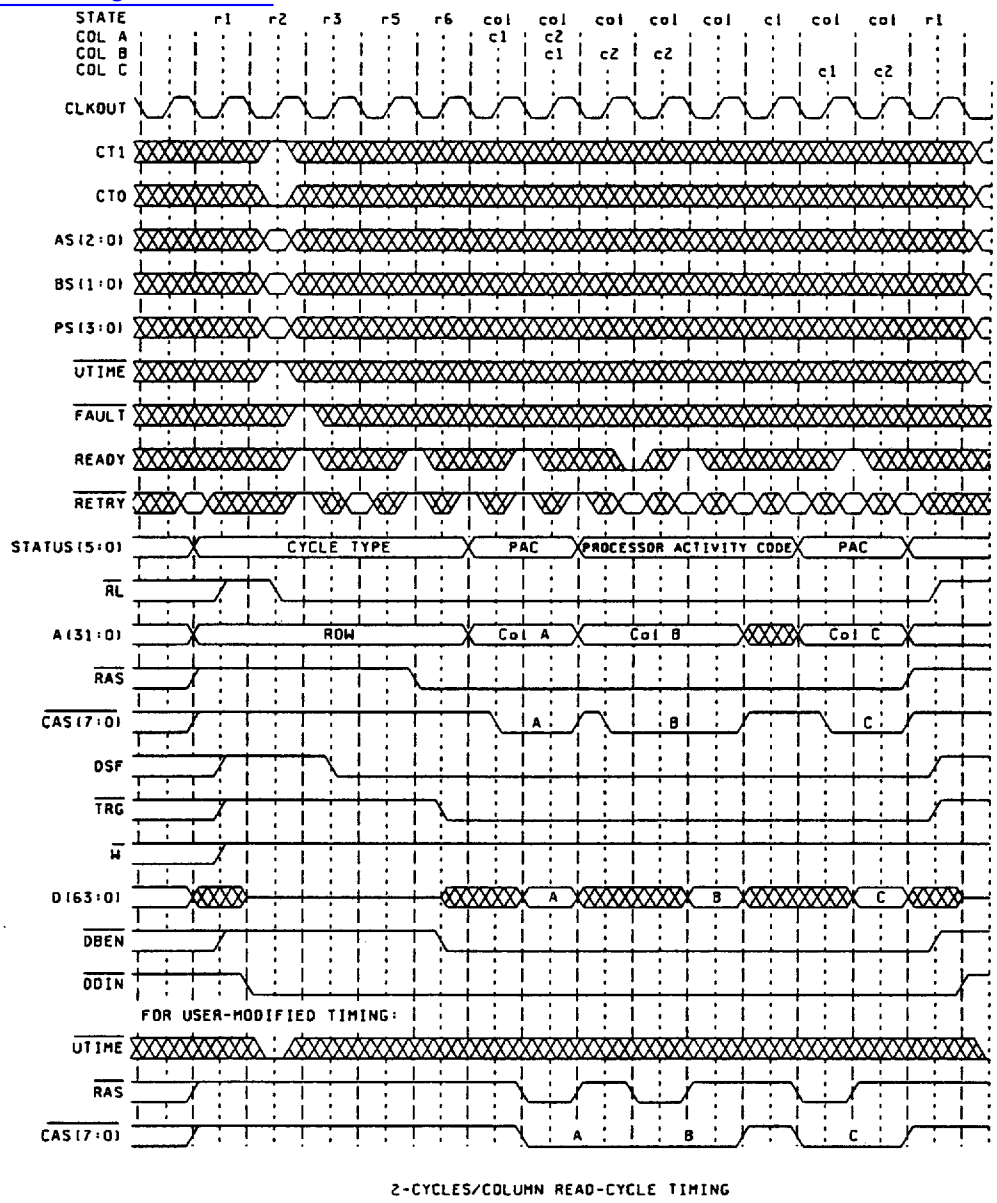
PIPELINED 1-CYCLE/COLUMN READ-CYCLE TIMING

FIGURE 4. Timing waveforms.



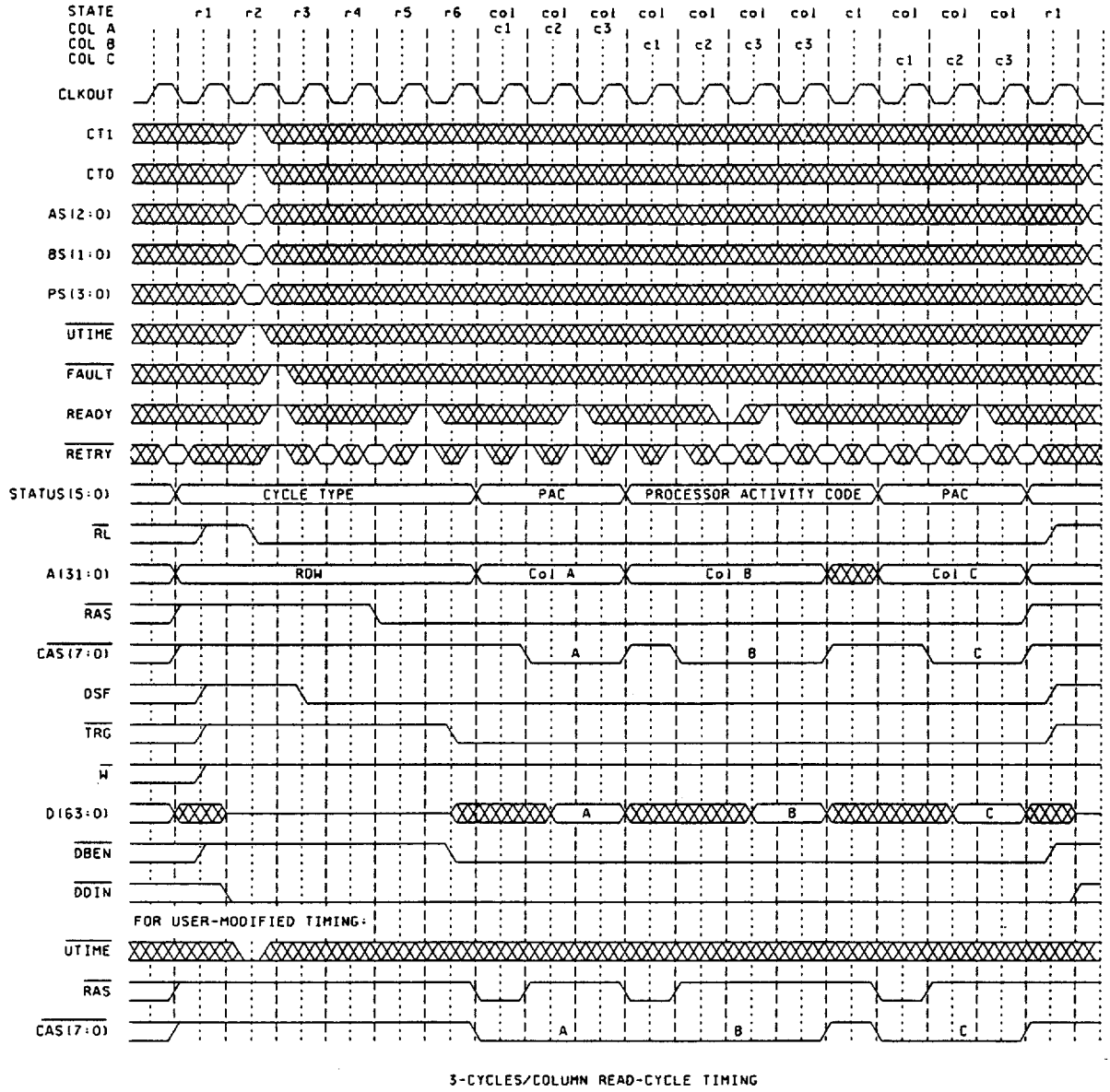
NONPIPELINED 1-CYCLE/COLUMN READ-CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



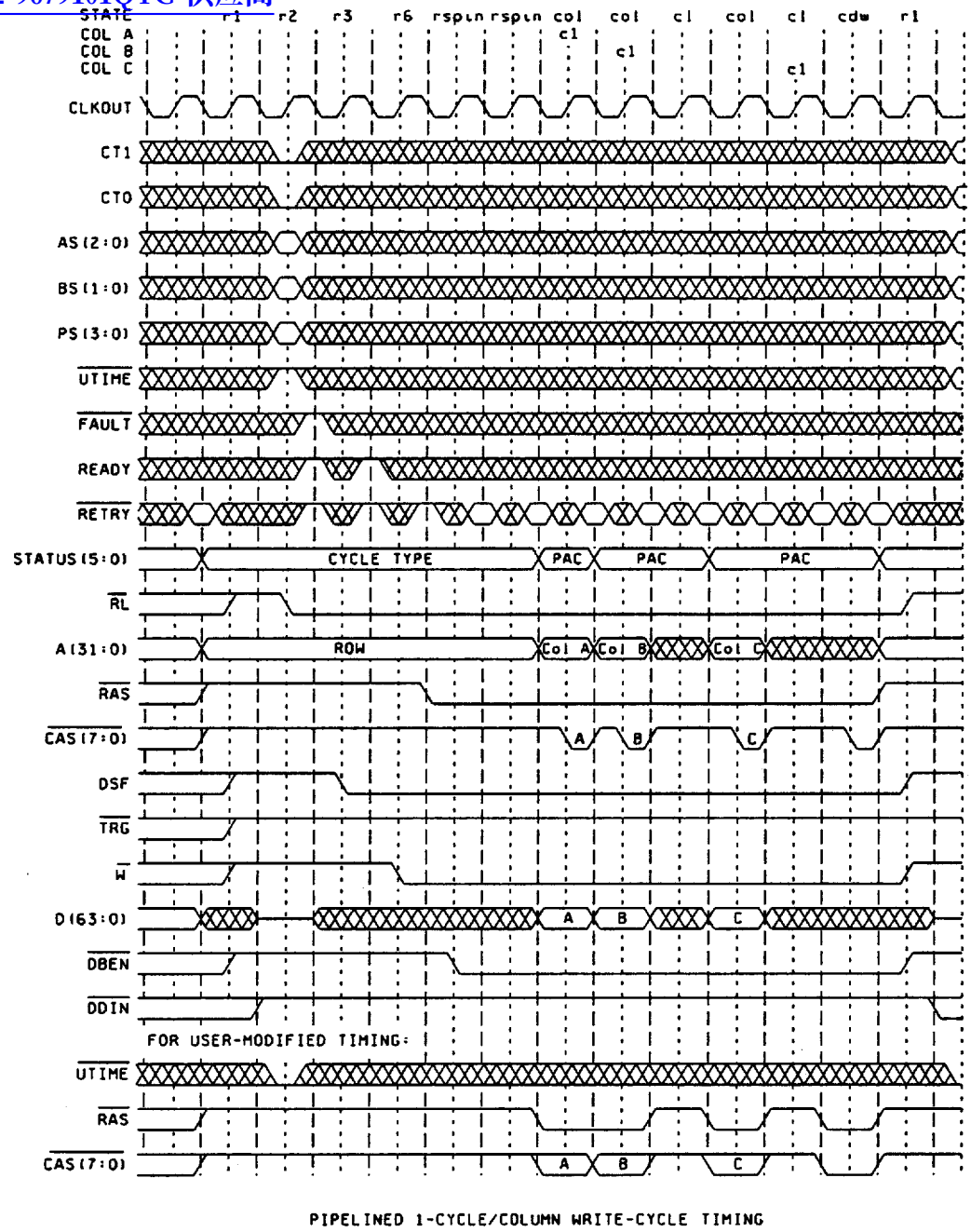
2-CYCLES/COLUMN READ-CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



3-CYCLES/COLUMN READ-CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



PIPELINED 1-CYCLE/COLUMN WRITE-CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.

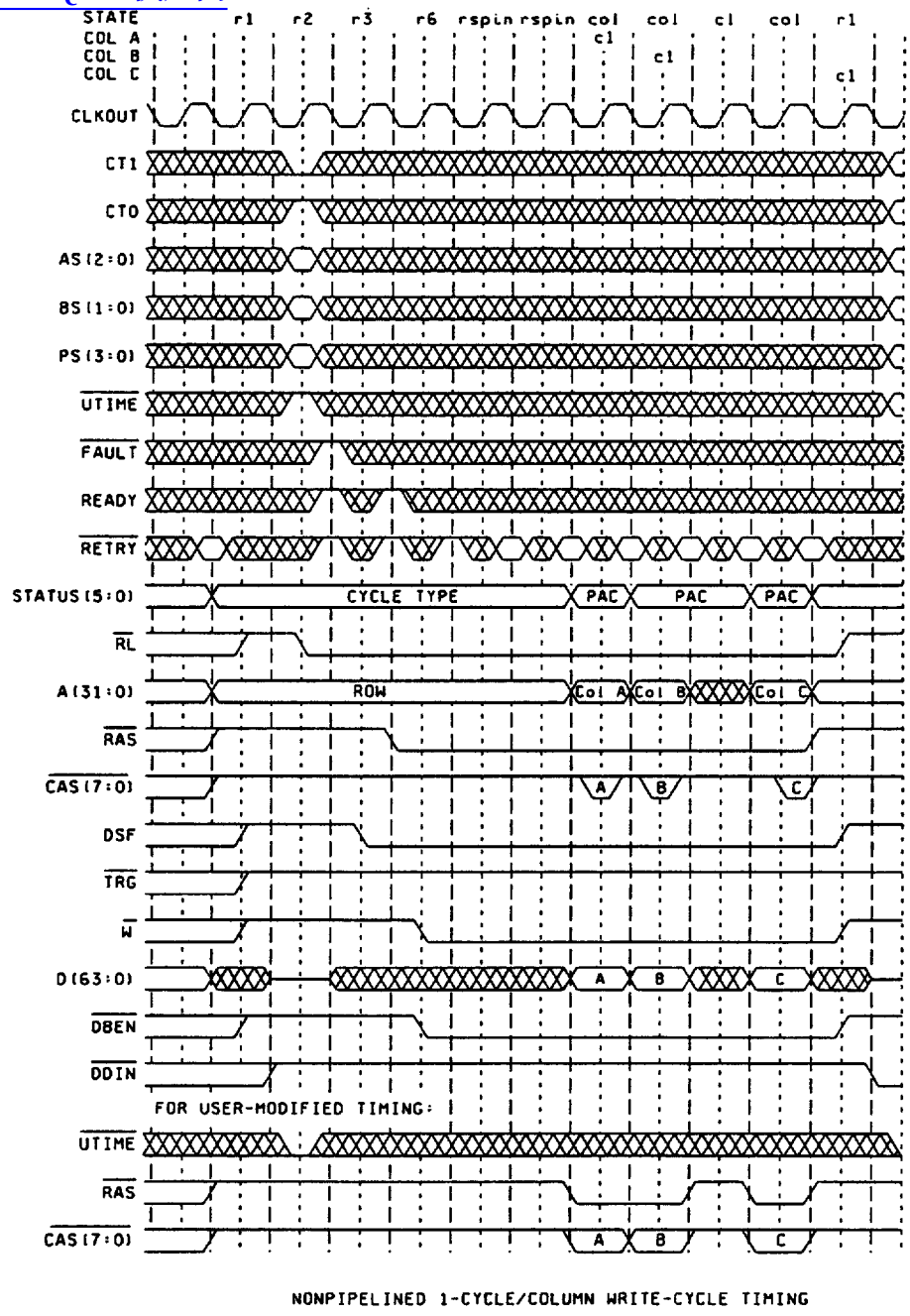


FIGURE 4. Timing waveforms - Continued.

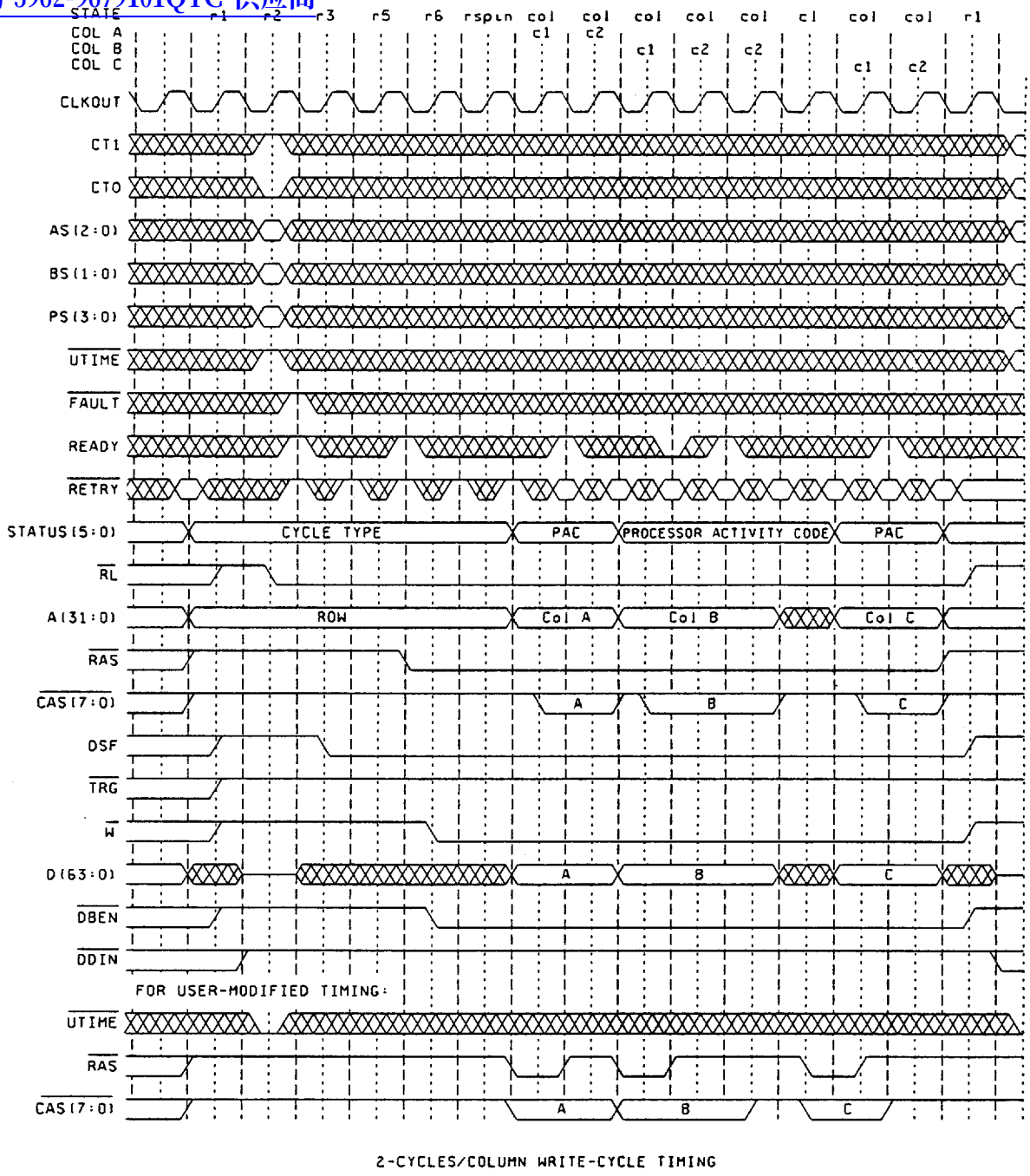
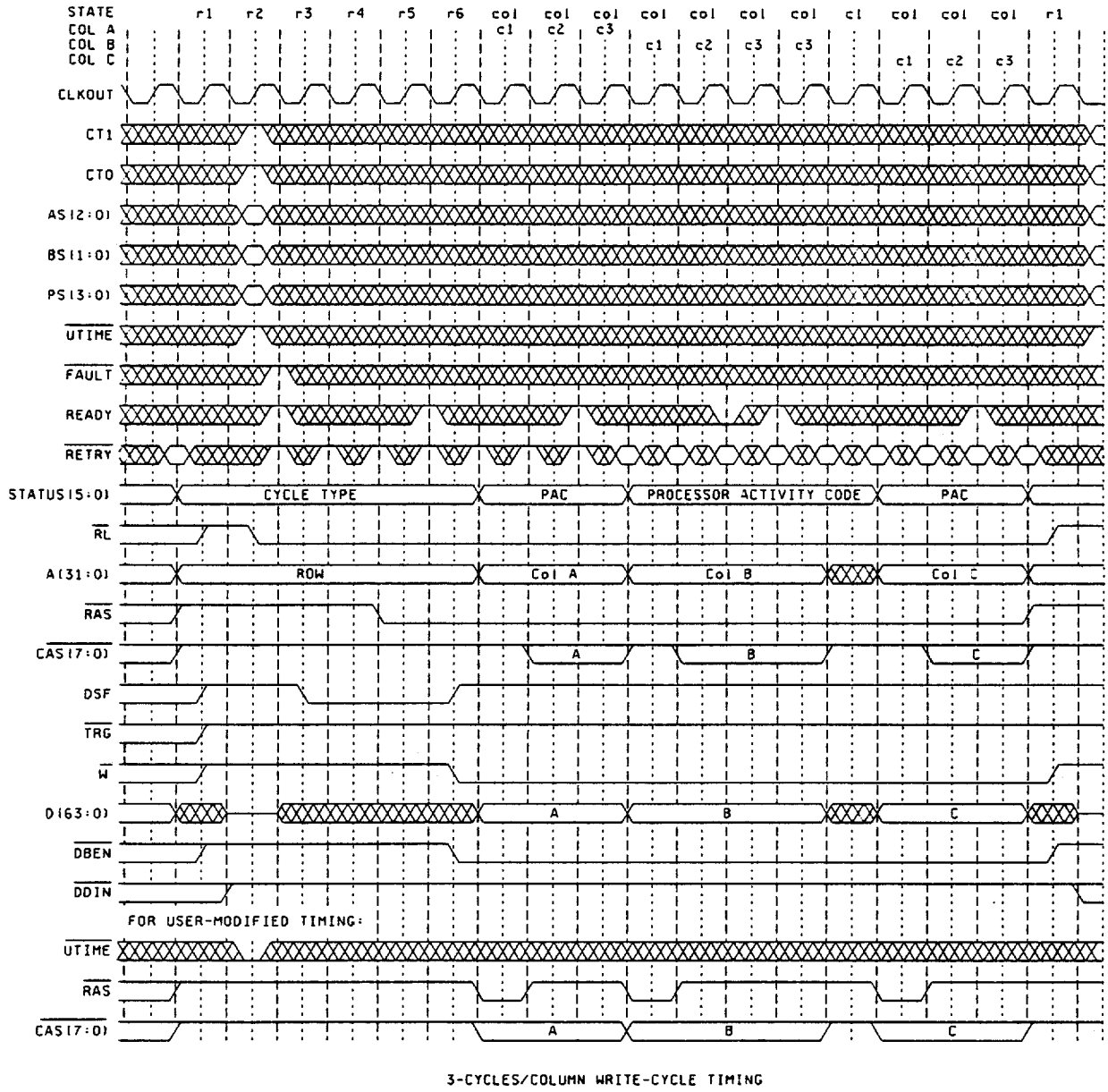
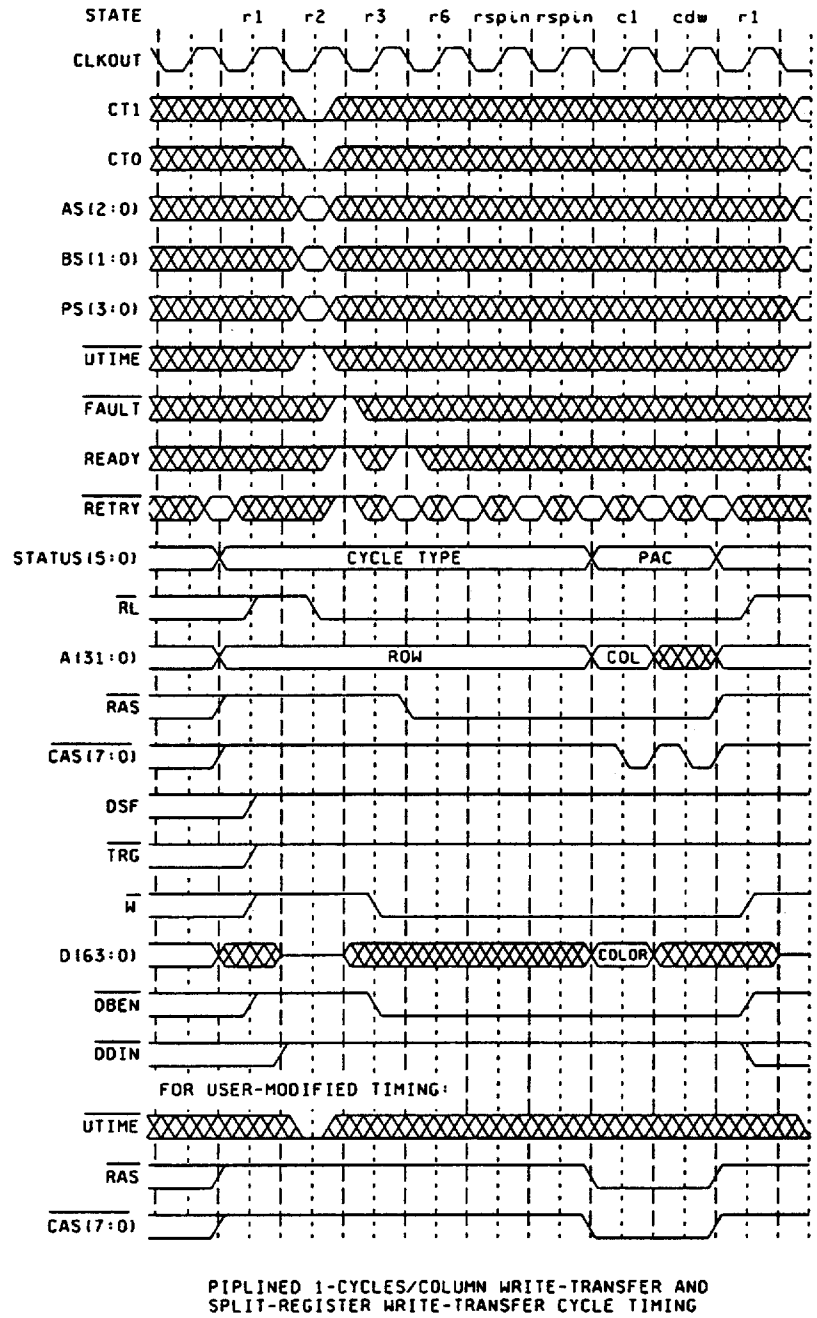


FIGURE 4. Timing waveforms - Continued.



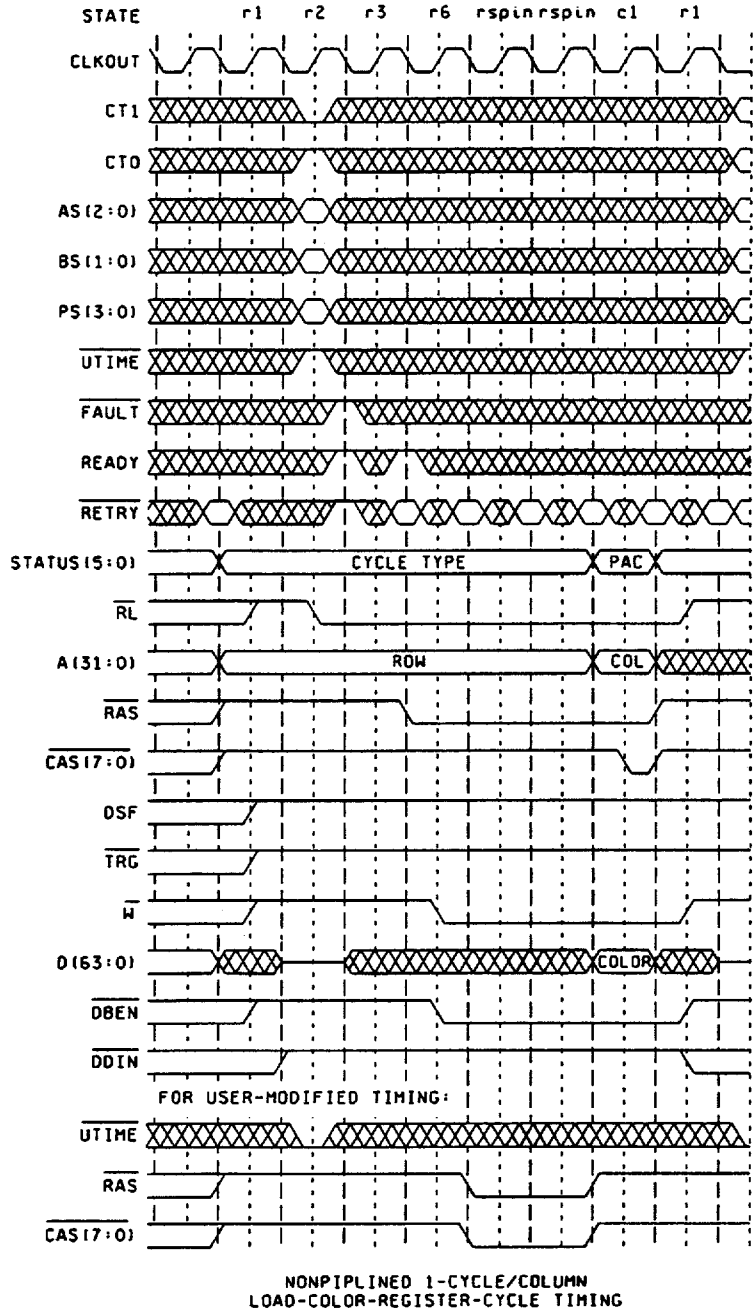
3-CYCLES/COLUMN WRITE-CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



PIPLINED 1-CYCLES/COLUMN WRITE-TRANSFER AND
SPLIT-REGISTER WRITE-TRANSFER CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



NONPIPLINED 1-CYCLE/COLUMN
LOAD-COLOR-REGISTER-CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.

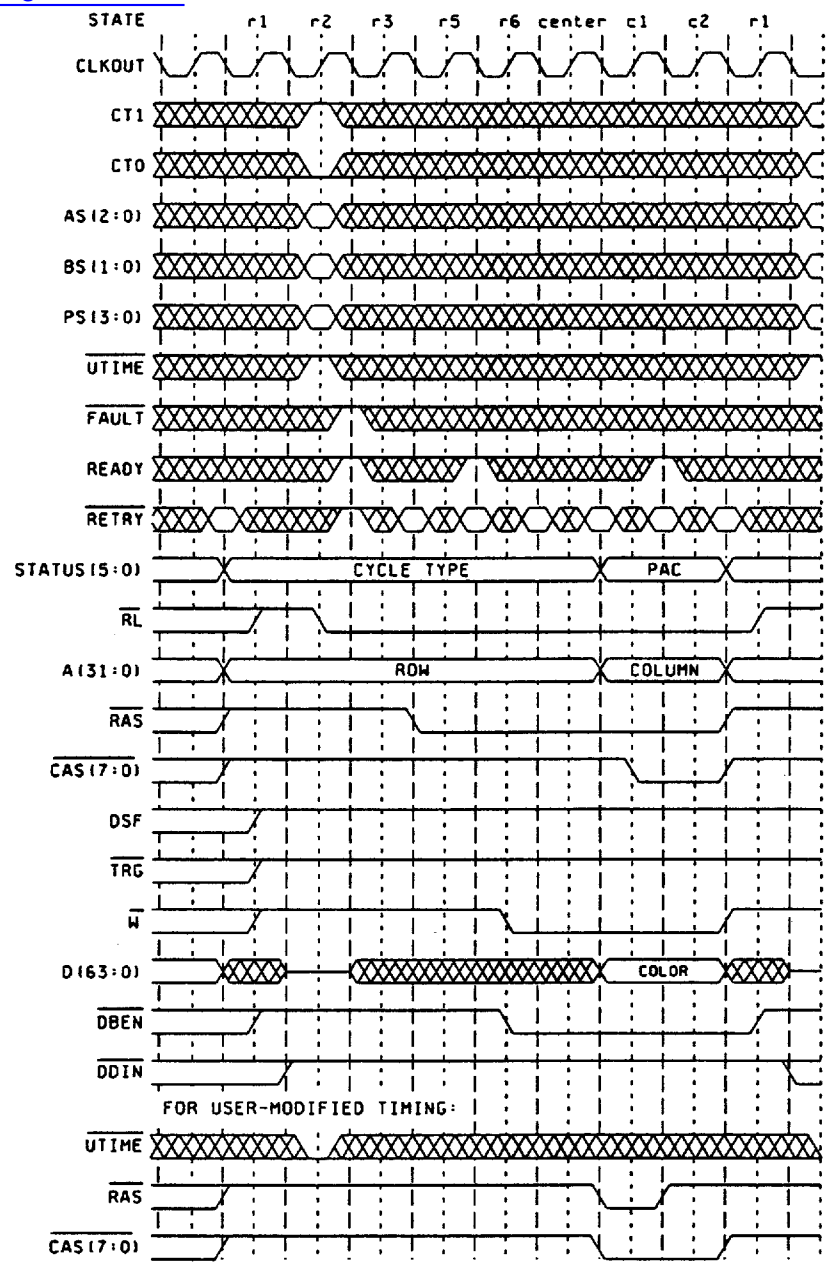
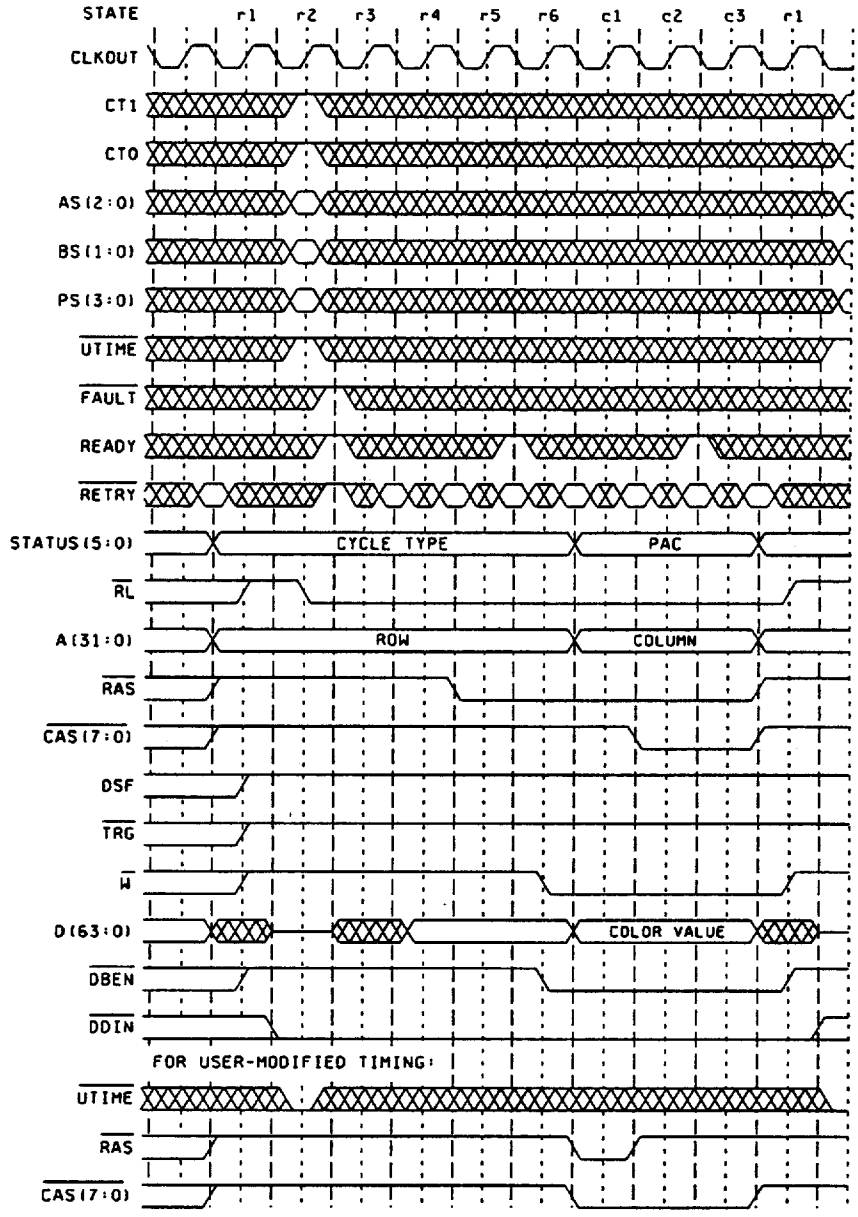


FIGURE 4. Timing waveforms - Continued.



3 CYCLES/COLUMN LOAD-COLOR-REGISTER-CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.

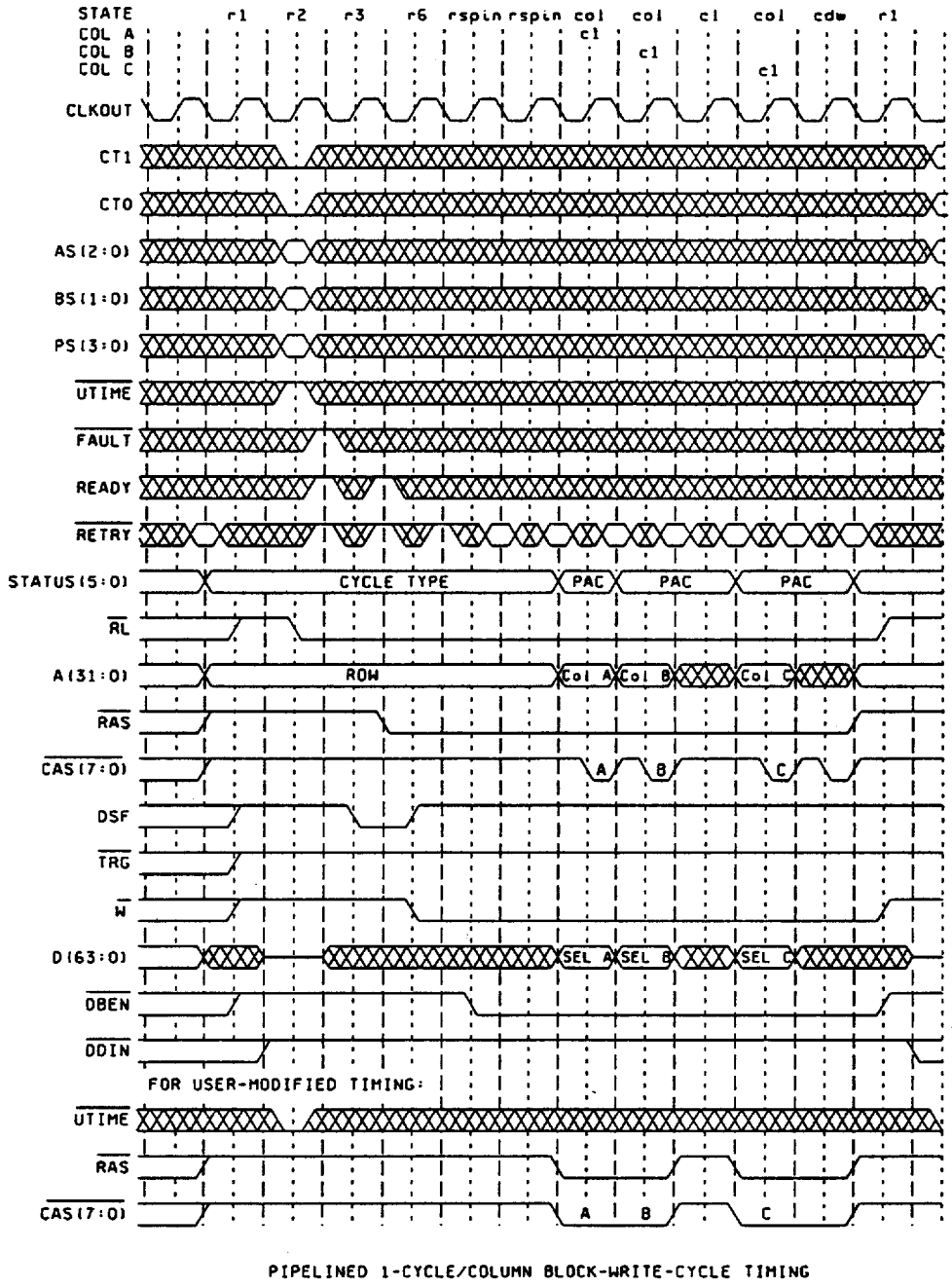


FIGURE 4. Timing waveforms - Continued.

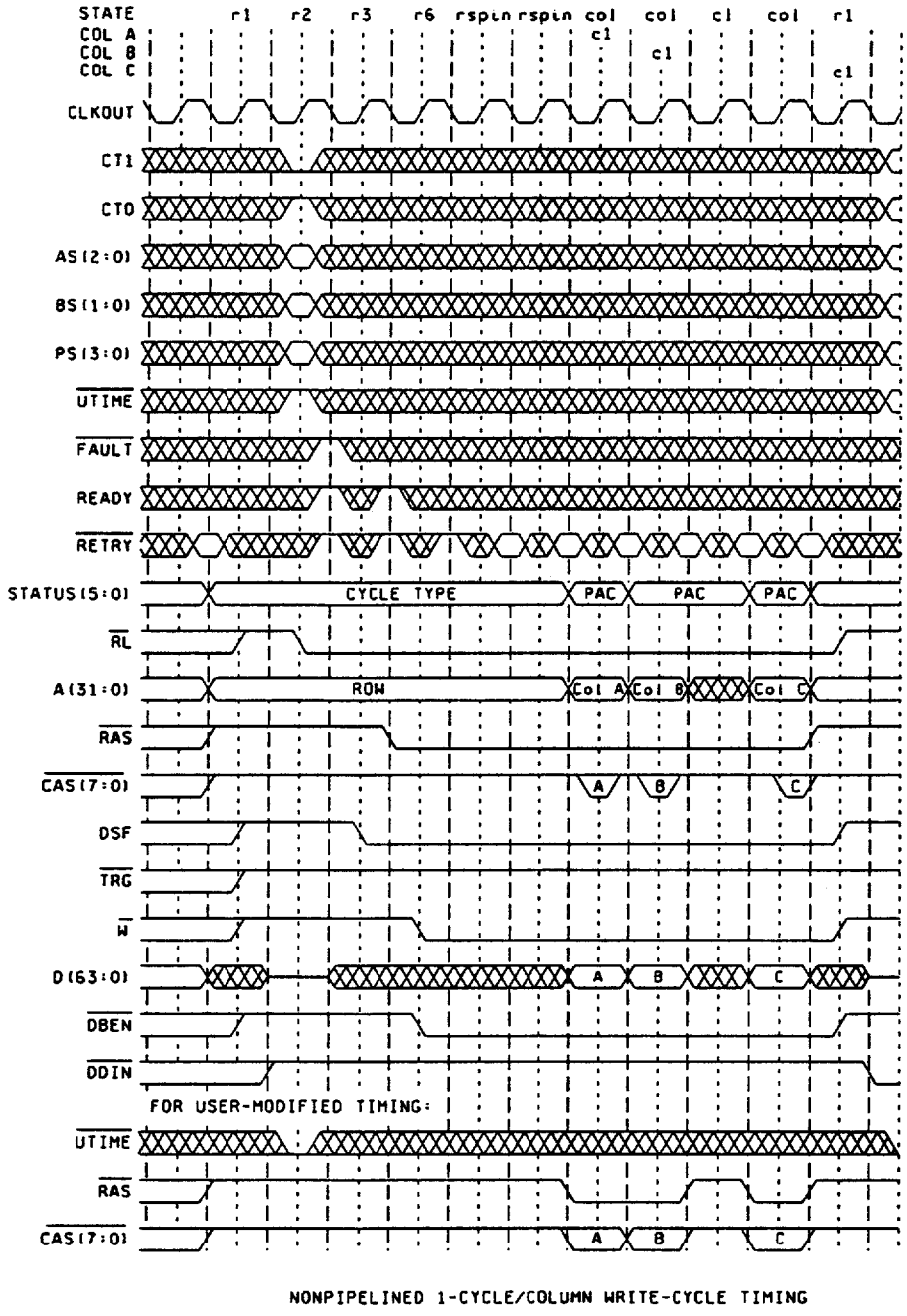
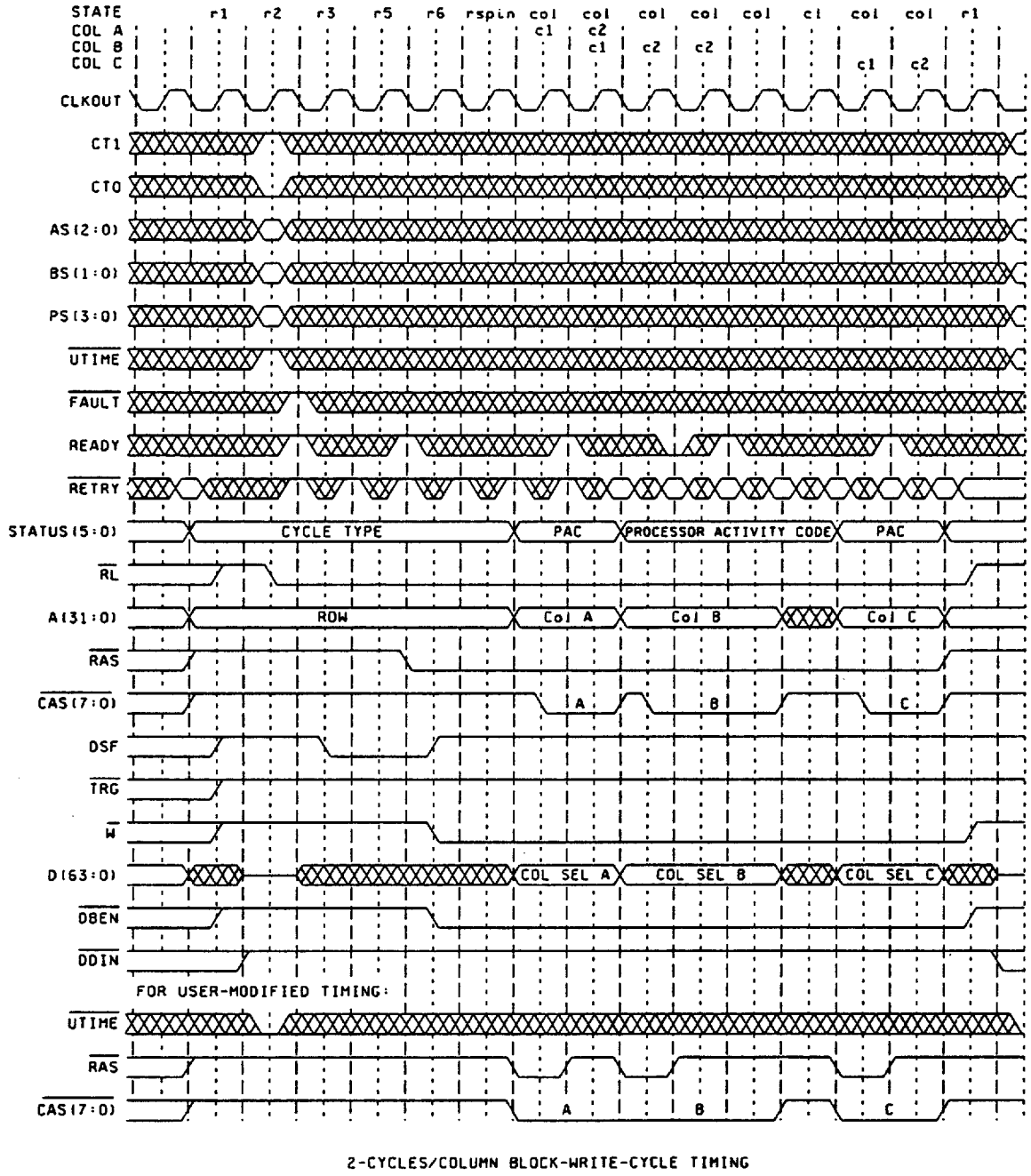


FIGURE 4. Timing waveforms - Continued.



2-CYCLES/COLUMN BLOCK-WRITE-CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.

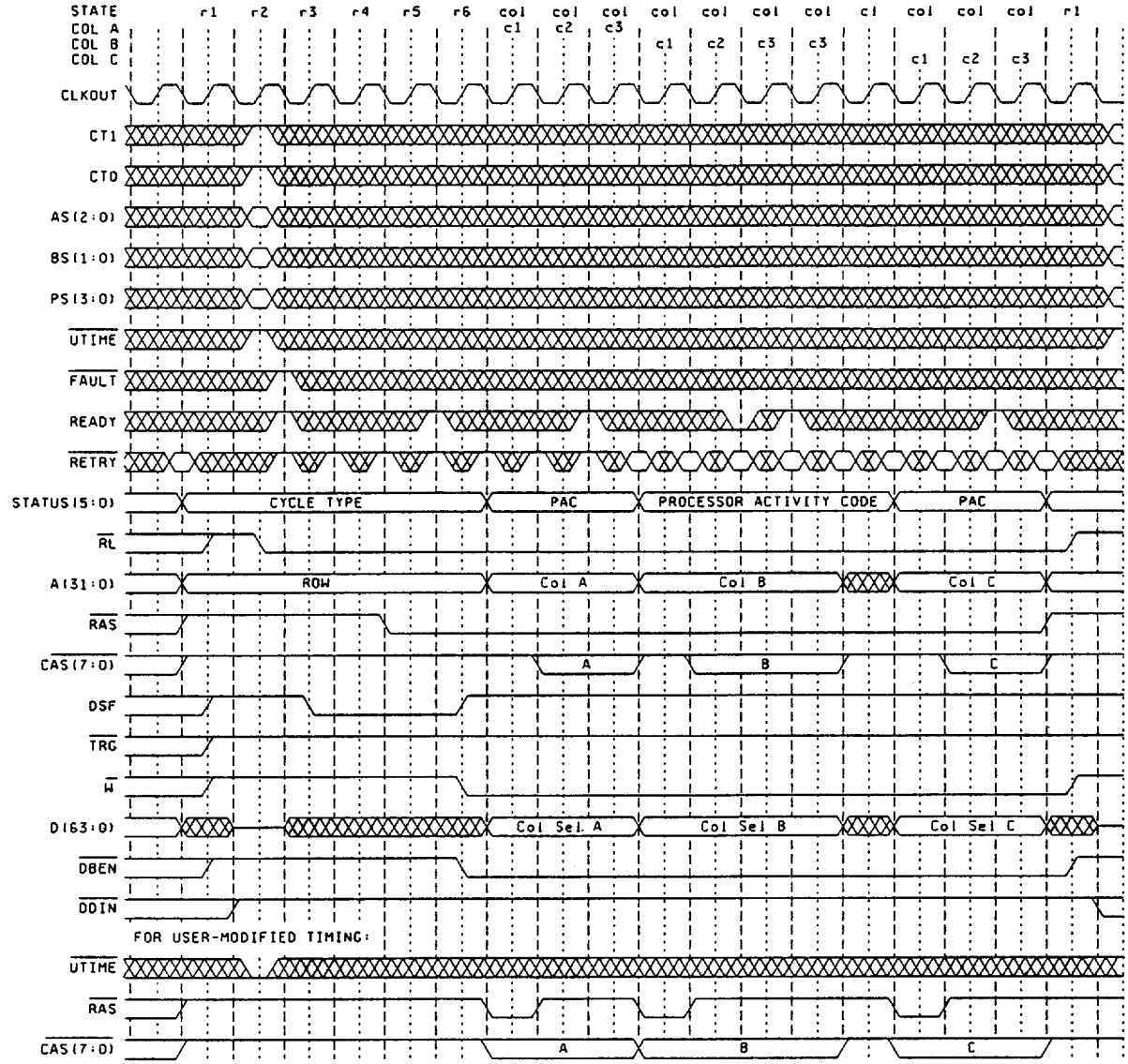
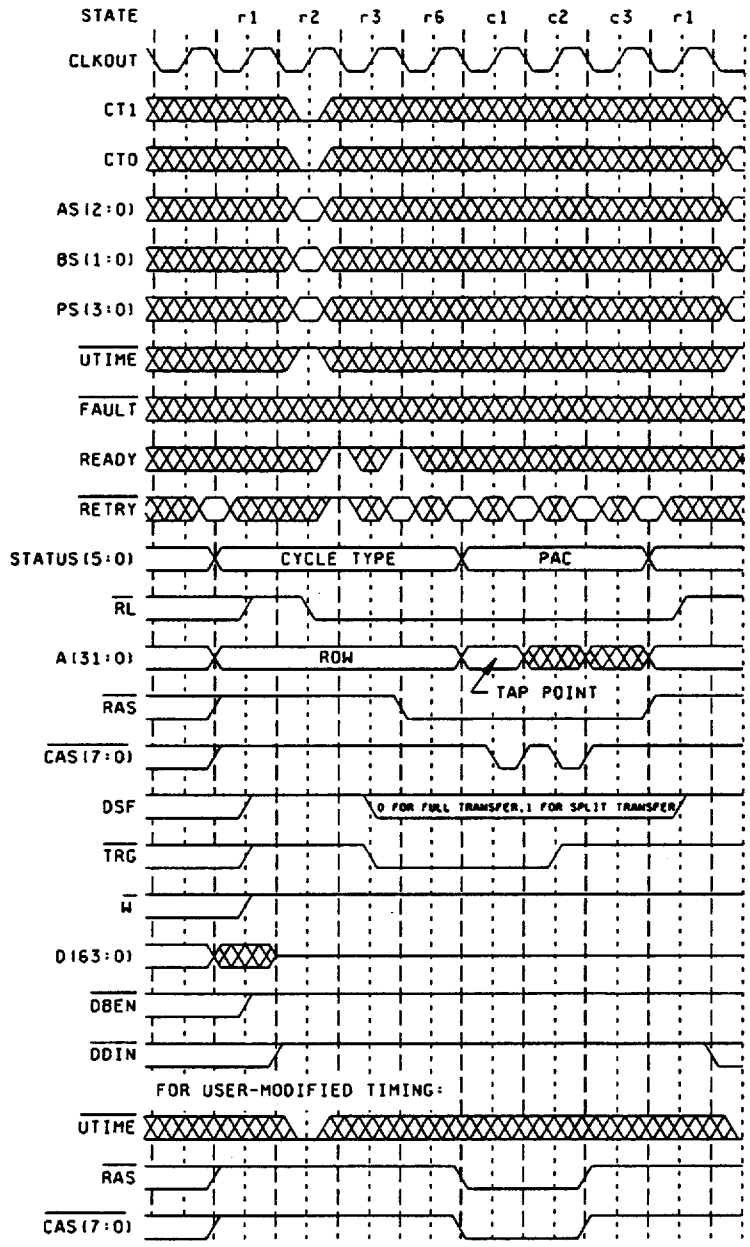
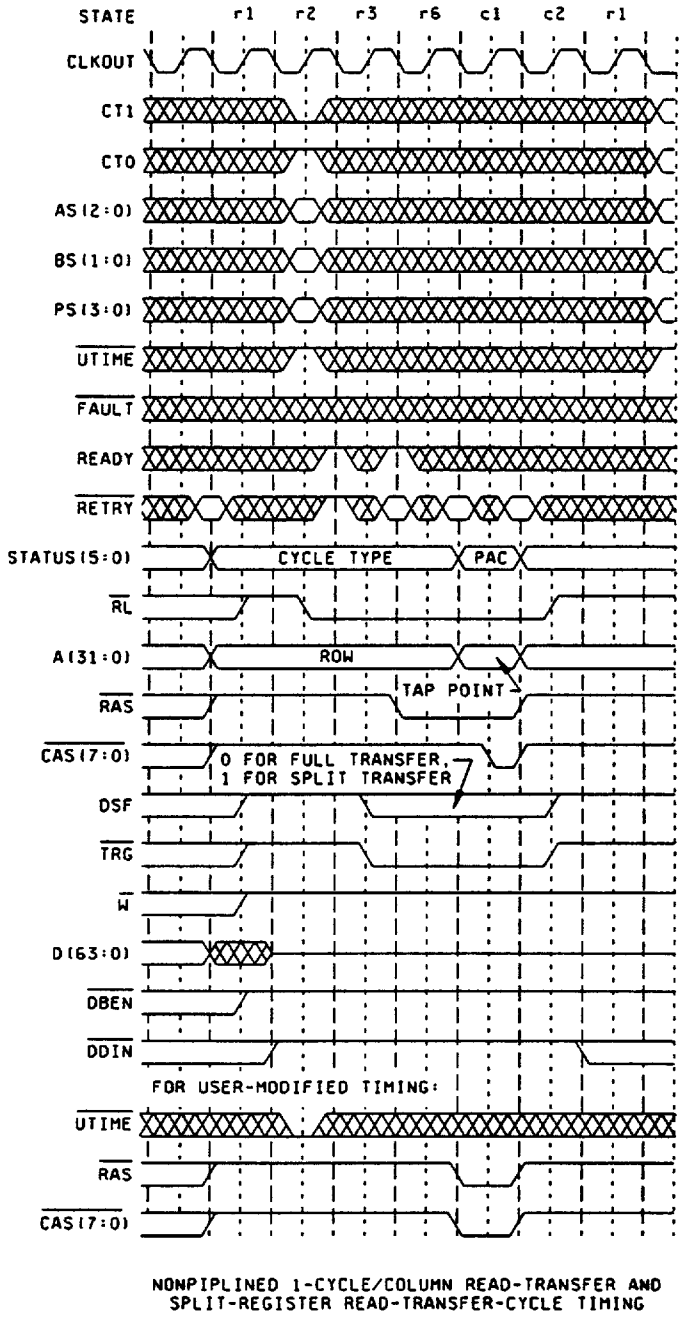


FIGURE 4. Timing waveforms - Continued.



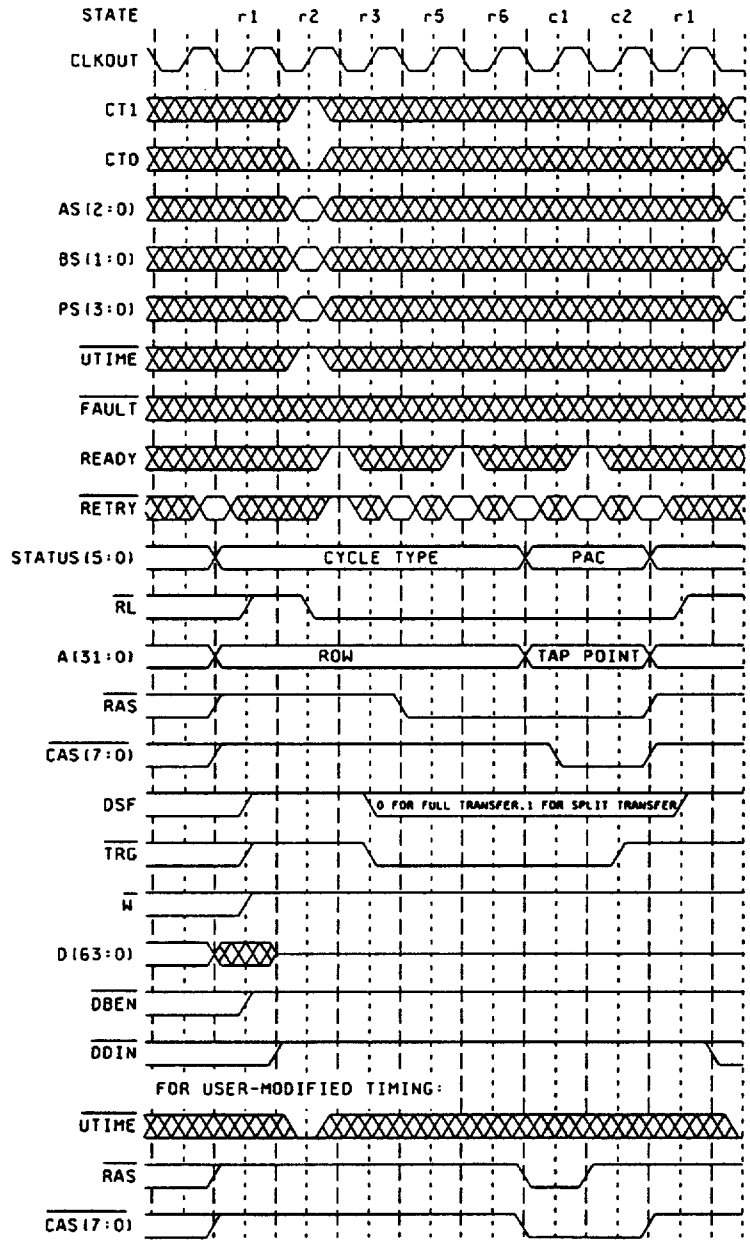
PIPLINED 1-CYCLE/COLUMN READ-TRANSFER AND
SPLIT-REGISTER READ-TRANSFER CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



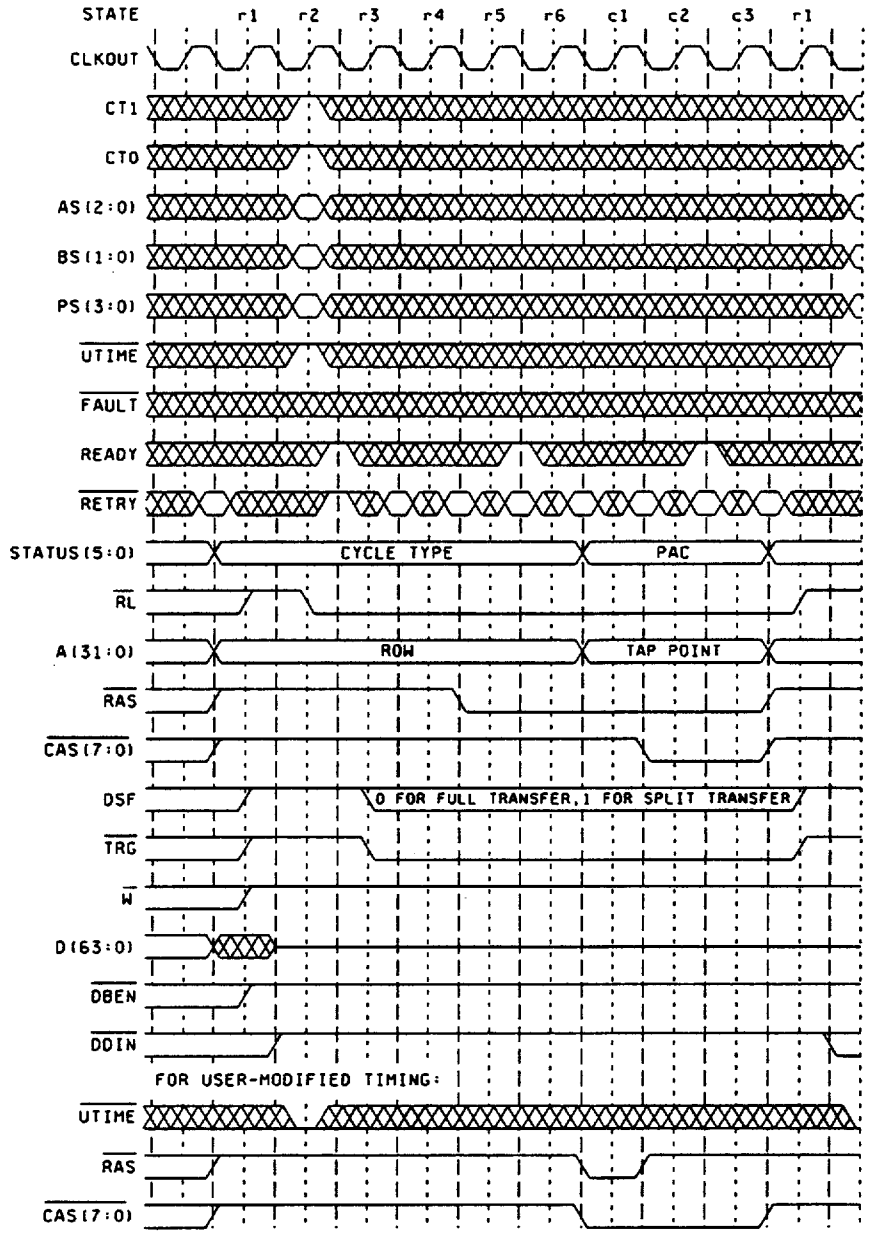
NONPIPLINED 1-CYCLE/COLUMN READ-TRANSFER AND SPLIT-REGISTER READ-TRANSFER-CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



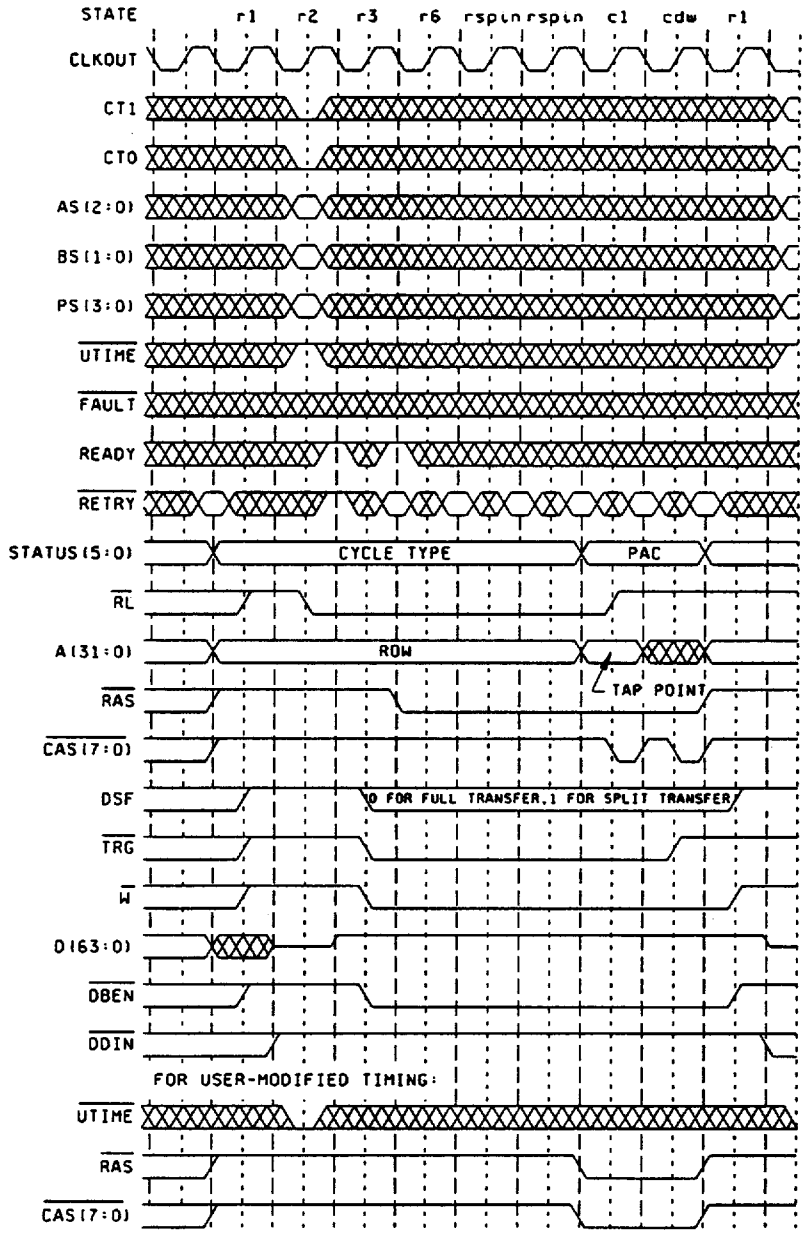
2-CYCLES/COLUMN READ-TRANSFER AND
SPLIT-REGISTER READ-TRANSFER-CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



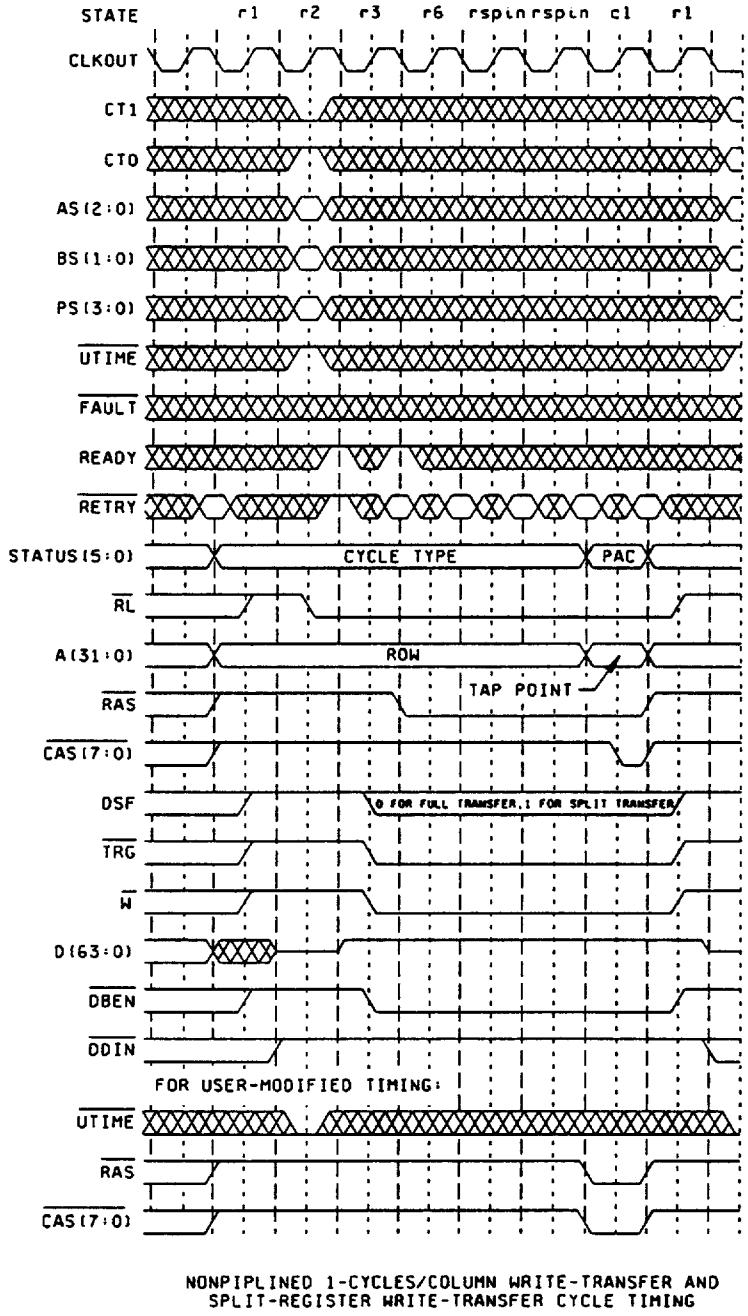
3 CYCLES/COLUMN READ-TRANSFER AND SPLIT-REGISTER READ-TRANSFER CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



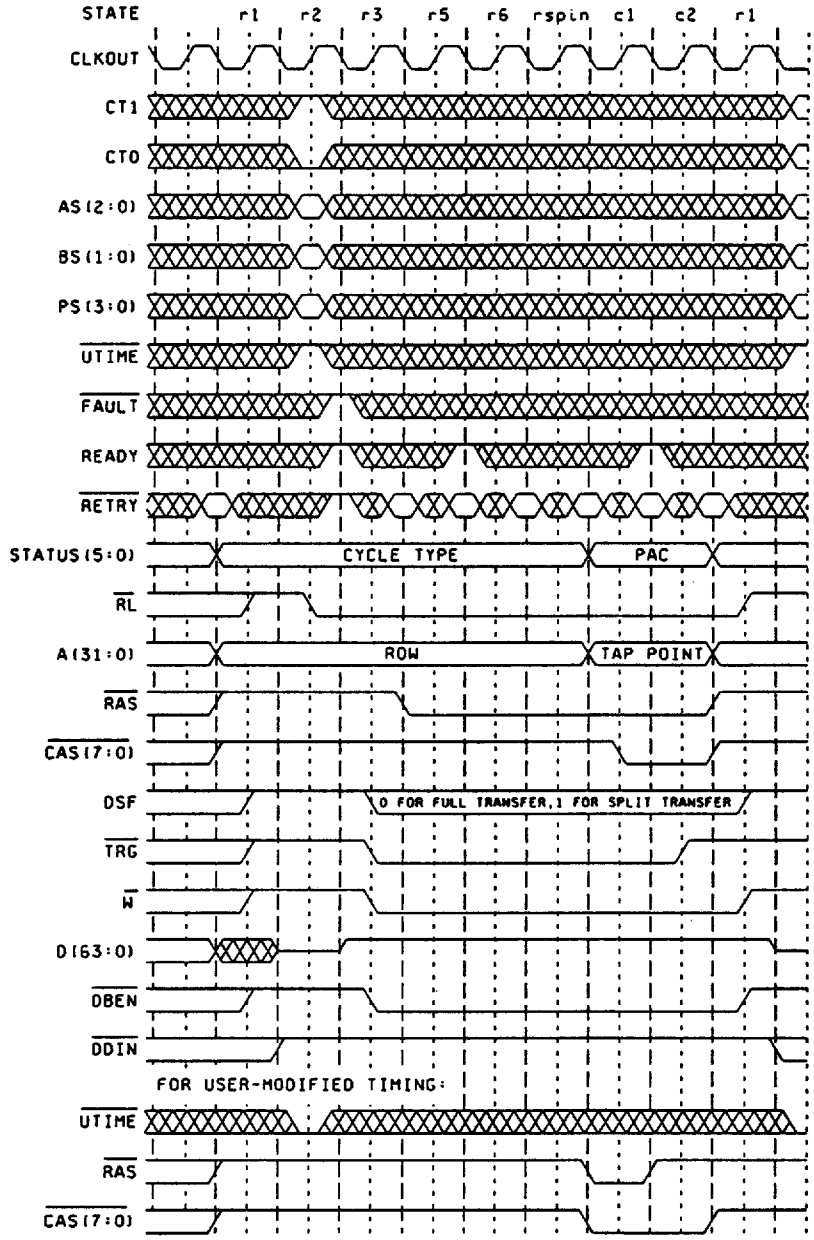
PIPLINED 1-CYCLES/COLUMN WRITE-TRANSFER AND
SPLIT-REGISTER WRITE-TRANSFER CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



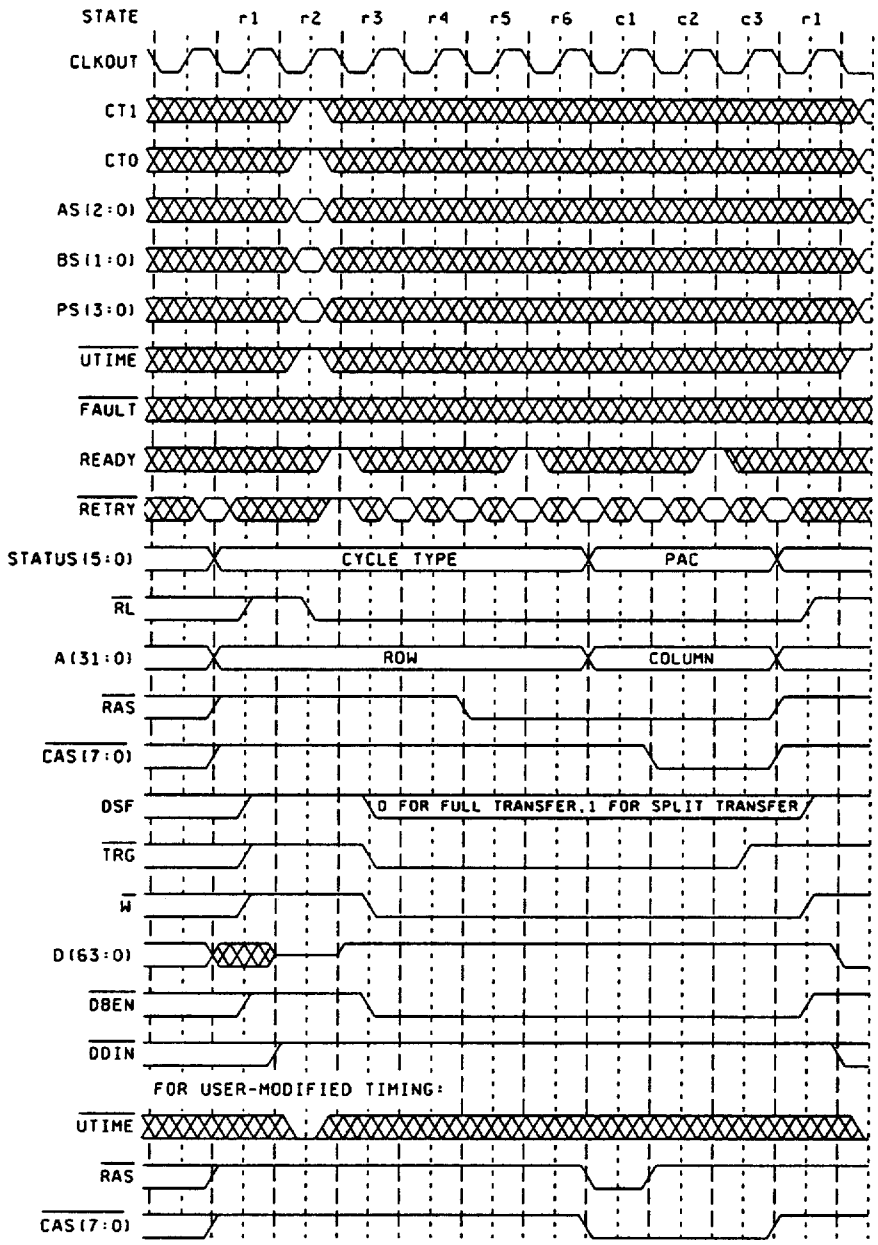
NONPIPLINED 1-CYCLES/COLUMN WRITE-TRANSFER AND
SPLIT-REGISTER WRITE-TRANSFER CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



2-CYCLES/COLUMN WRITE-TRANSFER AND
SPLIT-REGISTER WRITE-TRANSFER-CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



3 CYCLES/COLUMN WRITE-TRANSFER AND
SPLIT-REGISTER WRITE-TRANSFER-CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.

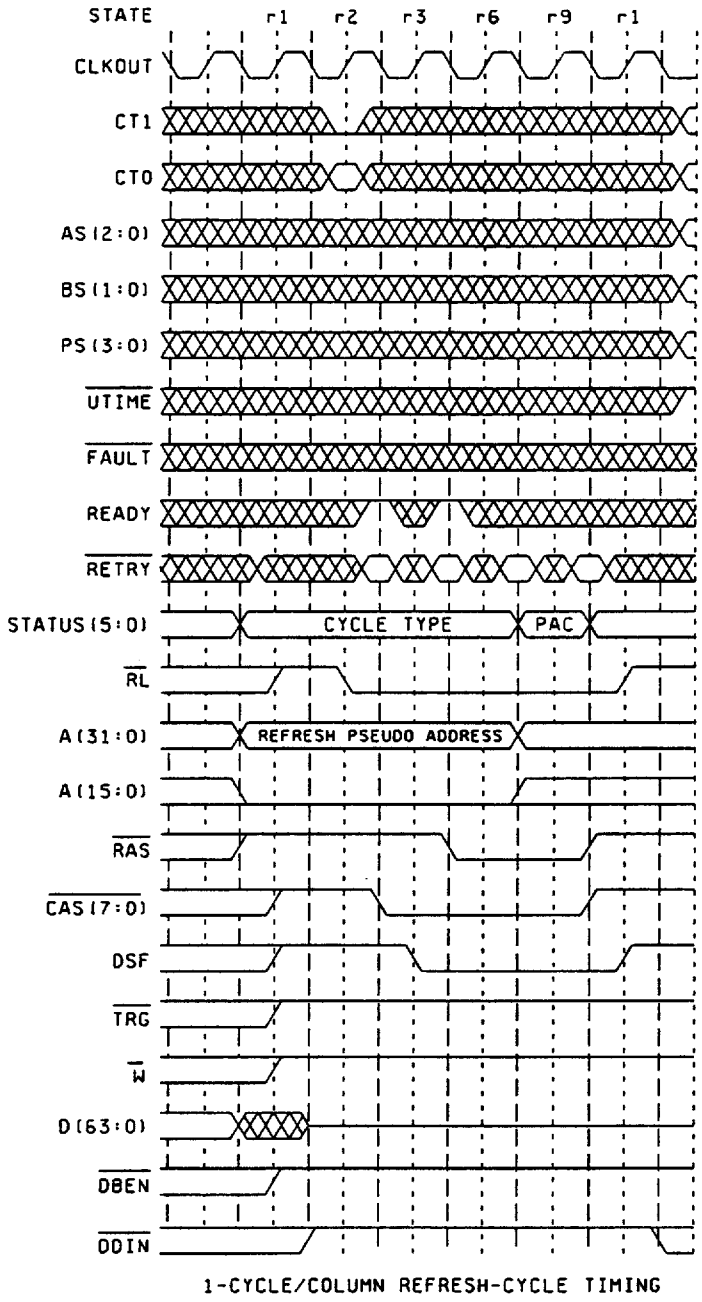


FIGURE 4. Timing waveforms - Continued.

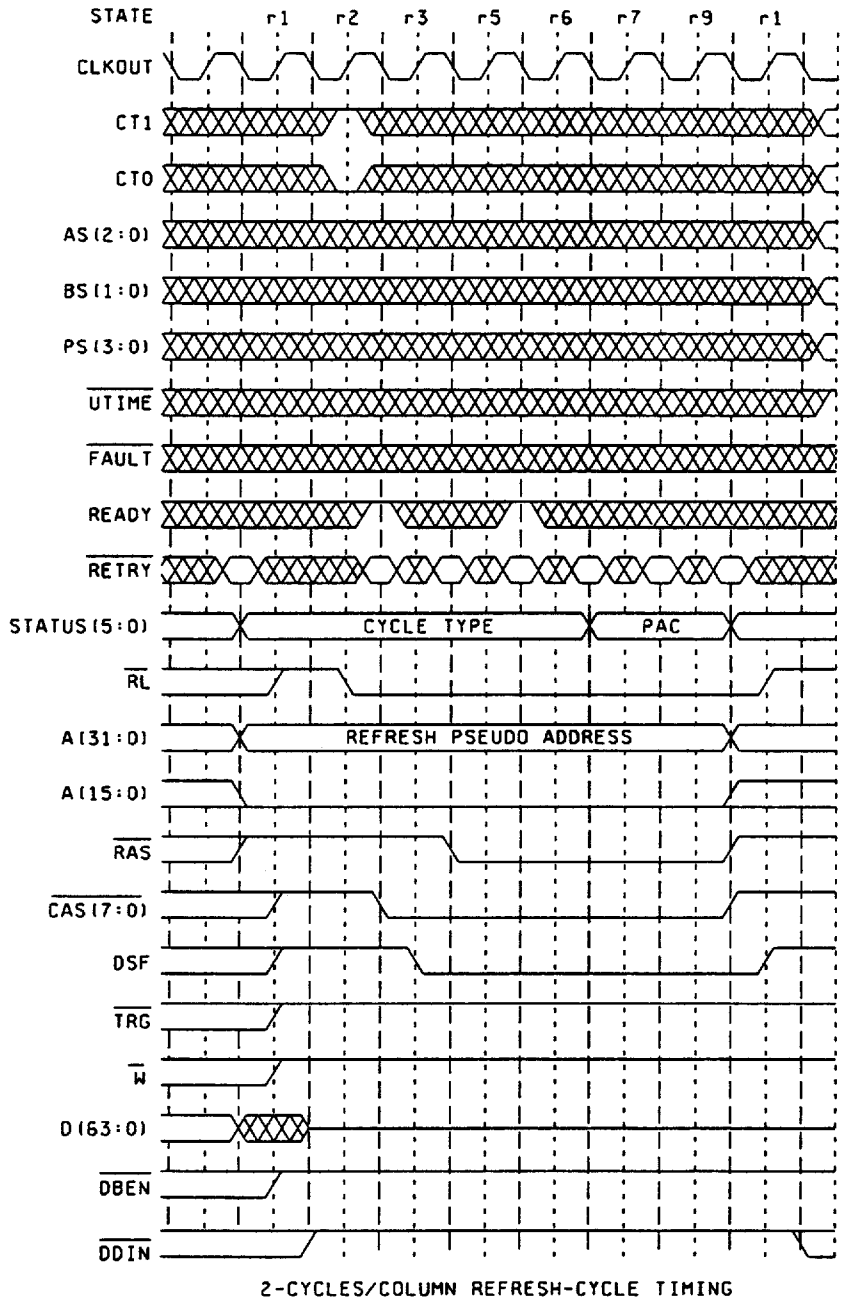
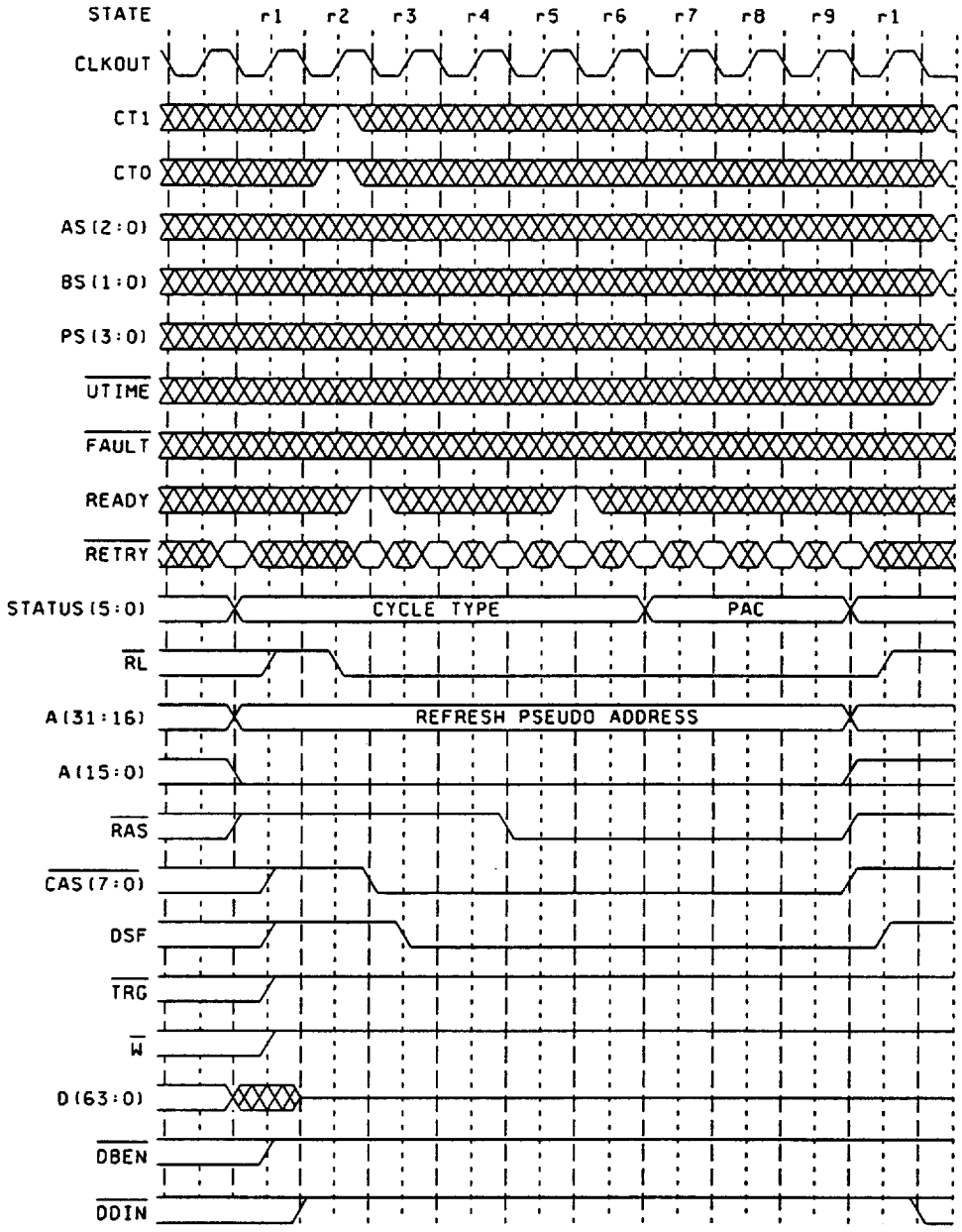
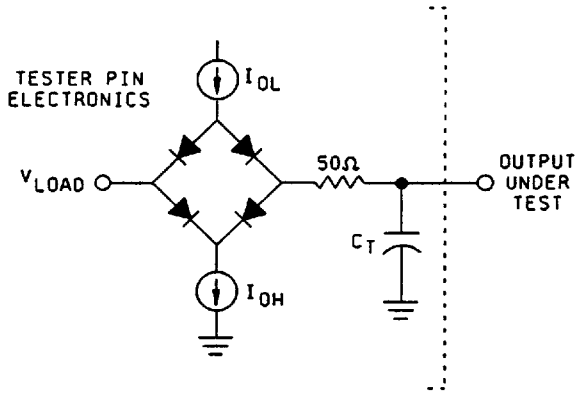


FIGURE 4. Timing waveforms - Continued.

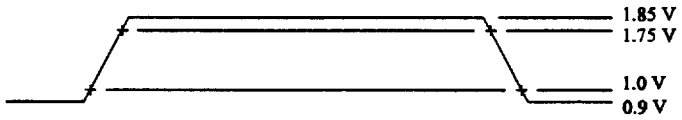


3 CYCLES/COLUMN REFRESH-CYCLE TIMING

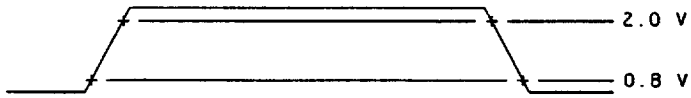
FIGURE 4. Timing waveforms - Continued.



TEST LOAD CIRCUIT



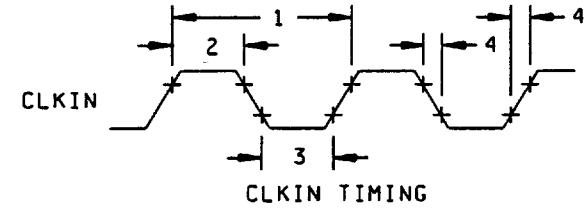
TTL LEVEL OUTPUTS



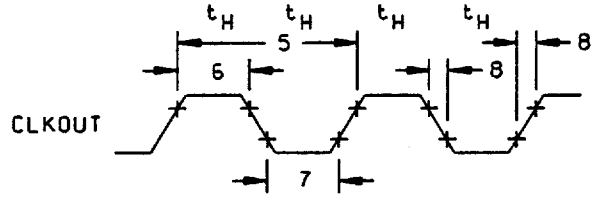
TTL LEVEL INPUTS

NOTE:
I_{OL} = 2.0 mA (all outputs)
I_{OH} = 400 µA (all outputs)
V_{LOAD} = 2.2 V
C_T = 60 pF typical load circuit distributed capacitance

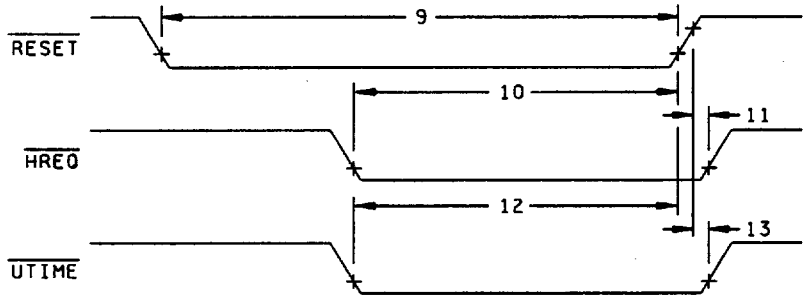
FIGURE 4. Timing waveforms - Continued.



CLKIN TIMING

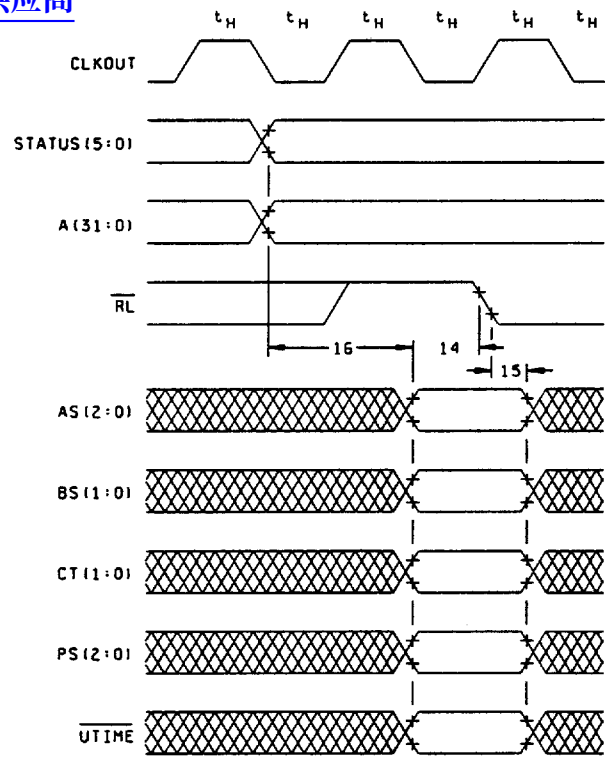


CLKOUT TIMING



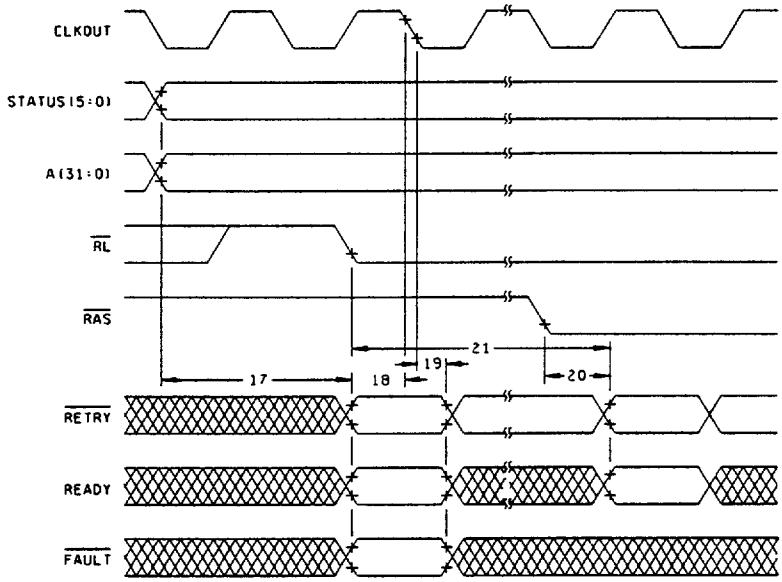
DEVICE RESET TIMING

FIGURE 4. Timing waveforms - Continued.

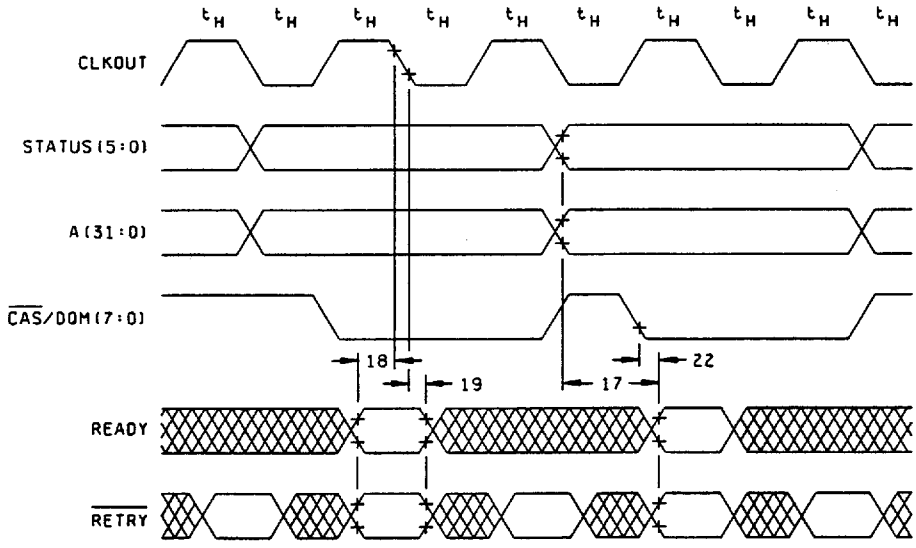


CYCLE CONFIGURATION INPUT TIMING

FIGURE 4. Timing waveforms - Continued.

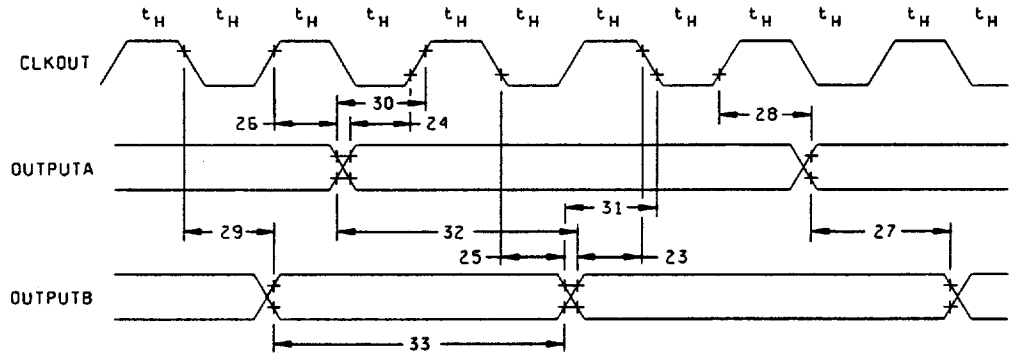


ROW TIME CYCLE COMPLETION INPUT TIMING

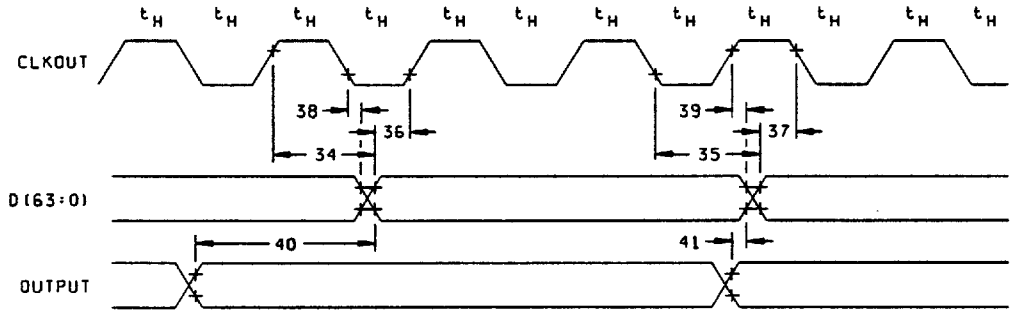


COLUMN TIME CYCLE COMPLETION INPUT TIMING

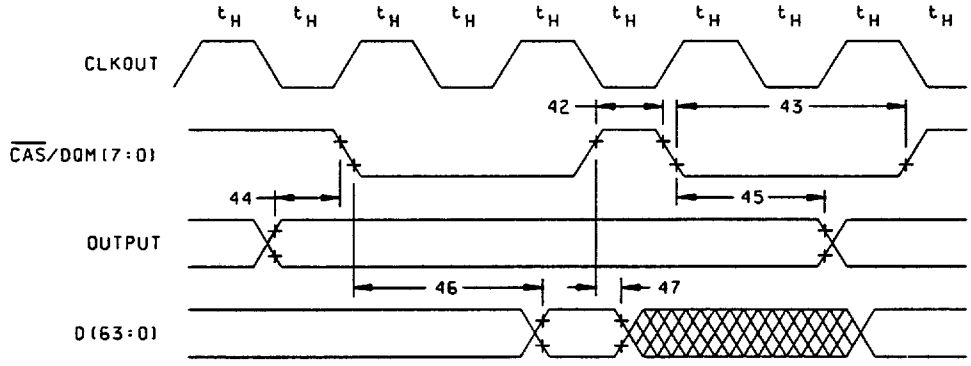
FIGURE 4. Timing waveforms - Continued.



GENERAL OUTPUT TIMING

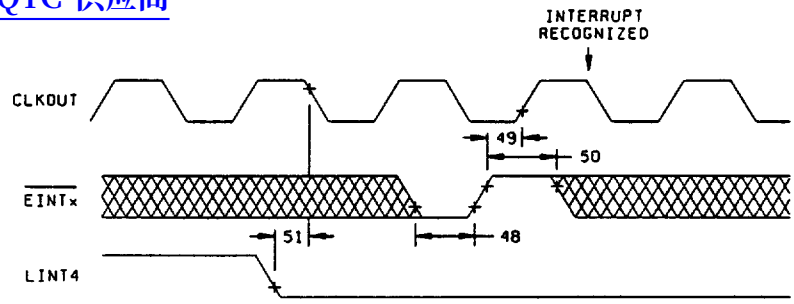


DATA INPUT TIMING

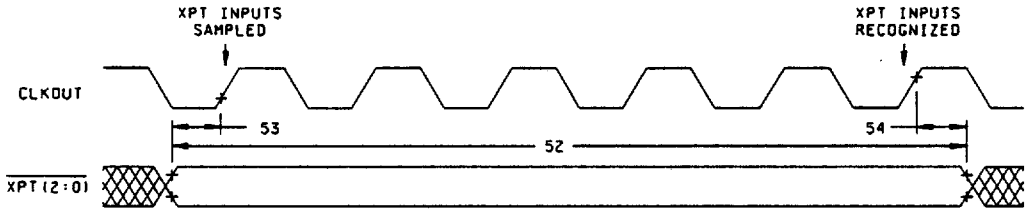


2 CYCLE/COLUMN CAS TIMING

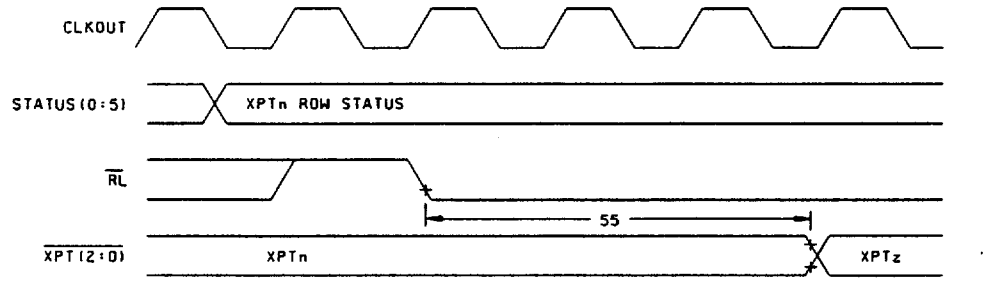
FIGURE 4. Timing waveforms - Continued.



EXTERNAL INTERRUPT TIMING

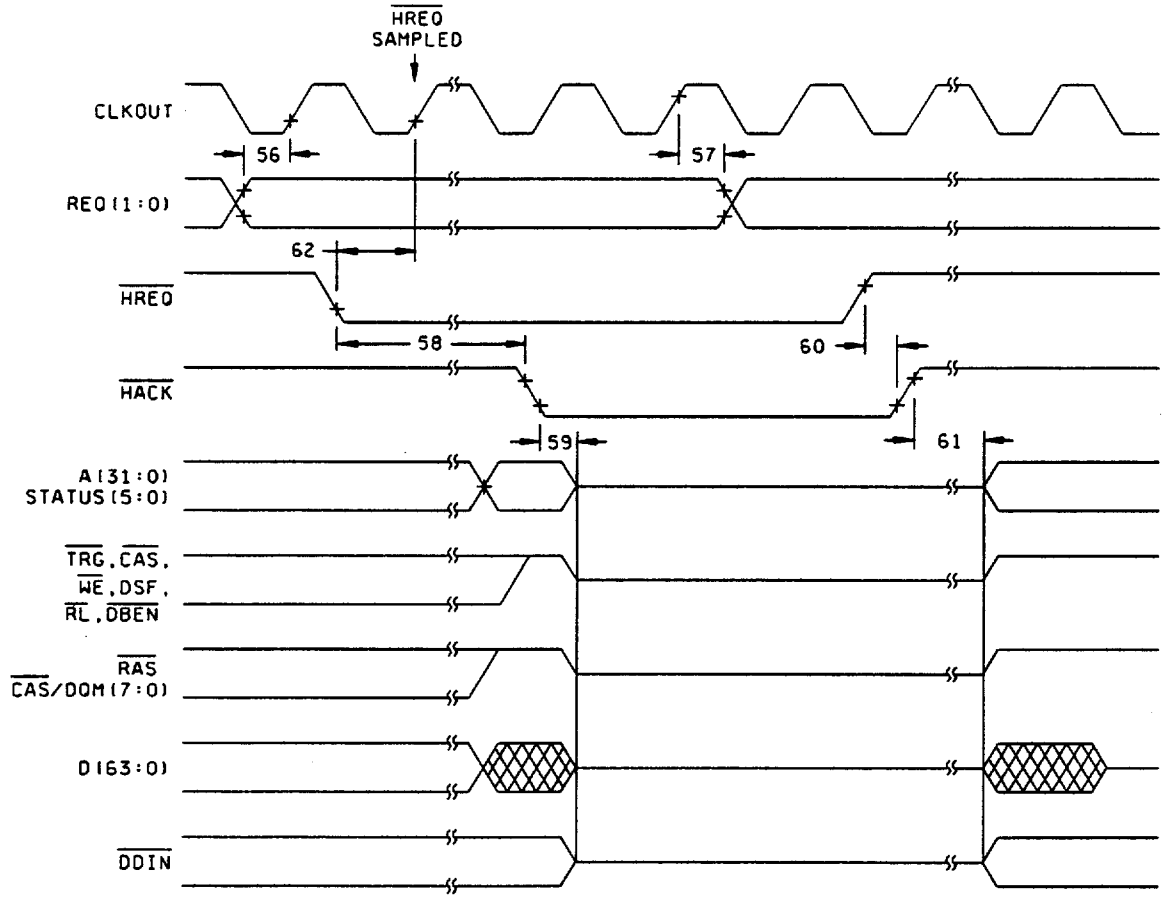


XPT IMPUT TIMING - XPT RECOGNITION



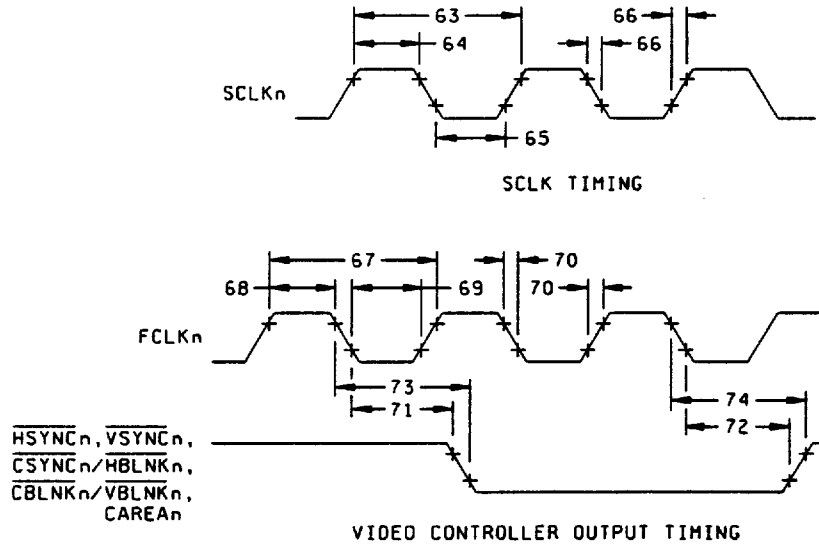
XPT IMPUT TIMING - XPT SERVICE

FIGURE 4. Timing waveforms - Continued.



HOST INTERFACE TIMING

FIGURE 4. Timing waveforms - Continued.



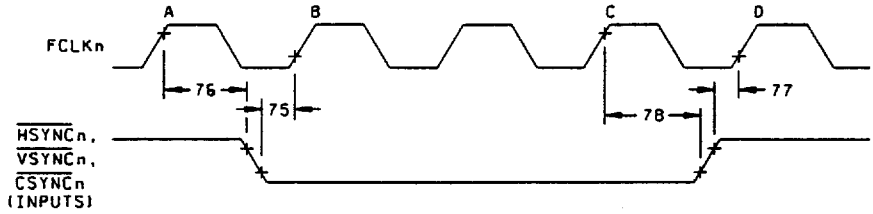


FIGURE 4. Timing waveforms - Continued.

Instruction Code	Instruction Name
00000000	Extest
11111111	Bypass
00000010	Sample
00000110	TRIBYP
00000011	INTEST

FIGURE 5. Boundry scan instruction codes.

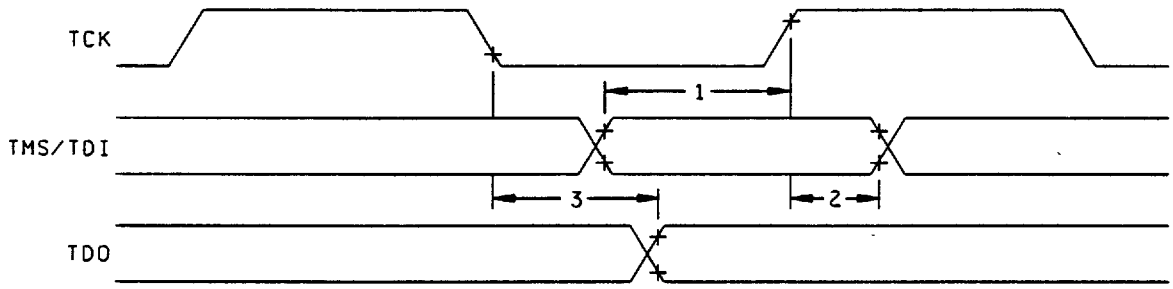


FIGURE 6. JTAG timing waveforms.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the funcionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_I and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)				1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8,9, 10,11
Group C end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group D end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows:

Pin symbol	Type	Description
		LOCAL MEMORY INTERFACE
A31-A0	O	Address bus. These terminals ouput the 32-bit byte address of the external memory cycle. The address can be multiplexed for DRAM accesses.
AS2-AS0	I	Address shift selection. These signals determine how the column address appears on the address bus. Eight shift values are supported, including zero.
BS1-BS0	I	Bus-size selection. These signals indicate the bus size of the memory or other device being accessed, allowing dynamic bus sizing for data buses less than 64 bits wide, as indicated below:

CT2	CT1	CT0	Cycle timing
0	0	1	Pipelined (burst lenght 1) SDRAM CAS latency of 2
0	0	0	Pipelined (burst lenght 1) SDRAM CAS latency of 3
0	1	0	Interleaved (burst lenght 2) SDRAM CAS latency of 2
0	1	1	Interleaved (burst lenght 2) SDRAM CAS latency of 3
1	0	0	Pipelined 1 cycle/column
1	0	1	Nonpipelined 1 cycle/column
1	1	0	2 cycle/column
1	1	1	3 cycle/column

D63-D0	I/O	Data bus. These signals transfer up to 64 bits of data per memory cycle into or out of the device.
$\overline{DBEN}$	O	Data buffer enable. This signal drives the active-low output enables of bidirectional transceivers that can be used to buffer input and output data on D63-D0.
$\overline{DDTN}$	O	Data-direction indicator. This signal indicate the direction of the data that passes through the transceivers. When $\overline{DDTN}$ is low, the transfer is from external memory into the device.
$\overline{FAULT}$	I	Fault. This input signal is driven low by external circuitry to inform the device that a fault occurred on the current memory row access.

Pin symbol	Type	Description - Continued.
ASIZ1-ASIZ0	I	Page-size indication. These signals indicate the page size of the memory device(s) being accessed by the current cycle. The device uses this to determine when to begin a new row access.
READY	I	Ready. This signal indicates that the external device is ready to complete the memory cycle. This signal is driven low by external circuitry to insert wait states into a memory cycle.
$\overline{RL}$	O	Row latch. The high-to-low transition of RL can be used to latch the valid 32-bit byte address that is present on A31-A0.
$\overline{RETRY}$	I	Retry. This signal is driven low by external circuitry to indicate that the addressed memory is busy. The device will begin the cycle again.
STATUS5-STATUS0	O	Status code. At row time, these signals indicate the type of cycle being performed. At column time, they indentify the processor and type of request that initated the cycle.
$\overline{UTIME}$	I	User-timing selection. This signal causes the time of RAS and CAS7-CAS0 to be modified so that custom memory timings can be generated. During reset, UTIME selects the endian mode in which the device operates.
		DRAM AND VRAM CONTROL
$\overline{CAS7}$-$\overline{CAS0}$	O	Column-address strobes. These outputs drive the CAS inputs of DRAMs and VRAMs. The eight stroves provide byte write access to memory.
DSF	O	Special function. This signal selects special VRAM functions such as block write, load color register, and split-register transfer.
$\overline{RAS}$	O	Row-address strobe. This signal drives the RAS inputs of DRAMs and VRAMs.
$\overline{TRG}$	O	Transfer/output enable. During memory-read cycles, TRG is used as an output enable or DRAMs and VRAMs. During VRAM register-transfer cycle, TRG is used as a transfer enable.
$\overline{W}$	O	Write enable. This signal is driven low before CAS during write cycles. W controls the direction of the transfer during VRAM transfer cycles.
		HOST INTERFACE
$\overline{HACK}$	O	Host acknowledge. The device drives this terminal low following an active HREQ to indicate that it has driven the local-memory-bus signals to the high-impedance state and is relinquishing the bus. HACK is driven high asynchronously following HREQ being detected inactive and the device resumes driving the bus.
$\overline{HREQ}$	I	Host request. An external device drives this input low to request ownership of the local-memory bus. When HREQ is high, the device owns and drives the bus. HREQ is internally synchronized to the devices internal clock. HREQ is also used at reset to determine the power-up state of the MP. If HREQ is low at the rising edge of RESET, the MP comes up running. If HREQ is high, the MP remains halted until the first interrupt occurrence on EINT3.
REQ1,REQ0	O	Internal cycle request. These signals provide a two-bit code indicating the highest priority memory-cycle request that is being received ty the TC. External logic can monitor these signals to determine if it is necessary to relinquish the local-memory bus to the device.

INTERNAL REQUEST

REQ1	REQ0	
0	0	Low-priority packet transfer, trackle refresh, idle
0	1	High-priority packet transfer
1	0	Cache/DEA (direct exterbak access) request, urgent packet transfer
1	1	VC SRT (serial-register transfer), urgent refresh, XPT (external packet transfer) or VCPT (VC packet transfer)

Pin symbol	Type	Description - Continued.
		SYSTEM CONTROL
CLKIN	I	Input clock. This signal generates the internal device clocks to which all processor functions (except the frame timers) are synchronous.
CLKOUT	O	Local output clock. This signal provides a way to synchronize external circuitry to internal timings. All device output signals (except the VC signals) are synchronous to this clock.
$\overline{\text{ETNT1}}$,$\overline{\text{ETNT2}}$, $\overline{\text{ETNT3}}$	I	Edge-triggered interrupts. These signals allow external devices to interrupt the MP on one of three interrupt levels ($\overline{\text{ETNT1}}$ is the highest priority). The interrupts are rising-edge triggered. $\overline{\text{ETNT3}}$ also serves as an unhalt signal. If the MP is powered up halted, the first rising edge on $\overline{\text{ETNT3}}$ causes the MP to unhalt and fetch its reset vector (the $\overline{\text{ETNT3}}$ interrupt pending bit is not set in this case).
$\overline{\text{LTNT4}}$	I	Level-triggered interrupt. This signal provides and active-low level-triggered interrupt to the MP. Its priority falls below that of the edge-triggered interrupts. Any interrupt request should remain low until it is recognized by the device.
$\overline{\text{RESET}}$	I	Reset. This signal is driven low to reset the device (all processors). During reset, all internal registers are set to their initial state and all ouputs are driven to their inactive or high-impedance levels. During the rising edge of $\overline{\text{RESET}}$, the MP reset mode and the devices operating endian mode are determined by the levels of $\overline{\text{HREQ}}$ and $\overline{\text{UTIME}}$ terminals, respectively.
$\overline{\text{XPT2}}$-$\overline{\text{XPT0}}$	I	External packet transfer. These encoded inputs are used by external devices to request a high-prioity XPT by the TC.
		EMULATION CONTROL
EMU0, EMU1	I/O	Emulation terminals. These terminals are used to support emulation host interupts, special functions targeted at a single processor, and multiprocessor halt-event communications.
TCK	I	Test clock. This signal provides the clock for the devices IEEE-1149.1 logic, allowing it to be compatible with IEEE-1149.1 devices, controllers, and test equipment designed for different clock rates.
TDI	I	Test data input. This signal provides input data for all IEEE-1149.1 instructions and data scans of the device.
TDO	O	Test data output. This signal provides output data for all IEEE-1149.1 instructions and data scans of the device.
TMS	I	Test mode select. This signal controls the IEEE-1149.1 state machine.
$\overline{\text{TRST}}$	I	Test reset. This signal resets the devices IEEE-1149.1 module. When low, all boundary-scan logic is disabled, allowing normal device operation.
CAREA0, CAREA1	O	Composite area. These signals define a special area such as an overscan boundary. This area represent the logical OR of the internal horizontal and vertical area signals.
$\overline{\text{CBLNK0}}$/$\overline{\text{VBLNK0}}$ $\overline{\text{CBLNK1}}$/$\overline{\text{VBLNK1}}$	O	Composite blanking/vertical blanking. Each of these signals provides one of two blanking functions, depending on the configuration of the $\overline{\text{CSYNC}}$/$\overline{\text{HBLNK}}$ terminal: Composite blanking disables pixel display/capture during both horizontal and vertical retrace periods and is enabled when $\overline{\text{CSYNC}}$ is selected for composite sync video systems. Vertical blanking disables pixel display/capture during vertical retrace periods and is enable when $\overline{\text{HBLNK}}$ is selected for separate-sync video systems. Initially these signals are configured as $\overline{\text{CBLNK0}}$, $\overline{\text{CBLNK1}}$

Pin symbol	Type	Description - Continued.

DESCRIPTION

$\overline{CSYNC0}$/$\overline{HBLNK0}$ $\overline{CSYNC1}$/$\overline{HBLNK1}$	I/O/Z	Composite sync/horizontal blanking. Thes terminals can be programmed for one of two functions: Composite sync is for use on composite-sync video systems and can be programmed as an input, output, or high-impedance signal. As an input, the device extracts horizontal and vertical sync information from externally generated from either external $\overline{HSYNC}$ and $\overline{VSYNC}$ signals or the devices internal video timers. In the high-impedance state, the terminal is neither driven nor allowed to drive circuitry. Horizontal blank disables pixel display/capture during horizontal retrace periods in separate-sync video systems and can be used as an output only. Immediately following reset, these signals are configured as high-impedance $\overline{CSYNC0}$ and $\overline{CSYNC1}$.
FCLK0, FCLK1	I	Frame clock. These signals are derived from the external video system's dotclock and are used to drive the devices video logic for frame timer 0 and frame timer 1.
$\overline{HSYNC0}$ $\overline{HSYNC1}$	I/O/Z	Horizontal sync. These signals control the video system. They can be programmed as input, ouput, or high-impedance signals. As an input, $\overline{HSYNC}$ synchronizes the video timer to externally generated horizontal sync pulses. As an output, $\overline{HSYNC}$ is an active-low horizontal sync pulse gererated by the device on-chip frame timer. In the high impedance state, the terminal is not driven and no internal synchronization is allowed to occur. Immediately folowing reset, these signals are in the high-impedance state.
SCLK0, SCLK1	I	Serial data clock. These clock inputs are used by the devices SRT controller to track the VRAM tap point when using midline reload. SCLK0 and SCLK1 should be the same signals that clock the serial register on the VRAMs controlled by frame timer 0 and frame timer 1, respectively.
$\overline{VSYNC0}$ $\overline{VSYNC}$	I/O/Z	Vertical sync. These signals control the video system. They can be programmed as an inputs, outputs, or high-impedance signals. As inputs, $\overline{VSYNCx}$ synchronizes the frame timer to externally generated vertical sync pulses. As ouputs, $\overline{VSYNCx}$ are active-low vertical-sync pulses generated by the device on-chip frame timer. In the high-impedance state, the terminal is not driven and no internal synchronization is allowed to occur, Immediately following reset, this signal is in the high-impedance state.
V_{SS}	I	Ground. Electrical ground inputs.
V_{DD}	I	Power. Nominal 3.3-V power supply inputs.
V_{CC}	I	5 V power. Nominal 5-V power supply inputs.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-06-10

Approved sources of supply for SMD 5962-96791 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9679101QXA	01295	SMJ320C80GFM50
5962-9679101QYC	01295	SMJ320C80HFHM50

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instrument, Incorporated 13500 North Central Expressway P.O. Box 655303 Dallas TX 75265 Point of contact: I-20 at FM 1788 Midland TX 79711-0448

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.