



# FDS4675\_F085

## 40V P-Channel PowerTrench<sup>®</sup> MOSFET

### General Description

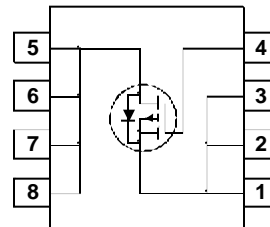
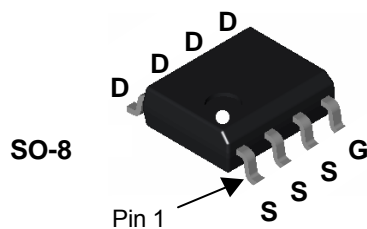
This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V – 20V).

### Applications

- Power management
- Load switch
- Battery protection

### Features

- –11 A, –40 V  $R_{DS(ON)} = 0.013 \Omega @ V_{GS} = -10 V$   
 $R_{DS(ON)} = 0.017 \Omega @ V_{GS} = -4.5 V$
- Fast switching speed
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability
- Qualified to AEC Q101
- RoHS Compliant



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	–40	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>b</sub>	Drain Current – Continuous (Note 1a) – Pulsed	–11	A
		–50	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	2.4 (steady state)	W
		1.4	
		1.2	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	–55 to +175	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	62.5 (steady state), 50 (10 sec)	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1c)	125	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	25	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS4675	FDS4675_F085	13"	12mm	2500 units



## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$		-34		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -32\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

## On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1	-1.4	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$		4.6		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -11\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -9.5\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -11\text{ A}, T_J = 125^\circ\text{C}$		10 13 15	13 17 21	m $\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-25			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -11\text{ A}$		44		S

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		4350		pF
$C_{oss}$	Output Capacitance			622		pF
$C_{rss}$	Reverse Transfer Capacitance			290		pF

## Switching Characteristics (Note 2)

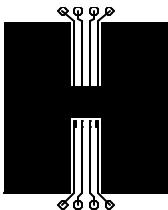
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -20\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		20	36	ns
$t_r$	Turn-On Rise Time			29	46	ns
$t_{d(off)}$	Turn-Off Delay Time			95	152	ns
$t_f$	Turn-Off Fall Time			60	96	ns
$Q_g$	Total Gate Charge	$V_{DS} = -20\text{ V}, I_D = -11\text{ A},$ $V_{GS} = -4.5\text{ V}$		40	56	nC
$Q_{gs}$	Gate-Source Charge			11		nC
$Q_{gd}$	Gate-Drain Charge			13		nC

## Drain-Source Diode Characteristics and Maximum Ratings

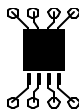
$I_S$	Maximum Continuous Drain-Source Diode Forward Current			-2.1		A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.1\text{ A}$ (Note 2)		-0.7	-1.2	V

### Notes:

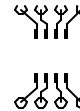
- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $105^\circ\text{C/W}$  when mounted on a  $.04\text{ in}^2$  pad of 2 oz copper



c)  $125^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty Cycle  $< 2.0\%$



## Typical Characteristics

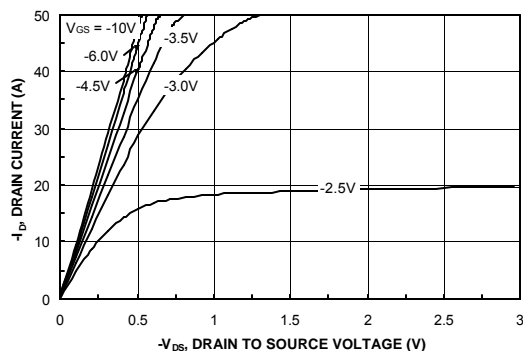


Figure 1. On-Region Characteristics.

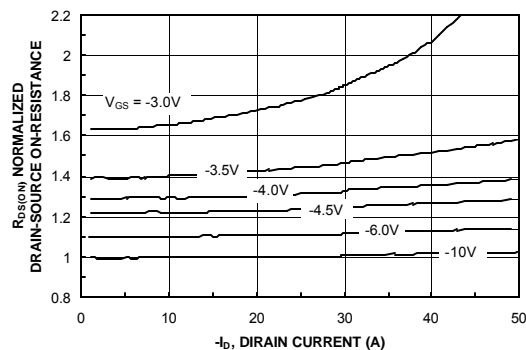


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

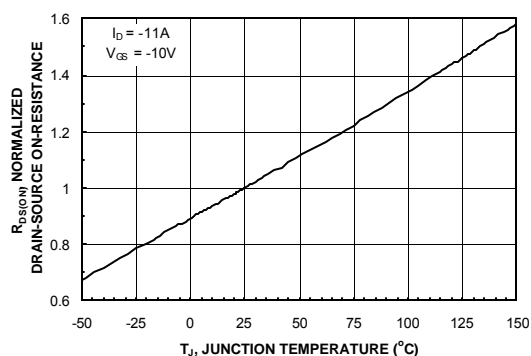


Figure 3. On-Resistance Variation with Temperature.

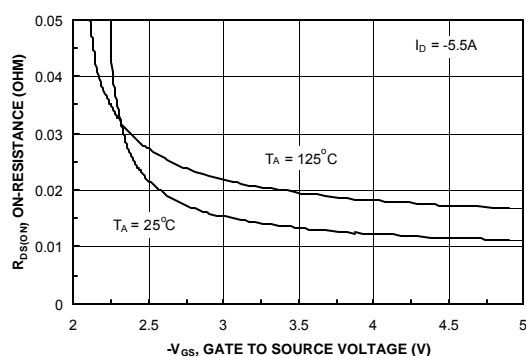


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

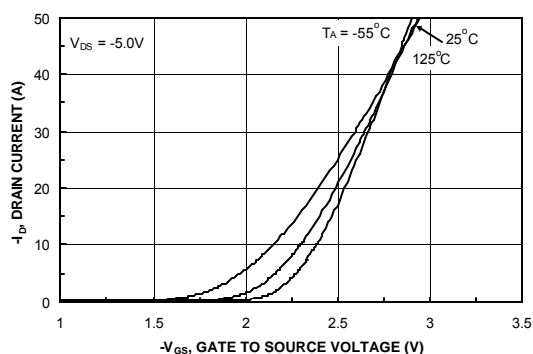


Figure 5. Transfer Characteristics.

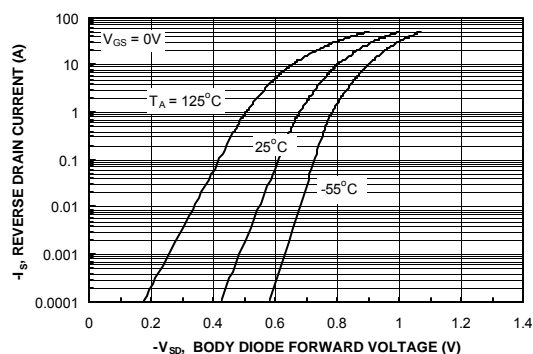


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.



## Typical Characteristics

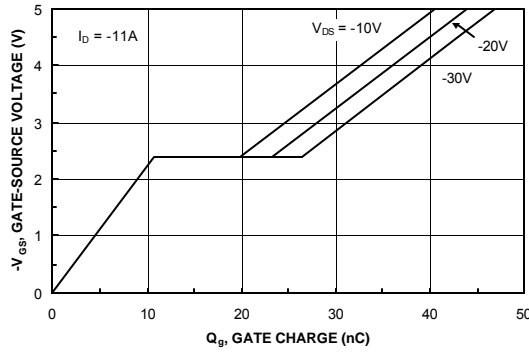


Figure 7. Gate Charge Characteristics.

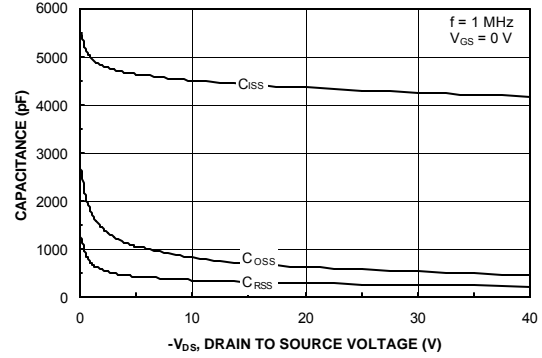


Figure 8. Capacitance Characteristics.

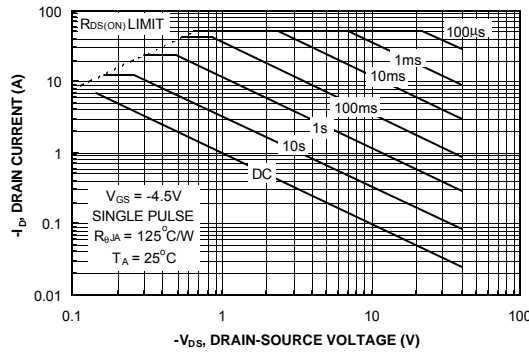


Figure 9. Maximum Safe Operating Area.

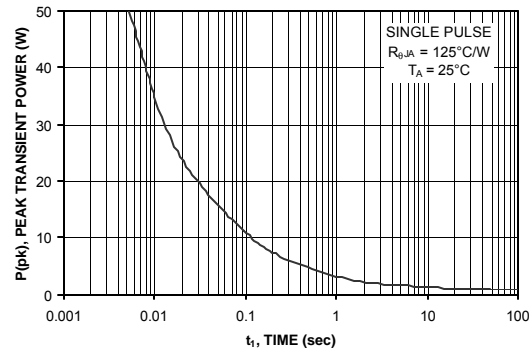


Figure 10. Single Pulse Maximum Power Dissipation.

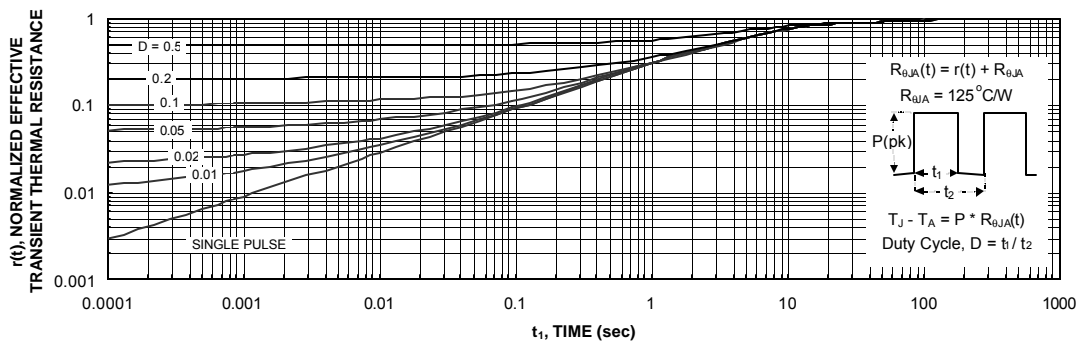


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.  
Transient thermal response will change depending on the circuit board design.







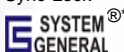
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