

查询"74HC563D-T"供应商

OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessor
- Common 3-state output enable input
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT563 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT563 are octal D-type transparent latches featuring separate D-type inputs for each latch and inverting 3-state outputs for bus oriented applications.

A latch enable (LE) input and an output enable (\bar{OE}) input are common to all latches.

The "563" is functionally identical to the "573", but has inverted outputs.

The "563" consists of eight D-type transparent latches with 3-state inverting outputs. The LE and \bar{OE} are common to all latches.

When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.

When \bar{OE} is LOW, the contents of the 8 latches are available at the outputs. When \bar{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \bar{OE} input does not affect the state of the latches.

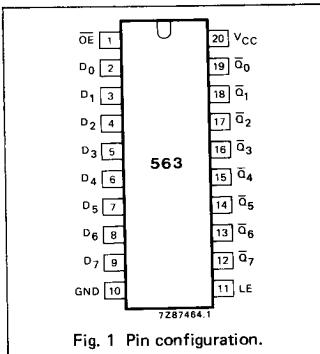


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n , LE to \bar{Q}_n	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	14	16	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

$GND = 0 \text{ V}$; $T_{amb} = 25^\circ \text{C}$; $t_r = t_f = 6 \text{ ns}$

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF
 f_o = output frequency in MHz V_{CC} = supply voltage in V
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC, the condition is $V_I = GND$ to V_{CC}
For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).

20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
11	LE	latch enable input (active HIGH)
1	\bar{OE}	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	\bar{Q}_0 to \bar{Q}_7	3-state latch outputs
20	V_{CC}	positive supply voltage

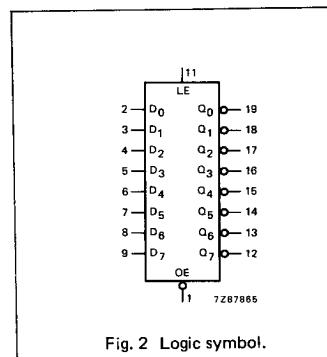


Fig. 2 Logic symbol.

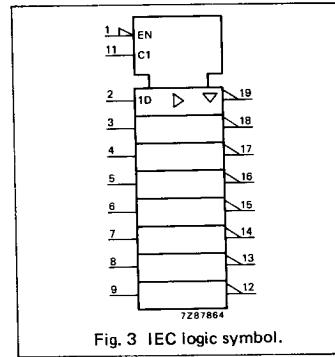
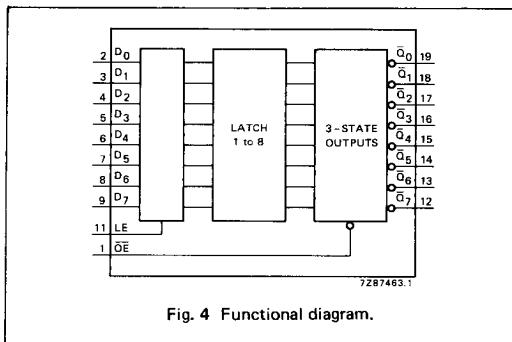


Fig. 3 IEC logic symbol.

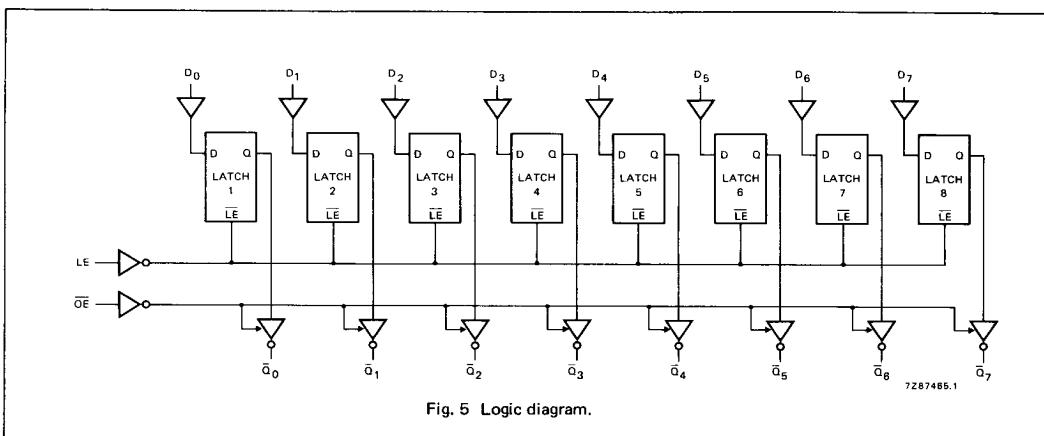
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FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS \bar{Q}_0 to \bar{Q}_7
	OE	LE	D_n		
enable and read register	L L	H H	L H	L H	H L
latch and read register	L L	L h	I	L H	H L
latch register and disable outputs	H H	L L	I h	L H	Z Z

H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
 L = LOW voltage level
 I = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
 Z = high impedance OFF-state



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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HC							V _{CC} V	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay D _n to \bar{Q}_n	47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6		
t _{PHL} / t _{PLH}	propagation delay LE to \bar{Q}_n	47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7		
t _{PZH} / t _{PZL}	3-state output enable time \bar{OE} to \bar{Q}_n	47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8		
t _{PHZ} / t _{PLZ}	3-state output disable time \bar{OE} to \bar{Q}_n	50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8		
t _{THL} / t _{TLH}	output transition time	14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6		
t _W	enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 7		
t _{su}	set-up time D _n to LE	50 10 9	11 4 3		65 13 11		75 15 13	ns	2.0 4.5 6.0	Fig. 9		
t _h	hold time D _n to LE	4 4 4	−6 −2 −2		4 4 4		4 4 4	ns	2.0 4.5 6.0	Fig. 9		

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_n	0.35
LE	0.65
\overline{OE}	1.25

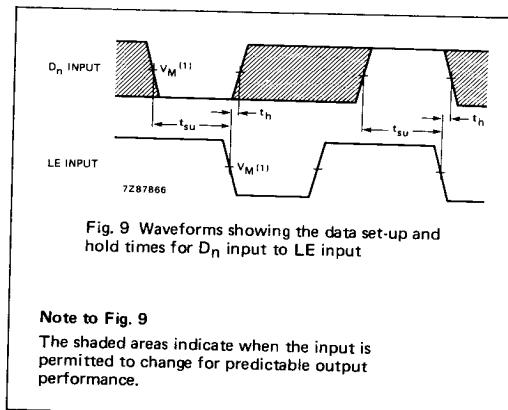
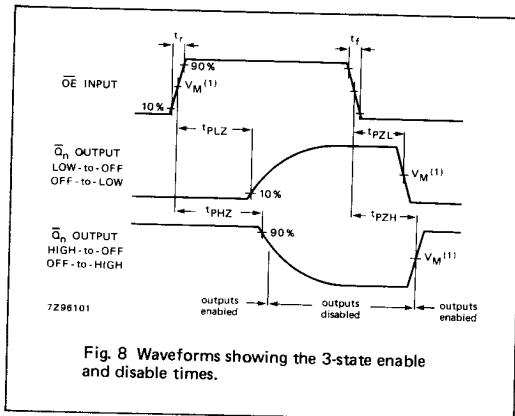
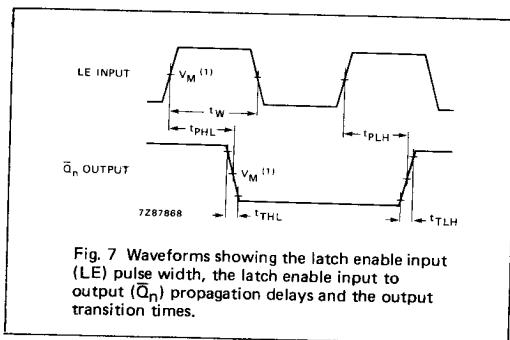
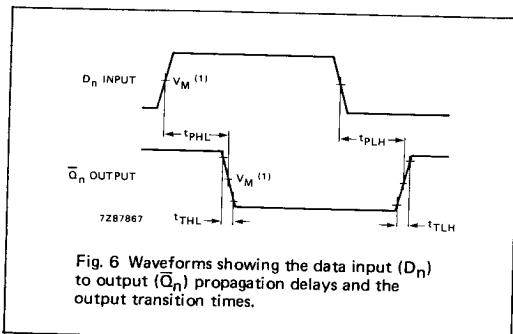
AC CHARACTERISTICS FOR 74HCT

$GND = 0 \text{ V}$; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HCT							V _{CC} V	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/t_{PLH}	propagation delay D_n to \overline{Q}_n		18	30		38		45	ns	4.5	Fig. 6	
t_{PHL}/t_{PLH}	propagation delay LE to \overline{Q}_n		19	35		44		53	ns	4.5	Fig. 7	
t_{PZH}/t_{PZL}	3-state output enable time \overline{OE} to \overline{Q}_n		20	35		44		53	ns	4.5	Fig. 8	
t_{PHZ}/t_{PZL}	3-state output disable time \overline{OE} to \overline{Q}_n		22	35		44		53	ns	4.5	Fig. 8	
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6	
t_W	enable pulse width HIGH	16	5		20		24		ns	4.5	Fig. 7	
t_{su}	set-up time D_n to LE	10	3		13		15		ns	4.5	Fig. 9	
t_h	hold time D_n to LE	5	−1		5		5		ns	4.5	Fig. 9	

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AC WAVEFORMS



Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC}
HCT: $V_M = 1.3\text{ V}$; $V_I = GND$ to 3 V .