

# 2N7104 SERIES



N-Channel Lateral DMOS FETs

T-35-25

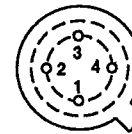
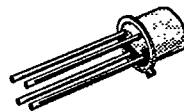
The 2N7104 Series of lateral DMOS FETs is designed for high speed switching in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. For long term reliability this series features a polysilicon gate, making Siliconix 2N7104 devices the perfect choice for high-performance military applications.

PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{ds(ON)}$ MAX ( $\Omega$ )	$C_{rss}$ MAX (pF)	$t_{ON}$ MAX (ns)
2N7104	20	70	0.5	2
2N7106	10	70	0.5	2
2N7108	15	70	0.5	2

For additional design information please see performance curves DMOS, which are located in Section 7.

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BOTTOM VIEW



- 1 SOURCE
- 2 DRAIN
- 3 GATE
- 4 SUBSTRATE, CASE

## SIMILAR PRODUCTS

- Quad Array, See 2N7116 Series
- SO-14 Array, See SD5400 Series
- Zener Protection, See 2N7105 Series
- SOT-143, See SST211 Series
- Chips, Order 2N710XCHP

## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT			UNITS
		2N7104	2N7106	2N7108	
Gate-Source, Gate-Drain Gate-Substrate Voltage	$V_{GS}, V_{GD}, V_{GB}$	$\pm 40$	$\pm 40$	$\pm 40$	V
Drain-Source Voltage	$V_{DS}$	30	10	20	
Source-Drain Voltage	$V_{SD}$	10	10	20	
Drain-Substrate Voltage	$V_{DB}$	30	15	25	
Source-Substrate Voltage	$V_{SB}$	15	15	25	
Drain Current	$I_D$	50	50	50	mA
Power Dissipation ( $T_J = 25^\circ\text{C}$ )	$P_D$	300	300	300	mW
Power Derating		2.4	2.4	2.4	mW/ $^\circ\text{C}$
Operating Junction Temperature	$T_J$	-55 to 150			$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65 to 200			
Lead Temperature (1/16" from case for 10 seconds)	$T_L$	300			



## 2N7104 SERIES

ELECTRICAL CHARACTERISTICS <sup>1</sup>			LIMITS							
PARAMETER	SYMBOL	TEST CONDITIONS	TYP <sup>2</sup>	2N7104		2N7106		2N7108		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
<b>STATIC</b>										
Drain-Source Breakdown Voltage <sup>3</sup>	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0\text{ V}, I_D = 10\ \mu\text{A}$	35	30						V
		$V_{GS} = V_{BS} = -5\text{ V}, I_S = 10\text{ nA}$	30	10		10		20		
Source-Drain Breakdown Voltage <sup>3</sup>	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5\text{ V}, I_D = 10\text{ nA}$	22	10		10		20		
Drain-Substrate Breakdown Voltage <sup>3</sup>	$V_{(BR)DB}$	$V_{GB} = 0\text{ V}$ $I_D = 10\text{ nA}$ Source OPEN	35	15		15		25		
Source-Substrate Breakdown Voltage <sup>3</sup>	$V_{(BR)SB}$	$V_{GB} = 0\text{ V}$ $I_S = 10\ \mu\text{A}$ Drain OPEN	35	15		15		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5\text{ V}$	$V_{DS} = 10\text{ V}$ 0.4		10		10			nA
		$V_{GS} = V_{BS} = -5\text{ V}$ $T_A = 125^\circ\text{C}$	$V_{DS} = 20\text{ V}$ 0.9						10	
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5\text{ V}$	$V_{SD} = 10\text{ V}$ 0.5		10		10			nA
		$V_{GD} = -5\text{ V}$ $T_A = 125^\circ\text{C}$	$V_{SD} = 20\text{ V}$ 1						10	
Gate Leakage	$I_{GSS}$	$V_{DS} = V_{SB} = 0\text{ V}$ $V_{GS} = 12\text{ V}$			100		100		100	nA
		$T_A = 125^\circ\text{C}$			1		1		1	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = V_{BS} = 0\text{ V}$			10					$\mu\text{A}$
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}, I_S = 1\ \mu\text{A}$ $V_{SB} = 0\text{ V}$	0.7	0.5	2.0	0.1	2.0	0.1	2.0	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{GS} = 5\text{ V}, I_D = 1\text{ mA}$	58		70		70		70	$\Omega$
<b>DYNAMIC</b>										
Forward Transconductance <sup>3</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, V_{SB} = 0\text{ V}$ $I_D = 20\text{ mA}, f = 1\text{ kHz}$	11							mS
Output Conductance <sup>3</sup>	$g_{os}$		0.9							
Gate Node Capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, f = 1\text{ MHz}$ $V_{GS} = V_{BS} = -15\text{ V}$	2.5		3.5		3.5		3.5	pF
Reverse Transfer Capacitance	$C_{rss}$		0.2		0.5		0.5		0.5	
<b>SWITCHING</b>										
Turn-ON Time	$t_d(ON)$	$V_{DD} = 5\text{ V}, R_L = 680\ \Omega$ $V_{IN} = 5\text{ V}, R_G = 50\ \Omega$	0.5		1		1		1	ns
	$t_r$		0.6		1		1		1	
Turn-OFF Time <sup>3</sup>	$t_d(OFF)$		2							
	$t_f$		6							

NOTES: 1.  $T_A = 25^\circ\text{C}$  unless otherwise noted.

2. For design aid only, not subject to production testing.

3. This parameter not registered with JEDEC.

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