Signetics

T-45-23-09

54F190, 54F191
Counters

54F190 Asynchronous Presettable BCD/Decade Up/Down Counter
54F191 Asynchronous Presettable 4-Bit Binary Up/Down Counter

Product Specification

Military FAST Products

FEATURES

- Synchronous, reversible counting
- BCD/decade — 54F190
  4-bit binary — 54F191
- Asynchronous parallel load capability
- Count enable control for synchronous expansion
- Single up/down control input

DESCRIPTION

The 54F190 is an asynchronous presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. The 54F191 is similar, but is a 4-bit binary counter.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

ORDERING INFORMATION

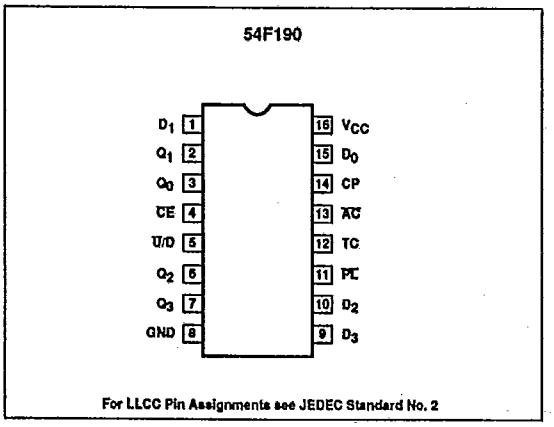
DESCRIPTION	ORDER CODE
Ceramic DIP	54F190/BEA 54F191/BEA
Ceramic Flat Pack	54F190/BFA 54F191/BFA
Ceramic LLCC	54F190/B2A 54F191/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

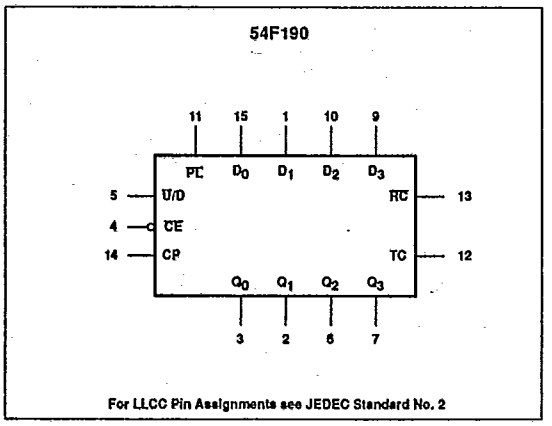
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CE}$	Count enable input (active low)	1.0/3.0	20µA/1.8mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
D_0 - D_3	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{PL}$	Asynchronous parallel load input (active low)	1.0/1.0	20µA/0.6mA
U/D	Up/down count control input	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{RC}$	Ripple clock output (active low)	50/33	1.0mA/20mA
TC	Terminal count output (active high)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

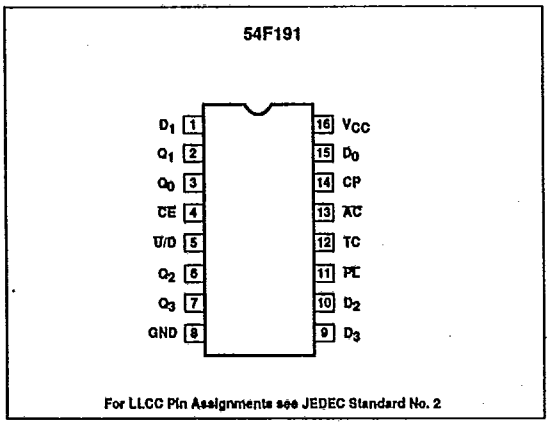
PIN CONFIGURATION



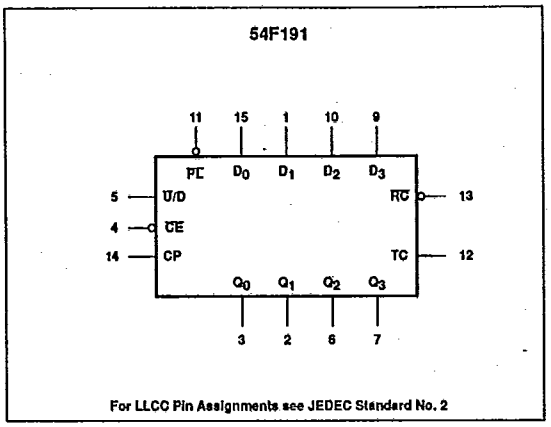
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC SYMBOL



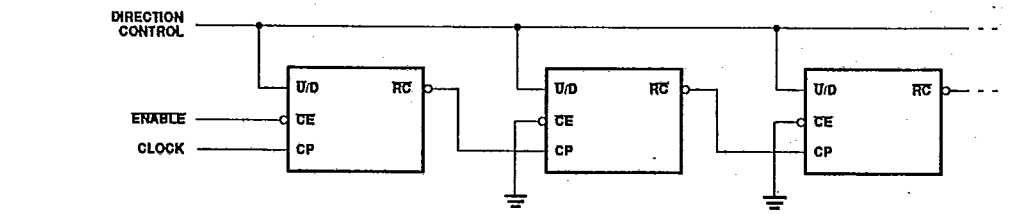
Counting is inhibited by a High level on the Count Enable ($\overline{CE}$) input. When $\overline{CE}$ is Low, internal state changes are initiated.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally Low and goes High when a circuit reaches zero in the count-down mode or reaches "9" in the count-up mode for 54F190 and reaches "15" in the count-up mode for 54F191. The TC output will remain High until a state change occurs, either by counting or presetting, or until U/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

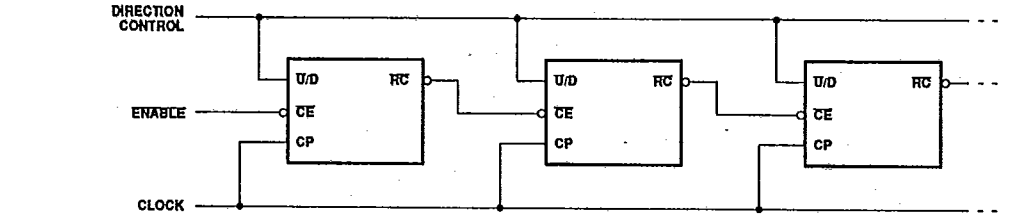
The TC signal is used internally to enable the $\overline{RC}$ output. When TC is High and $\overline{CE}$ is Low, the $\overline{RC}$ follows the Clock Pulse (CP) delayed by two gate delays. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays. This feature simplifies the design of multi-stage counters, as indicated in Figures 1a and 1b. In Figure 1a, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any package goes High shortly after its CP input goes High, there is no such restriction on the High state duration of the clock.

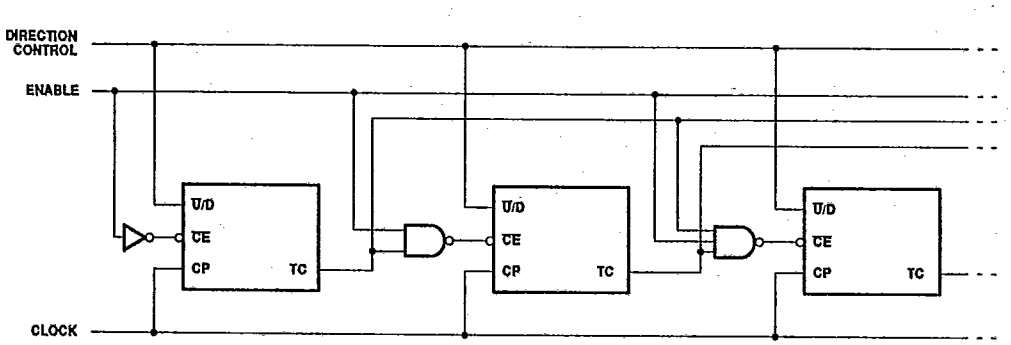
In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.



a. N-Stage Counter Using Ripple Clock



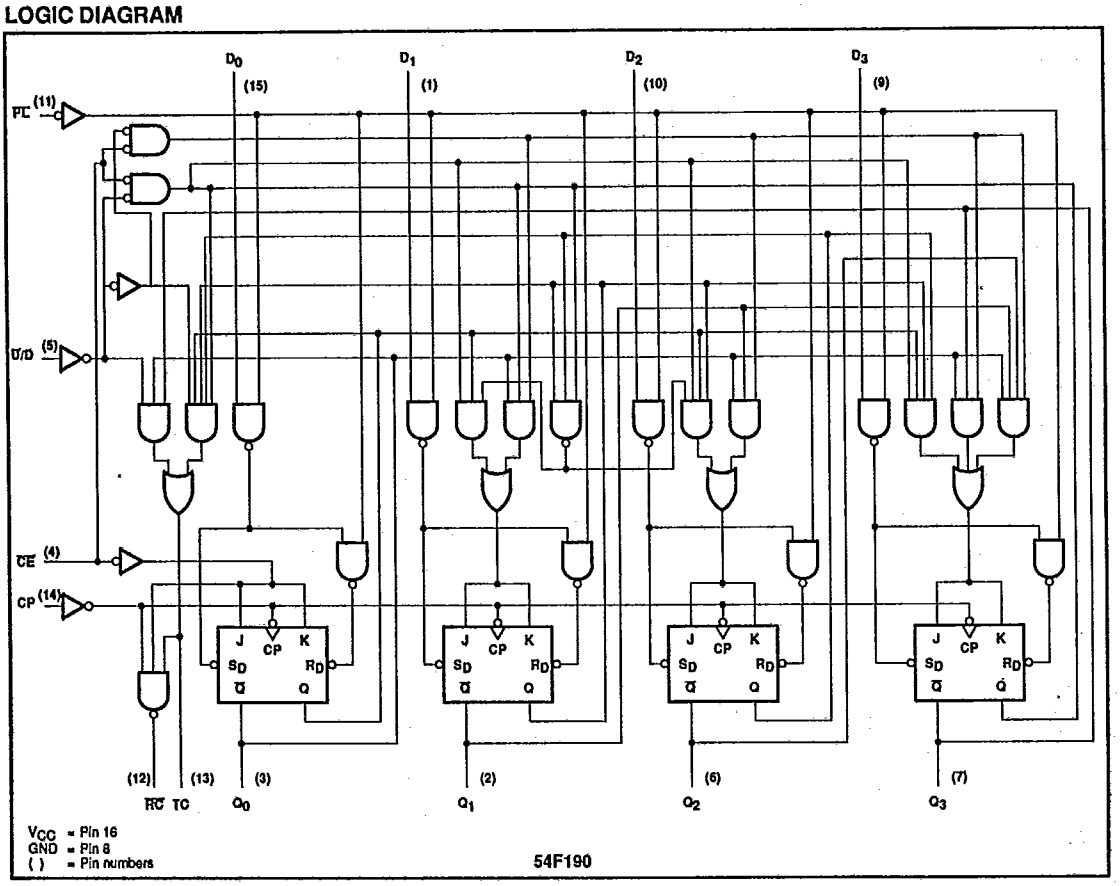
b. Synchronous N-Stage Counter Using Ripple Carry Borrow



c. Synchronous N-Stage Counter with Parallel Gated Carry Borrow

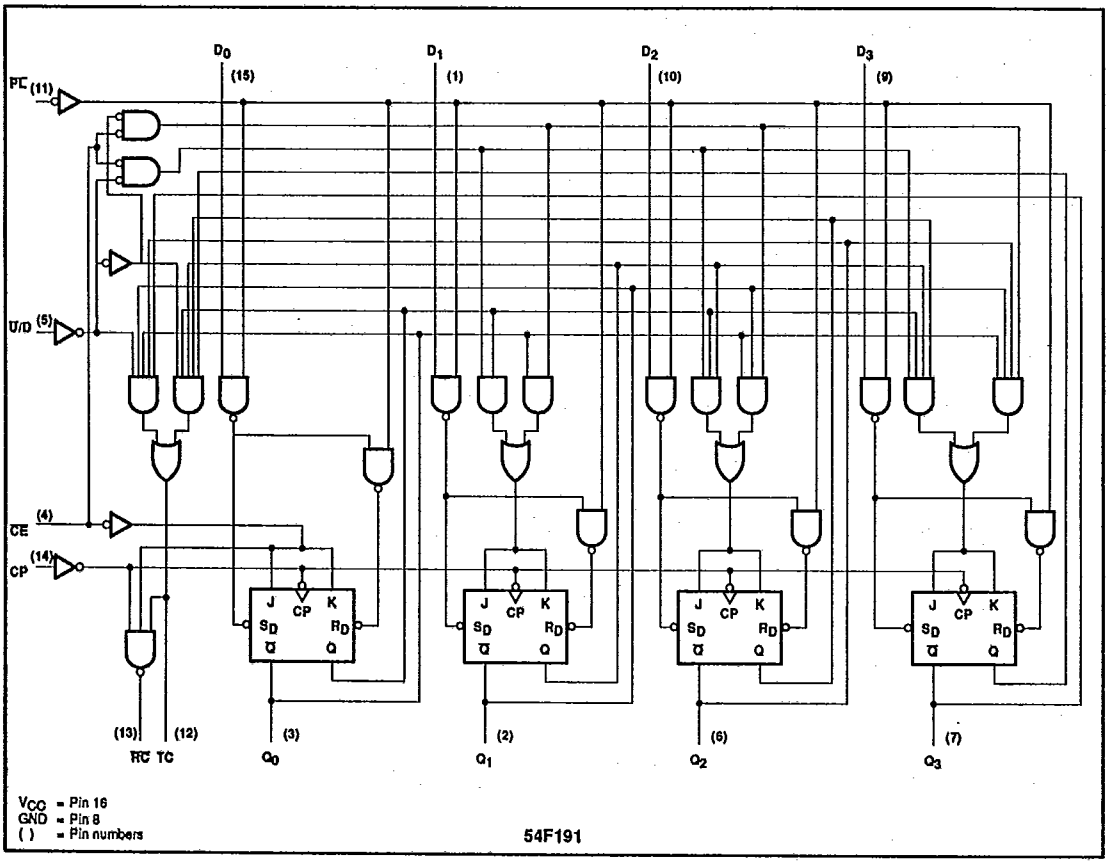
Figure 1

LOGIC DIAGRAM



54F190

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE, 54F190, 54F191

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	U/D	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L L	X X	X X	X X	L H	L H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE, 54F190

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
U/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊔	H	X	X	H	↓	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	↓	⊔

TC AND $\overline{RC}$ FUNCTION TABLE, 54F191

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
U/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊔	H	H	H	H	↓	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	↓	⊔

H = High voltage level steady state
L = Low voltage level steady state
l = Low voltage level one set-up time prior to Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
⊔ = Low pulse
↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	$\overline{CE}$ input	V_{CC} = Max, V_I = 7.0V			0.3	mA
		Other inputs				0.1	mA
I_{IH1}	High-level input current	$\overline{CE}$ input	V_{CC} = Max, V_I = 2.7V			60	µA
		Other inputs				20	µA
I_{IL}	Low-level input current	$\overline{CE}$ input	V_{CC} = Max, V_I = 0.5V			-1.8	mA
		Other inputs				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = Max		38	55	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

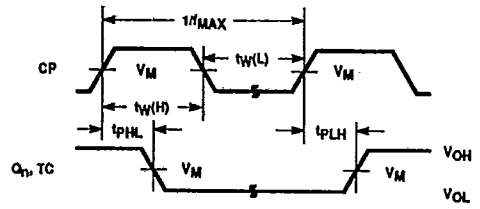
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency (Q_n)	Waveform 1	100	125		80[5]		MHz
f_{MAX}	Maximum clock frequency ($\overline{RC}$)	Waveform 2	85	95		75[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	2.5 5.0	4.5 7.5	8.0 11.5	2.0 5.0	8.5 12.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	Waveform 1	6.5 6.0	9.0 8.0	12.5 11.0	6.0 6.0	13.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$	Waveform 2	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	8.0 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$	Waveform 2	2.0 3.0	4.0 5.0	7.0 7.5	2.0 3.0	7.5 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/D to $\overline{RC}$	Waveform 2	8.0 4.5	11.0 7.5	16.0 10.5	8.0 4.0	17.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/D to TC	Waveform 4	4.0 3.0	6.5 6.0	9.5 9.5	3.0 3.0	10.5 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 3	2.0 6.5	4.0 9.0	7.0 12.0	1.5 6.5	7.5 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n	Waveform 5	4.5 5.5	6.5 8.0	9.5 11.5	4.0 5.0	11.0 12.5	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$	Waveform 3 Waveform 4	6.0 6.0	14.0 11.0	18.0 13.5	6.0 6.0	21.0 15.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC	Waveform 3 Waveform 4	5.5 6.5	9.5 9.5	13.0 13.0	5.0 6.0	14.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC	Waveform 5	5.5 6.0	8.5 10.5	12.0 13.5	5.5 6.0	14.5 15.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$	Waveform 5	8.5 7.5	16.0 10.0	18.5 13.0	8.5 7.0	22.0 14.5	ns ns

AC SETUP REQUIREMENTS

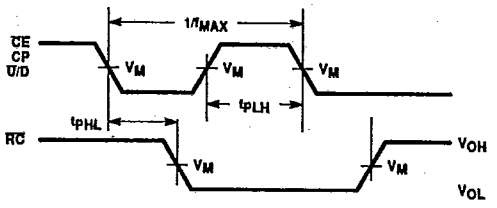
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 6.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 3.0		ns ns
$t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	Waveform 6	10.0			10.0		ns
$t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP	Waveform 6	0			0.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{U}$/D to CP	Waveform 6	12.0 12.0			12.0 12.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP	Waveform 6	0 0			0 0		ns ns
$t_w(L)$	$\overline{PL}$ Pulse width	Waveform 5	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width	Waveform 1	3.5 6.0			3.5 6.0		ns ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 5	6.0			8.0		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.
5. These parameters are guaranteed, but not tested.

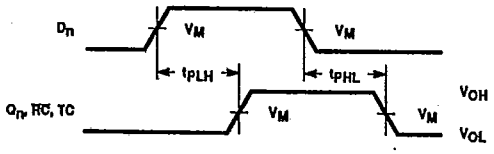
AC WAVEFORMS



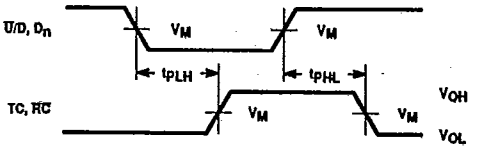
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths and Maximum Clock Frequency.



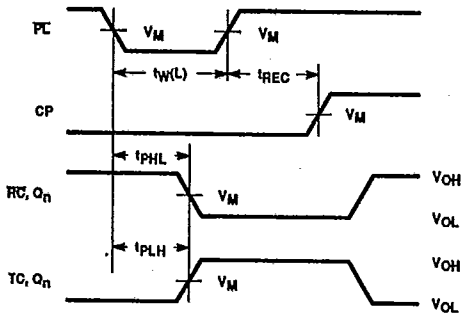
Waveform 2. Propagation Delay, Clock or Clock Enable to Ripple Clock Output and Maximum Clock Frequency



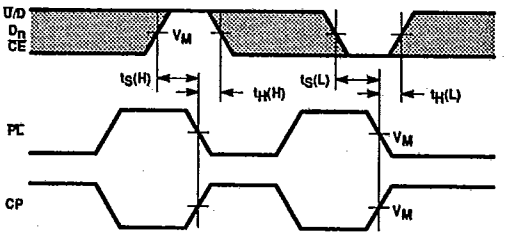
Waveform 3. Non-Inverting Propagation Delays



Waveform 4. Inverting Propagation Delay



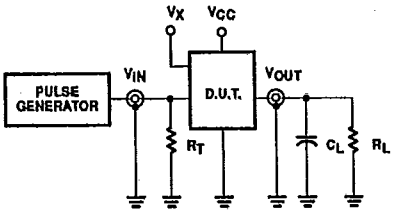
Waveform 5. Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time



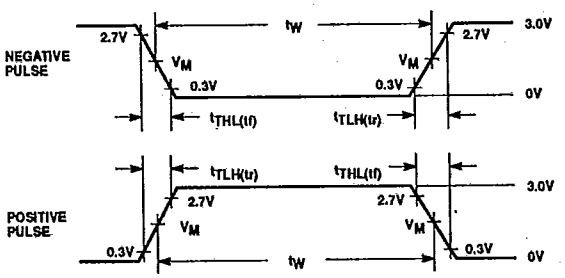
Waveform 6. Set-Up Time and Hold Time for D_n to $\overline{PL}$, U/D to CP and $\overline{CE}$ to CP

V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns