*MAXIM*

# Power-Line Communications (PLC) Integrated Analog Front-End Transceiver

**MAX2991**

## General Description

The MAX2991 power-line communication analog front-end (AFE) is a state-of-the-art integrated circuit that delivers high integration and superb performance, while reducing the total system cost. The MAX2991 is the first AFE specifically designed for OFDM (orthogonal frequency division multiplexing) modulated signal transmission over power lines. Operating in the 10kHz to 490kHz band, the programmable filters allow compliance with CENELEC, FCC, and ARIB standards using the same device.

The MAX2991 transceiver provides two main paths: transmit (Tx) path and receive (Rx) path. The transmit path injects an OFDM modulated signal into the AC or DC line. The transmit path is composed of a digital IIR filter, digital-to-analog converter (DAC), followed by a lowpass filter, and a preline driver. The receiver path is for the signal enhancement, filtering, and digitization of the received signal. The receiver is composed of a low-pass and a highpass filter, a two-stage automatic gain control (AGC), and an analog-to-digital converter (ADC). The integrated AGC maximizes the dynamic range of the signal up to 60dB, while the lowpass filter removes any out-of-band noise, and selects the desired frequency band. The ADC converts the enhanced and amplified input signal to a digital format. An integrated offset cancellation loop minimizes the DC offset.

The MAX2991, along with the MAX2990 PLC baseband modem, delivers the most cost-effective data communication solution over power-line networks in the market. The MAX2991 is specified over the -40°C to +85°C temperature range and is available in a 48-pin LQFP package.

## Features

♦ **Optimized to Operate with the MAX2990 PLC Baseband**

♦ **Integrated Band Select Filter, AGC, and 10-Bit ADC for Rx Path**

♦ **Integrated Wave-Shaping Filter, Programmable Predriver Gain, and 10-Bit DAC for Tx Path**

♦ **Variable Sampling Rate Up to 1.2Msps**

♦ **Built-In 60dB Dynamic Range AGC and DC Offset Cancellation**

♦ **Programmable Filters Operate in the CENELEC, FCC, and ARIB Frequency Bands**

♦ **Single 3.3V Power Supply**

♦ **70mA Typical Supply Current (Half-Duplex Mode)**

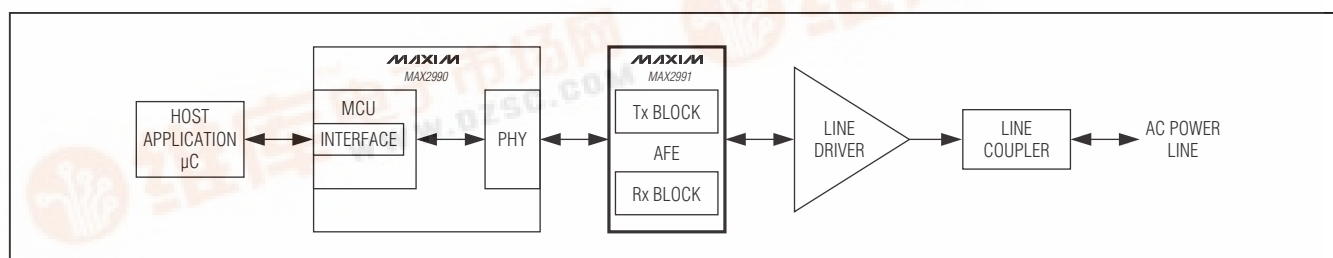♦ **Extended Operating Temperature Range**

## Applications

Automatic Meter Reading

Home Automation

Heating Ventilation and Air Conditioning (HVAC)

Building Automation

Industrial Automation

Lighting Control

Sensor Control and Data Acquisition (SCADA)

Remote Monitoring and Control

Security Systems/Keyless Entry

Smart Grid

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|------|------------|-------------|
| MAX2991ECM+ | -40°C to +85°C | 48 LQFP |

+Denotes a lead(Pb)-free/RoHS-compliant package.

## Typical Application Circuit

*For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.*

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## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND.........................................................-0.3V to +3.9V
All Other Inputs/Outputs........................................-0.3V to +3.9V
Continuous Power Dissipation ($T_A$ = +70°C)
   48-Pin LQFP (derate 25mW/°C above +70°C)..........1535mW

Operating Temperature Range.........................-40°C to +85°C
Junction Temperature ....................................................+150°C
Storage Temperature Range  .........................-60°C to +150°C
Lead Temperature (soldering, 10s) ...............................+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 3.3V, $V_{GND}$ = 0V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS ($f_S$ = 1200ksps)** | | | | | | | |
| Supply Voltage | $V_{DD}$ | | | 3 | 3.3 | 3.6 | V |
| Supply Current | $I_{DD}$ | Rx mode | | | 70 | 100 | mA |
| | | Tx mode | | | 36 | 50 | |
| High-Level Input Voltage | $V_{IH}$ | | | 2 | | | V |
| Low-Level Input Voltage | $V_{IL}$ | | | | | 0.8 | V |
| High-Level Output Voltage | $V_{OH}$ | Source 5mA | | 2.4 | | | V |
| Low-Level Output Voltage | $V_{OL}$ | Sink 5mA | | | | 0.4 | V |
| Input Leakage Current | $I_{IL}$ | | | -5 | | +5 | µA |
| Shutdown Current | $I_{SHDN}$ | Global power-down mode | | | | +5 | µA |
| **AC CHARACTERISTICS ($f_S$ = 1200ksps)** | | | | | | | |
| **TRANSMITTER** | | | | | | | |
| DAC Resolution | | | | | 10 | | Bits |
| DAC Sampling Rate | | | | | | 1200 | ksps |
| DAC Integral Nonlinearity | INL | | | | ±2 | | LSB |
| DAC Differential Nonlinearity | DNL | | | | ±0.5 | | LSB |
| Lowpass Filter Cutoff-Frequency Accuracy | | FCC, ARIB | | | ±5.0 | | % |
| | | CEN A | | | ±3.0 | | |
| | | Narrowband | | | ±5.0 | | |
| | | Full band | | | ±5.0 | | |
| Lowpass Filter -3dB Cutoff Frequency (Note 1) | | FCC, ARIB | | | 470 | | kHz |
| | | CEN A | | | 90 | | |
| | | Narrowband (Note 2) | | | 134 | | |
| | | Full band | | | 560 | | |
| Stopband Attenuation | | Includes digital IIR filter | FCC, ARIB | | 28 | | dB |
| | | | CEN A | | 28 | | |
| | | | Narrowband | | 28 | | |
| | | | Full band | | 28 | | |
| Output-Voltage Swing | | Predriver gain = 0dB, frequency = 50kHz, 50Ω single-ended | | | 1.5 | | $V_{P-P}$ |
| Total Cascaded IM3 | IM3 | In-band (Note 3) | | | -56 | -50 | dBc |
| Predriver Gain Range | | | | | 16 | | dB |

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## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 3.3V, $V_{GND}$ = 0V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **RECEIVER (Note 4)** | | | | | | |
| Input Impedance | | At maximum gain | | 850 | | Ω |
| Receiver Dynamic Range | | | | 60 | | dB |
| Lowpass Filter Cutoff-Frequency Accuracy | | FCC, ARIB | | ±5.0 | | % |
| | | CEN A | | ±3.0 | | |
| | | Narrowband | | ±5.0 | | |
| | | Full band | | ±5.0 | | |
| Lowpass Filter -3dB Cutoff Frequency (Note 1) | | FCC, ARIB | | 490 | | kHz |
| | | CEN A | | 100 | | |
| | | Narrowband (Note 2) | | 140 | | |
| | | Full band | | 560 | | |
| Stopband Attenuation | | FCC, ARIB | | 32 | | dB |
| | | CEN A | | 32 | | |
| | | Narrowband | | 32 | | |
| | | Full band | | 32 | | |
| ADC Resolution | | | | 10 | | Bits |
| ADC Sampling Rate | | | | | 1200 | ksps |
| ADC Integral Nonlinearity | INL | | | ±0.5 | | LSB |
| ADC Differential Nonlinearity | DNL | | | ±0.5 | | LSB |
| Total Cascaded IM3 | IM3 | | | -70 | -60 | dBc |

**Note 1:** Rx and Tx filter transfer functions for different bands are shown in Figure 1.
**Note 2:** The *Applications Information* section shows how to configure the Tx and Rx corner frequencies for different bands.
**Note 3:** Devices are tested with each tone at 0.7$V_{P-P}$ differential using the following two input frequencies:
$f_{IN1}$ = 200kHz and $f_{IN2}$ = 150kHz for FCC and ARIB
$f_{IN1}$ = 50kHz and $f_{IN2}$ = 80kHz for CENELEC A
$f_{IN1}$ = 60kHz and $f_{IN2}$ = 100kHz for narrowband
$f_{IN1}$ = 200kHz and $f_{IN2}$ = 300kHz for full band
**Note 4:** The parameters were tested using the external highpass filter circuit in Figure 10.

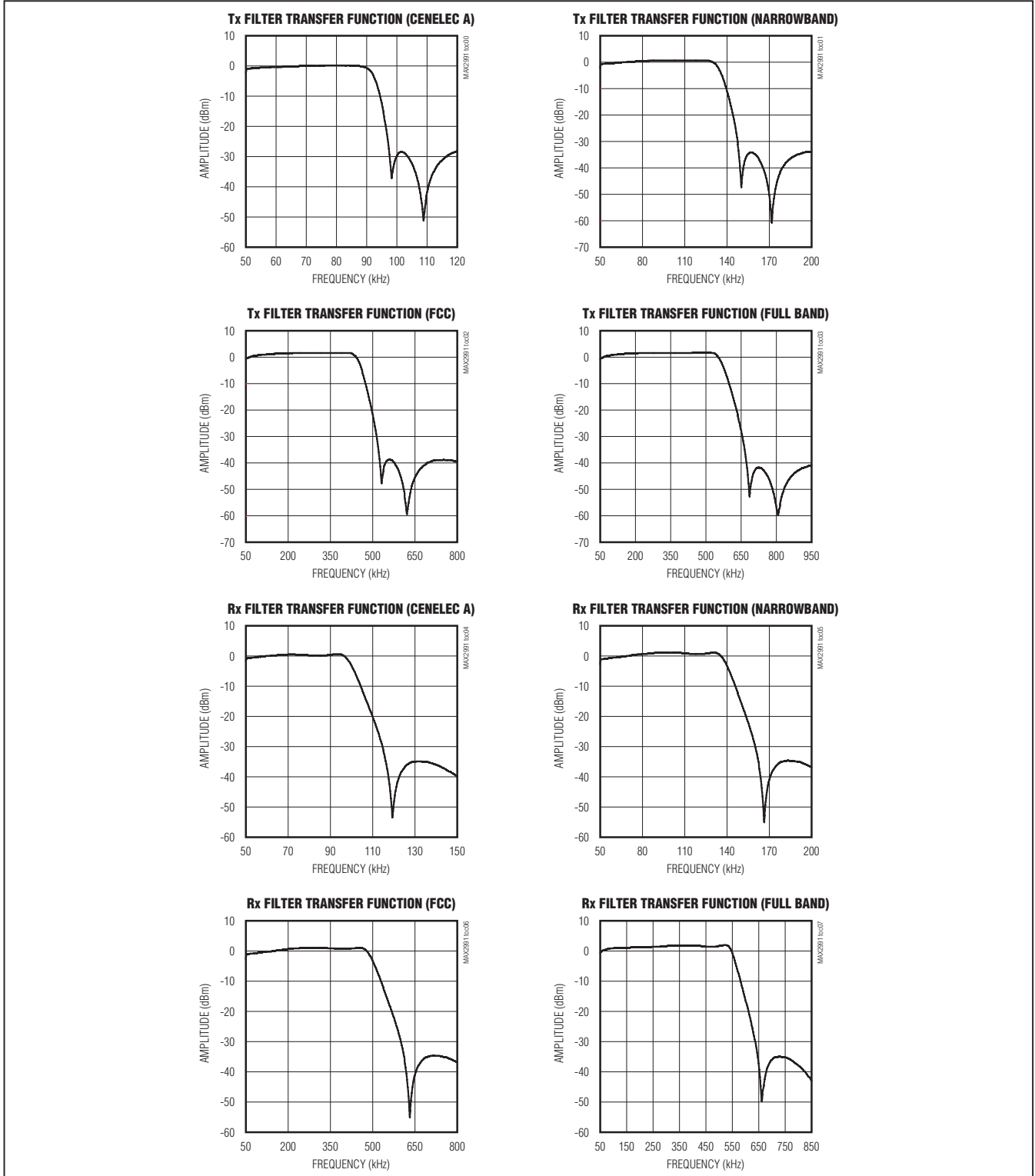# Power-Line Communications (PLC) Integrated Analog Front-End Transceiver

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Figure 1. Rx and Tx Filter Transfer Functions for Different Bands

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# Power-Line Communications (PLC) Integrated Analog Front-End Transceiver

## SPI™ TIMING CHARACTERISTICS (Figure 2)

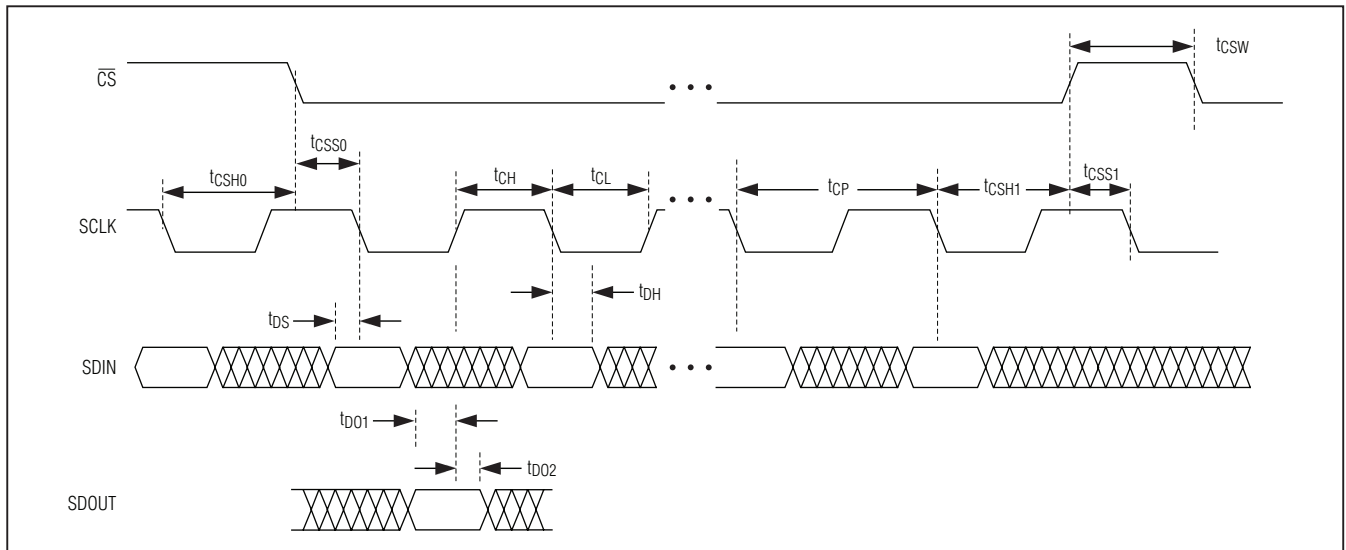| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SCLK Frequency | $f_{CLK}$ | | | | 20 | MHz |
| SCLK Clock Period | $t_{CP}$ | | 50 | | | ns |
| SCLK Pulse-Width High | $t_{CH}$ | | 20 | | | ns |
| SCLK Pulse-Width Low | $t_{CL}$ | | 20 | | | ns |
| $\overline{CS}$ Low to SCLK Setup | $t_{CSS0}$ | | 10 | | | ns |
| $\overline{CS}$ Low After SCLK Hold | $t_{CSH0}$ | | 10 | | | ns |
| $\overline{CS}$ High to SCLK Setup | $t_{CSS1}$ | | 10 | | | ns |
| $\overline{CS}$ High After SCLK Hold | $t_{CSH1}$ | | 10 | | | ns |
| $\overline{CS}$ Pulse-Width High | $t_{CSW}$ | | 20 | | | ns |
| SDIN to SCLK Setup | $t_{DS}$ | | 10 | | | ns |
| SDIN Hold After SCLK | $t_{DH}$ | | 10 | | | ns |
| SDOUT Valid Before SCLK | $t_{DO1}$ | | 20 | | | ns |
| SDOUT Valid After SCLK | $t_{DO2}$ | | 5 | | | ns |



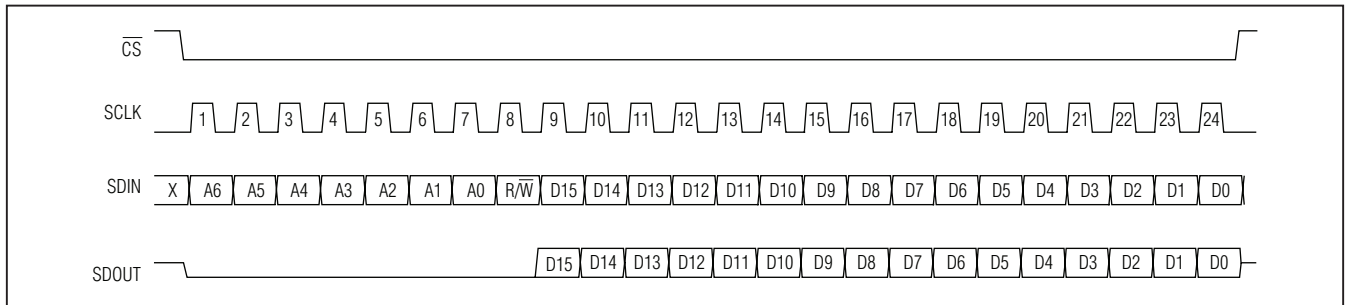Figure 2. SPI Interface Timing Diagram



Figure 3. SPI Communication Protocol

SPI is a trademark of Motorola, Inc.

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## AFE INTERFACE TIMING CHARACTERISTICS (Rx) (Figure 4)

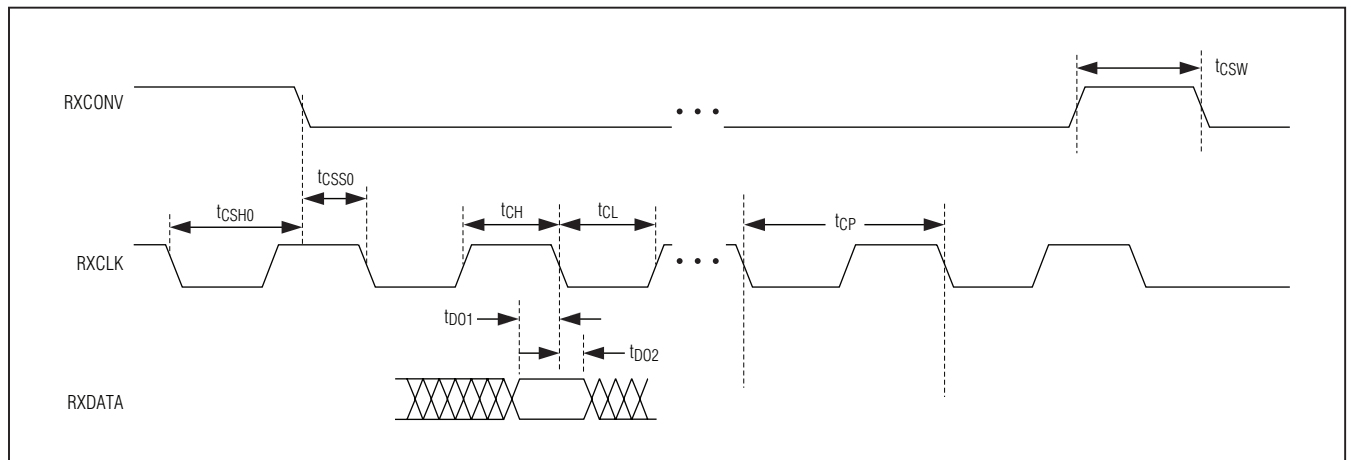| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| RXCLK Frequency | $f_{CLK}$ | | | | 20 | MHz |
| RXCLK Clock Period | $t_{CP}$ | | 50 | | | ns |
| RXCLK Pulse-Width High | $t_{CH}$ | | 20 | | | ns |
| RXCLK Pulse-Width Low | $t_{CL}$ | | 20 | | | ns |
| RXCONV Low to RXCLK Setup | $t_{CSS0}$ | | 10 | | | ns |
| RXCONV Low After RXCLK Hold | $t_{CSH0}$ | | 10 | | | ns |
| RXCONV Pulse-Width High | $t_{CSW}$ | | 15 | | | ns |
| RXDATA Valid Before RXCLK | $t_{DO1}$ | | 20 | | | ns |
| RXDATA Valid After RXCLK | $t_{DO2}$ | | 15 | | | ns |



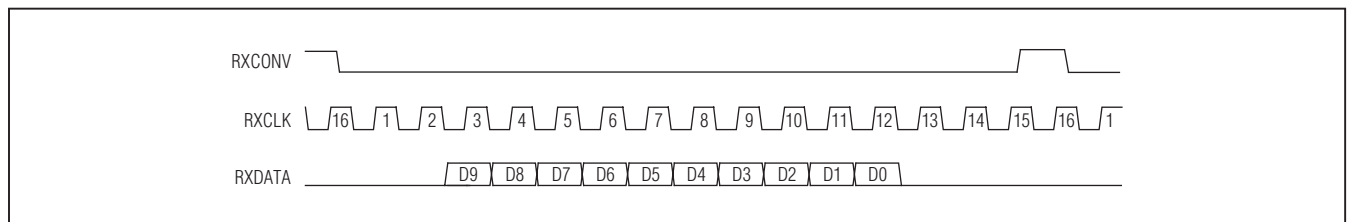Figure 4. AFE Interface Timing Diagram (Rx)



Figure 5. Rx Communication Protocol (Slave)

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## AFE INTERFACE TIMING CHARACTERISTICS (Tx) (Figure 6)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| TXCLK Frequency | $f_{CLK}$ | | | | 20 | MHz |
| TXCLK Clock Period | $t_{CP}$ | | 50 | | | ns |
| TXCLK Pulse-Width High | $t_{CH}$ | | 10 | | | ns |
| TXCLK Pulse-Width Low | $t_{CL}$ | | 10 | | | ns |
| TXCONV Low to TXCLK Setup | $t_{CSS0}$ | | 10 | | | ns |
| TXCONV Low After TXCLK Hold | $t_{CSH0}$ | | 10 | | | ns |
| TXCONV High to TXCLK Setup | $t_{CSS1}$ | | 10 | | | ns |
| TXCONV High After RXCLK Hold | $t_{CSH1}$ | | 10 | | | ns |
| TXCONV Pulse-Width High | $t_{CSW}$ | | 15 | | | ns |
| TXDATA to TXCLK Setup | $t_{DS}$ | | 5 | | | ns |
| TXDATA Hold After TXCLK | $t_{DH}$ | | 10 | | | ns |
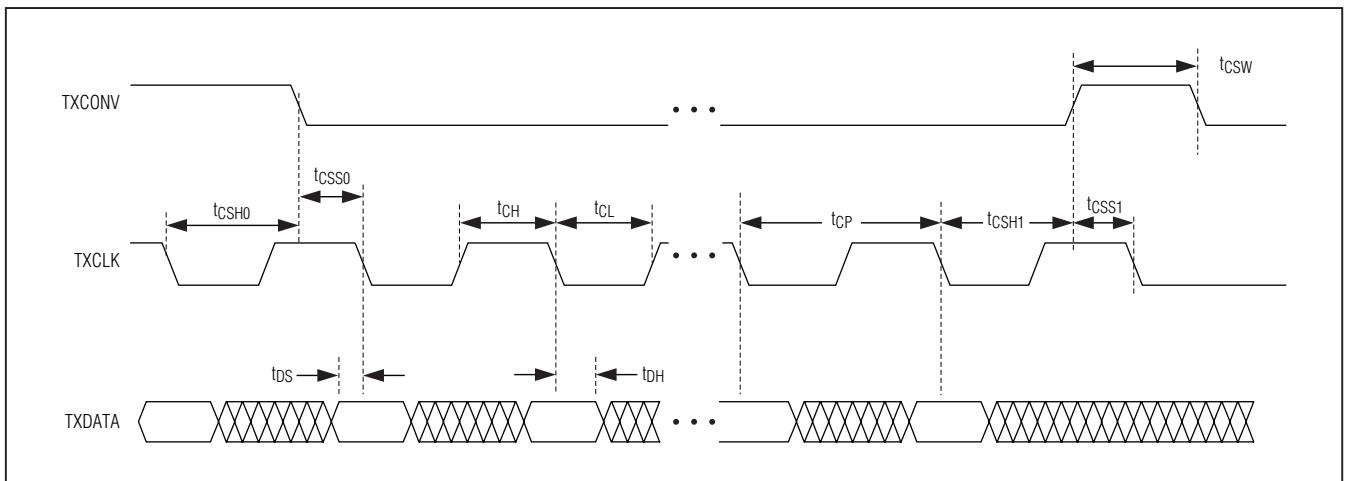


Figure 6. AFE Interface Timing Diagram (Tx)
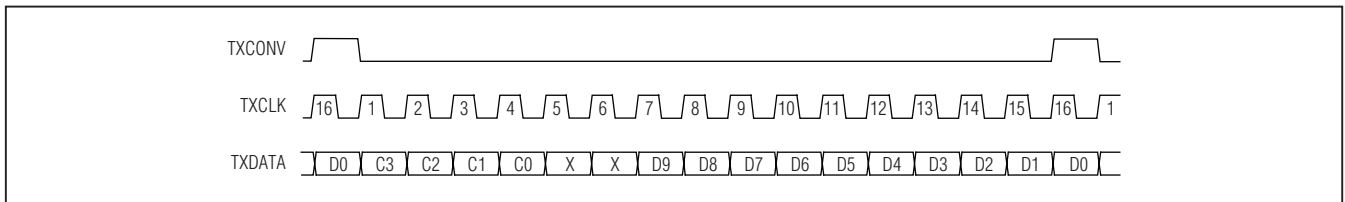


Figure 7. Tx Communication Protocol (Master)

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## Pin Configuration



LQFP
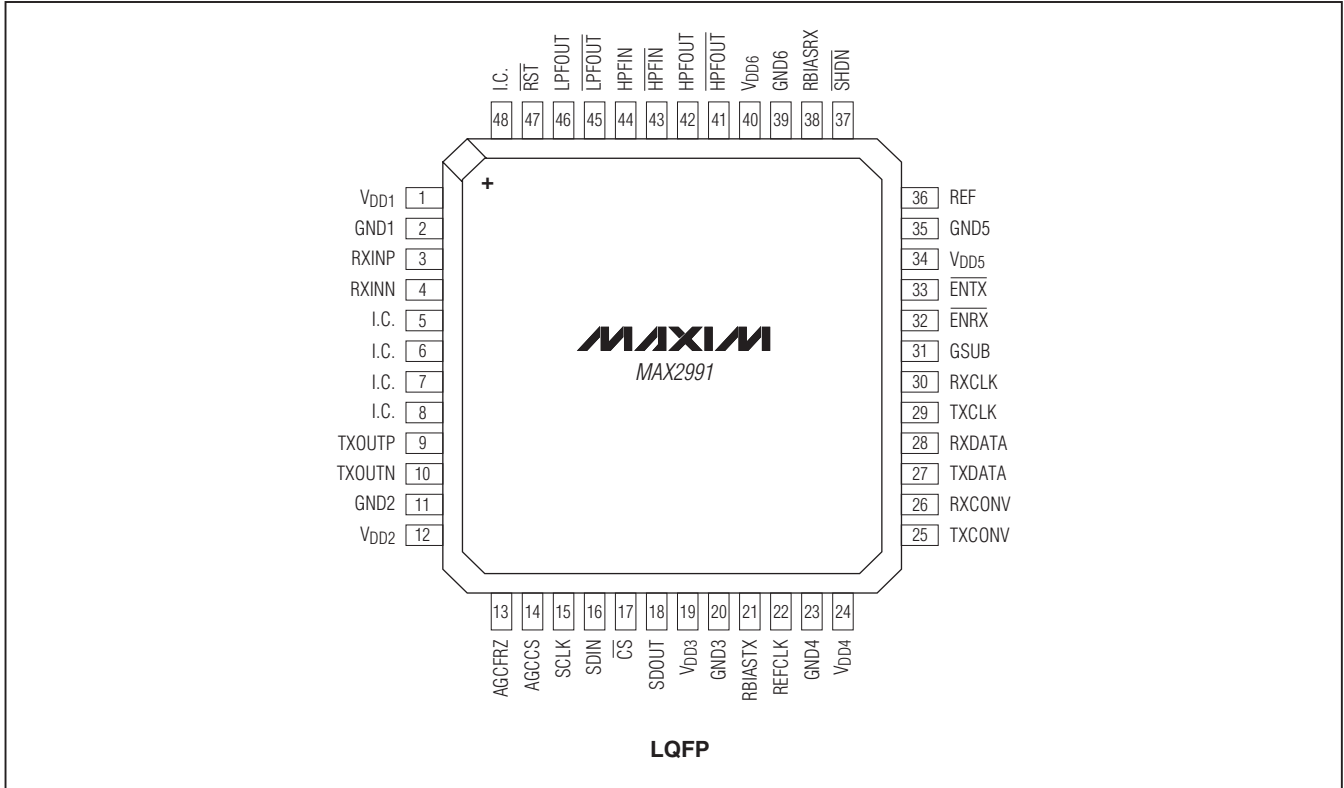
## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | $V_{DD1}$ | Analog Power-Supply 1. Bypass to GND1 with 100nF and 10µF capacitors in parallel located close to $V_{DD1}$. Connect $V_{DD}$ inputs together. |
| 2 | GND1 | Analog Ground 1. Connect GND1 to the PCB ground. |
| 3 | RXINP | AC Power-Line Positive Input |
| 4 | RXINN | AC Power-Line Negative Input |
| 5, 6, 48 | I.C. | Internal Connection. Connect to the PCB ground. |
| 7, 8 | I.C. | Internal Connection. Leave unconnected. |
| 9 | TXOUTP | AC Power-Line Positive Output |
| 10 | TXOUTN | AC Power-Line Negative Output |
| 11 | GND2 | Analog Ground 2. Connect GND2 to the PCB ground. |
| 12 | $V_{DD2}$ | Analog Power-Supply 2. Bypass to GND2 with 100nF and 10µF capacitors in parallel located close to $V_{DD2}$. Connect $V_{DD}$ inputs together. |
| 13 | AGCFRZ | Active-High AGC Freeze-Mode Enable. Drive AGCFRZ high to place the AGC adaptation in freeze mode. Drive AGCFRZ low to allow continuous AGC adaptation. |

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*Pin Description (continued)*

| PIN | NAME | FUNCTION |
|-----|------|----------|
| 14 | AGCCS | Active-High AGC Carrier-Select Enable. Drive AGCCS high to initiate the internal AGC adaptation timer. |
| 15 | SCLK | Host SPI Serial-Clock Input |
| 16 | SDIN | Host SPI Serial-Data Input |
| 17 | $\overline{CS}$ | Active-Low Host SPI Chip-Select Input |
| 18 | SDOUT | Host SPI Serial-Data Output |
| 19 | $V_{DD3}$ | Analog Power-Supply 3. Bypass to GND3 with 100nF and 10μF capacitors in parallel located close to $V_{DD3}$. Connect $V_{DD}$ inputs together. |
| 20 | GND3 | Analog Ground 3. Connect GND3 to the PCB ground. |
| 21 | RBIASTX | Transmitter Bias. Connect a 25kΩ resistor with 1% accuracy rating between RBIASTX and the PCB ground to set the bias current for the transmitter path. |
| 22 | REFCLK | Analog Reference Clock Input |
| 23 | GND4 | Digital Ground. Connect GND4 to the PCB ground. |
| 24 | $V_{DD4}$ | Digital Power Supply. Bypass to GND4 with 100nF and 10μF capacitors in parallel located close to $V_{DD4}$. Connect $V_{DD}$ inputs together. |
| 25 | TXCONV | Transmit DAC Conversion Start. The beginning of the Tx conversion data frame is signaled by the falling edge of TXCONV. |
| 26 | RXCONV | Receive ADC Conversion Start. Rx data is sampled by the ADC and conversion begins on the falling edge of RXCONV. |
| 27 | TXDATA | Transmit Path Serial-Data Input. Data is latched on the falling edge of the TXCLK. |
| 28 | RXDATA | Receive Path Serial-Data Output. Data is clocked out on the falling edge of RXCLK. |
| 29 | TXCLK | Transmit Path Serial Clock |
| 30 | RXCLK | Receive Path Serial Clock |
| 31 | GSUB | Substrate Ground. Make low resistance and low inductance connection to the PCB ground. |
| 32 | $\overline{ENRX}$ | Active-Low Receive Enable. Drive $\overline{ENRX}$ low to enable the receiver. Drive $\overline{ENRX}$ high to disable the receiver. |
| 33 | $\overline{ENTX}$ | Active-Low Transmit Enable. Drive $\overline{ENTX}$ low to enable the transmitter. Drive $\overline{ENTX}$ high to disable the transmitter and place predriver outputs into three-state. |
| 34 | $V_{DD5}$ | Analog Power-Supply 5. Bypass to GND5 with 100nF and 10μF capacitors in parallel located close to $V_{DD5}$. Connect $V_{DD}$ inputs together. |
| 35 | GND5 | Analog Ground 5. Connect GND5 to the PCB ground. |
| 36 | REF | ADC Reference Voltage Output. Internal 2.0V reference output. Bypass REF with parallel 100nF and 10μF capacitors to the ADC ground. |
| 37 | $\overline{SHDN}$ | Active-Low Shutdown Input. Drive $\overline{SHDN}$ low to place the MAX2991 into shutdown mode. Drive $\overline{SHDN}$ high for normal operation. |
| 38 | RBIASRX | Receive Bias. RBIASRX is the external resistor connection that sets the bias current for the receive path. Connect a 25kΩ resistor with 1% accuracy rating between RBIASRX and the PCB ground. |
| 39 | GND6 | Analog Ground 6. Connect GND6 to the PCB ground. |
| 40 | $V_{DD6}$ | Analog Power-Supply 6. Bypass to GND6 with parallel 100nF and 10μF capacitors located close to $V_{DD6}$. Connect $V_{DD}$ inputs together. |
| 41 | $\overline{HPFOUT}$ | Highpass Filter Negative Output |
| 42 | HPFOUT | Highpass Filter Positive Output |

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## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 43 | $\overline{\text{HPFIN}}$ | Highpass Filter Negative Input |
| 44 | HPFIN | Highpass Filter Positive Input |
| 45 | $\overline{\text{LPFOUT}}$ | Lowpass Filter Negative Output |
| 46 | LPFOUT | Lowpass Filter Positive Output |
| 47 | $\overline{\text{RST}}$ | Active-Low Reset Input. Drive $\overline{\text{RST}}$ low to place the MAX2991 in reset mode. Leave Rx and Tx clocks in free-running mode during a reset. The minimum reset pulse width is 100ns. Connect $\overline{\text{RST}}$ to V$_{DD}$ for normal operation. |

## Functional Diagram
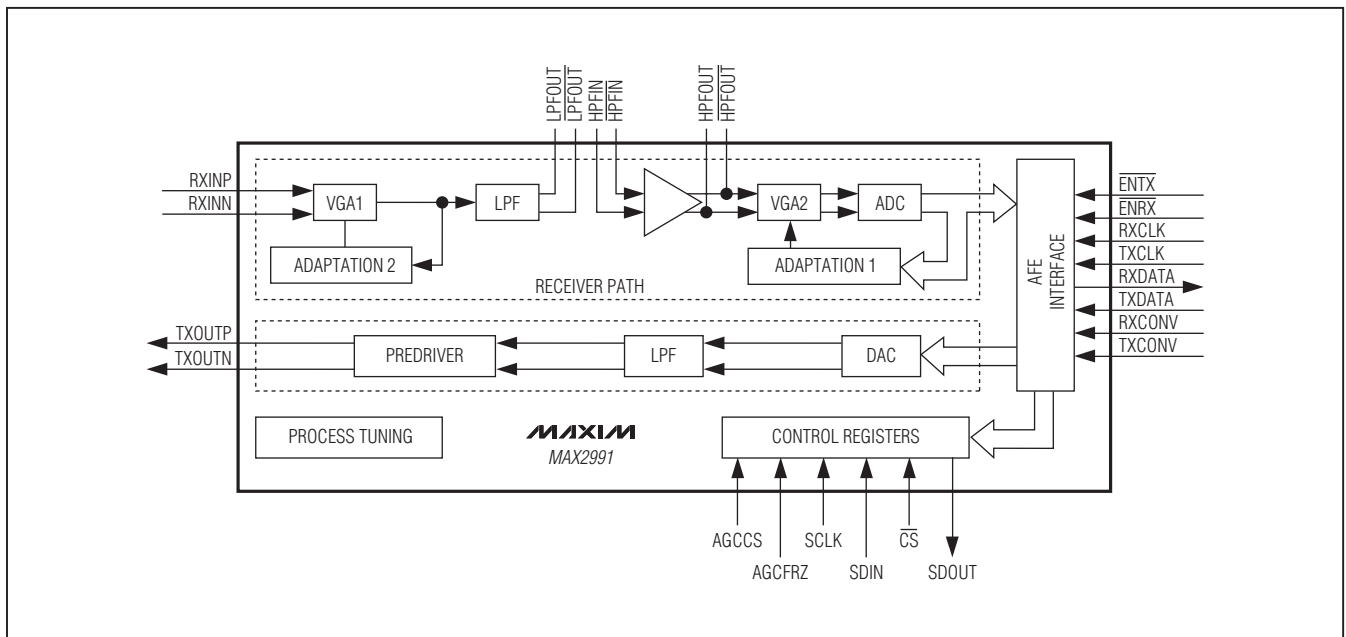
# Power-Line Communications (PLC) Integrated Analog Front-End Transceiver

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## Detailed Description

The MAX2991 power-line AFE integrated circuit is a state-of-the-art CMOS device that delivers high performance and low cost. This highly integrated design combines an ADC, DAC, signal conditioning, and predriver as shown in the *Functional Diagram*. The MAX2991 meets all frequency band requirements of the various popular power-line standards such as FCC, ARIB, and CENELEC.

The MAX2991 along with the MAX2990 PLC baseband modem deliver the most cost-effective data communication solution over power-line networks in the market. The advanced design of the MAX2991 allows operation without external controls, enabling simplified connection to a variety of third-party power-line digital PHY devices. The MAX2991 includes various control signals to achieve additional power reduction.

### Receive Channel

The receiver channel consists of a low-noise variable-gain amplifier (VGA1) followed by a lowpass filter (LPF), a highpass filter (HPF), and another variable-gain amplifier (VGA2) circuit. An ADC samples the VGA2 output. An AFE interface provides data communication to the digital PHY device.

The variable-gain low-noise amplifier reduces the receiver channel input-referred noise by providing additional signal gain to the AFE input. The filter blocks remove any out-of-band noise, provide anti-aliasing, and select a proper AFE bandwidth. Using the adaptation blocks, the VGAs scale the received signal to maintain the optimum signal level at the ADC input.

The 10-bit ADC samples the analog signal and converts it to a 10-bit digital stream with a maximum 1.2Msps sampling rate.

### Transmit Channel

The transmit channel consists of a 10-bit DAC, an image-reject lowpass filter, and a programmable-gain predriver. The DAC receives the data stream from the digital PHY device through the AFE interface. The 10-bit DAC provides a complementary function to the receive channel with a maximum 1.2Msps sampling rate. The DAC converts the 10-bit digital stream to an analog voltage.

The lowpass filter removes spurs and harmonics adjacent to the desired passband to reduce any out-of-band transmitted frequencies and energy from the DAC output. The lowpass filter ensures that the transmitted signal meets bandwidth requirements specified by the different wideband and narrowband standards.

The predriver controls the output level of the lowpass filter connected to an external line driver, which, in turn, connects to the power-line medium. The output level is adjustable by the predriver gain control that provides up to 6dB gain and 10dB attenuation.

### Serial Interface

The MAX2991 features two separate serial interfaces: host SPI interface and AFE interface. The host SPI interface provides direct access to the MAX2991 configuration registers, while the AFE interface allows data communication with the PLC baseband modem (MAX2990) and also provides indirect access to the MAX2991 configuration registers.

### Host SPI Interface

The MAX2991 host SPI interface provides access to the configuration registers using $\overline{CS}$, SCLK, SDIN, and SDOUT. A host SPI frame consists of a 7-bit register address, a read/write bit, and 16 bits of data. Data is driven on the rising edge of SCLK and sampled on the falling edge of SCLK. Figure 3 shows a valid host SPI communication protocol.

### AFE Interface

The AFE interface allows the MAX2991 to communicate with the PLC baseband modem (MAX2990) through a transmit channel (TXCLK, TXDATA, TXCONV) and a receive channel (RXCLK, RXDATA, RXCONV), and provides indirect access to the MAX2991 configuration registers. See the *Interfacing to the MAX2990 Baseband* section for connection details.

### AFE Interface Transmit Enable ($\overline{ENTX}$)

$\overline{ENTX}$ enables the transmitter of the MAX2991 AFE circuit. A logic-high on $\overline{ENTX}$ powers down the MAX2991 transmitter.

### AFE Interface Receiver Enable ($\overline{ENRX}$)

$\overline{ENRX}$ enables the receiver on the MAX2991. A logic-high on $\overline{ENRX}$ powers down the MAX2991 receiver.

### AFE Interface Tx Clock (TXCLK)

The TXCLK signal provides the clock to the MAX2991 AFE transmitter. Apply a 19.2MHz clock at TXCLK to achieve 1.2Msps data rate.

### AFE Interface Rx Clock (RXCLK)

The RXCLK signal provides the clock to the MAX2991 AFE receiver. Apply a 19.2MHz clock at RXCLK to achieve 1.2Msps data rate.

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### AGC Control Signals (AGCCS)

The AGCCS signal controls the AGC circuit of the receive path in the MAX2991. A logic-low on AGCCS sets the gain circuit on the input signal to continuously adapt for maximum sensitivity. A valid preamble detected by the digital PHY raises AGCCS to high. While AGCCS is high, the AGC continues to adapt for an additional programmable delay, then the AGC locks the currently adapted level on the incoming signal. The digital PHY holds AGCCS high while receiving a transmission and then lowers AGCCS for continuous adaptation for maximum sensitivity of other incoming signals.

### AGC Freeze Mode (AGCFRZ)

Use the AGCFRZ signal to instantly lock the VGA1 and VGA2 gains.

### Reset Input ($\overline{RST}$)

The $\overline{RST}$ signal provides reset control for the MAX2991. Drive $\overline{RST}$ low to place the MAX2991 in reset mode. Leave Rx and Tx clocks in free-running mode during a reset. The minimum reset pulse width is 100ns.

### Power-Down Modes

The MAX2991 features four power-down modes:

1) Global Power-Down Mode: Enter this mode either by setting the $\overline{SHDN}$ input to logic-low or by setting the CHIPENB bit (bit 0 of RXCONF register) to 1. All clocks to the digital circuitry are gated. Set $\overline{SHDN}$ to logic-high or set the CHIPENB bit to logic-low to exit this mode. The Tx and Rx blocks are fully operational approximately 20µs after coming out of global power-down mode.

2) Idle Mode: Enter this mode by setting the IDLEEN bit to 1. In this mode, all blocks are powered down except for the AFE interface and the bias blocks. RXCLK and TXCLK are not gated. Set IDLEEN to 0 to exit this mode. The Tx and Rx blocks are fully operational approximately 20µs after coming out of global power-down mode.

3) Transmit Power-Down Mode: Enter this mode by setting $\overline{ENTX}$ to logic-high while the ENTXBEN bit (bit 0 of register TXCONF) is set to 1. In this mode, the transmit predriver, lowpass filter, and the DAC are powered down. Set $\overline{ENTX}$ to logic-low to exit this mode. The Tx block is fully operational approximately 15µs after coming out of global power-down mode.

4) Receive Power-Down Mode: Enter this mode by setting $\overline{ENRX}$ to logic-high while the ENRXBEN bit (bit 2 of register RXCONF) is set to 1. In this mode, the receiver VGA1, VGA2, lowpass filter, lowpass filter buffer, highpass filter, and the ADC are powered down. Set $\overline{ENRX}$ to logic-low to exit this mode. The Rx block is fully operational approximately 20µs after coming out of global power-down mode.

### Register Map

Table 1 shows the MAX2991 register map.

## Table 1. Register Map

| REGISTER | WIDTH | ADDRESS | FUNCTION | DEFAULT |
|----------|-------|---------|----------|---------|
| RXCONF | <13:0> | 0x00 | Rx configuration and control | 0x0004 |
| TXCONF | <15:0> | 0x01 | Tx configuration and control | 0x282B |
| — | <13:0> | 0x02 | Reserved | 0x000 |
| PTUN1 | <5:0> | 0x03 | Process tuner configuration and control | 0x13 |
| PTUN2 | <13:0> | 0x04 | Process tuner manual override | 0x0000 |
| — | <11:0> | 0x05 | Reserved | 0xE8E |
| — | <11:0> | 0x06 | Reserved | 0xE00 |
| AGC3 | <13:0> | 0x07 | AGC configuration and control | 0x0320 |
| — | <13:0> | 0x08 | Reserved | 0x0000 |
| — | <14:0> | 0x09 | Reserved | 0x0200 |
| — | <15:0> | 0x0A | Reserved | 0x0000 |
| — | <9:0> | 0x0B | Reserved | 0x000 |
| IIR0CONF | <8:0> | 0x0C | IIR filter configuration of first biquad | 0x0ED |
| IIR0B0 | <15:0> | 0x0D | IIR filter B0 coefficient of first biquad | 0x0825C |
| IIR0B1 | <15:0> | 0x0E | IIR filter B1 coefficient of first biquad | 0xF43A |

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## Table 1. Register Map (continued)

| REGISTER | WIDTH | ADDRESS | FUNCTION | DEFAULT |
|----------|-------|---------|----------|---------|
| IIR0B2 | <15:0> | 0x0F | IIR filter B2 coefficient of first biquad | 0x0825 |
| IIR0A1 | <15:0> | 0x10 | IIR filter A1 coefficient of first biquad | 0xCEFF |
| IIR0A2 | <15:0> | 0x11 | IIR filter A2 coefficient of first biquad | 0x1613 |
| IIR1CONF | <8:0> | 0x12 | IIR filter configuration of second biquad | 0x0ED |
| IIR1B0 | <15:0> | 0x13 | IIR filter B0 coefficient of second biquad | 0x1DAA |
| IIR1B1 | <15:0> | 0x14 | IIR filter B1 coefficient of second biquad | 0xCBEF |
| IIR1B2 | <15:0> | 0x15 | IIR filter B2 coefficient of second biquad | 0x1DAA |
| IIR1A1 | <15:0> | 0x16 | IIR filter A1 coefficient of second biquad | 0xC7F6 |
| IIR1A2 | <15:0> | 0x17 | IIR filter A2 coefficient of second biquad | 0x1F4D |
| DPTUN1 | <11:0> | 0x18 | Process tuner digital settings | 0x3F4 |
| DPTUN2 | <11:0> | 0x19 | Process tuner digital settings | 0x006 |
| FRZTIME | <11:0> | 0x1A | Freeze timer control | 0x5C6 |

## Address 0x00: Rx Configuration (RXCONF<13:0>), Default: 0x0004

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|----------|--------------------|---------|----------|
| CHIPENB | 0 | 0 | Active-high global power-down bit. Set to 1 to enable global power-down mode. |
| IDLEEN | 1 | 0 | Active-high idle mode-enable bit. Set to 1 to enable idle mode. |
| ENRXBEN | 2 | 1 | Active-high receiver path shutdown bit. Set to 1 to power down the receive path. The receiver is normally shut down in transmit mode. |
| BYPRXHPF | 3 | 0 | Active-high receiver HPF bypass bit. Set to 1 to allow receive HPF bypass. |
| RXLPFBW<1:0> | 5, 4 | 00 | Receiver lowpass filter mode selection.<br>00: CENELEC A<br>01: Narrowband<br>10: FCC and ARIB<br>11: Full band |
| — | 11–6 | 000000 | Reserved |
| RDCONFMDEN | 12 | 0 | Set to 1 to enable the read configuration mode of the AFE interface. |
| RXCONV_EDGE | 13 | 0 | This bit defines the active RXCLK edge used to sample the RXCONV input (0 = rising edge, 1 = falling edge). |

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## Address 0x01: Tx Configuration (TXCONF<15:0>), Default: 0x282B

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| ENTXBEN | 0 | 1 | Active high. Set to 1 to enable the power down of the transmit path. The transmit path is normally powered down in receive mode. |
| PREDRVGAIN <3:0> | 4–1 | 0101 | Predriver gain settings:<br>0000: Gain = -10dB<br>0001: Gain = -8dB<br>0010: Gain = -6dB<br>0011: Gain = -4dB<br>0100: Gain = -2dB<br>0101: Gain = 0dB<br>0110: Gain = 2dB<br>0111: Gain = 4dB<br>1000: Gain = 6dB |
| — | 5 | 1 | Reserved |
| TXLPFBW<1:0> | 7, 6 | 00 | Transmit lowpass filter mode selection.<br>00: CENELEC A<br>01: Narrowband<br>10: FCC and ARIB<br>11: Full band |
| — | 12–8 | 01000 | Reserved |
| PREDRDYN | 13 | 1 | Active high. Enables the dynamic control of the predriver gain set by the command bits C<3:0> in the Tx transmit frame. |
| TXCONV_EDGE | 14 | 0 | Defines the active TXCLK edge used to sample the TXCONV input (0 = falling edge, 1 = rising edge). |
| TXDATA_DLY | 15 | 0 | Defines the position of the first TXDATA bit relative to the TXCONV active edge (0 = first TXDATA bit is coincident with the first active TXCONV cycle, 1 = first TXDATA bit is one cycle after the first active TXCONV cycle). |

## Address 0x03: Process Tuner Configuration (PTUN1<5:0>), Default: 0x13

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| — | 1, 0 | 11 | Reserved |
| OVERWRT_NDGE | 2 | 0 | Active high. Enables direct programming of process tuner settings from SPI registers. Set to 0 to enable systematic adjustment of the process tuner code by PTUNERXADJ and PTUNETXADJ independently for Rx and Tx filters, respectively. |
| PTCLKMUX | 4, 3 | 10 | Process tuner clock selection:<br>00 or 01: REFCLK<br>10: RXCLK<br>11: TXCLK |
| — | 5 | 0 | Reserved |

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## Address 0x04: Process Tuner Adjust (PTUN2<13:0>), Default: 0x0000

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| PTUNERXADJ <6:0> | 6–0 | 0000000 | Adjust bits to set Rx filter process code slightly different from process tuner output code. MSB is used as sign bit. |
| PTUNETXADJ <6:0> | 13–7 | 0000000 | Adjust bits to set Tx filter process code slightly different from process tuner output code. MSB is used as sign bit. |

## Address 0x07: AGC Control 3 (AGC3<13:0>), Default: 0x0320

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| — | 10–0 | 01100100000 | Reserved |
| EN30U | 11 | 0 | Enables the programmable freeze signal delay set by FRZTIMEOFF2. When disabled, the default delay is 400 ADC clock cycles (1 = enable). |
| — | 13, 12 | 00 | Reserved |

## Address 0x0C: IIR0 1st Biquad Configuration (IIR0CONF<8:0>), Default: 0x0ED

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| IIR0_CONF | 0 | 1 | Set to 1 to enable the first biquad of the IIR filter. Set to 0 to bypass the first biquad. |
| — | 8–1 | 01110110 | Reserved |

## Address 0x0D: IIR0 B0 Coefficient (IIR0B0<15:0>), Default: 0x0825C

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| IIR0_B0<15:0> | 15–0 | 2085 | B0 coefficient of the first biquad of the IIR filter. |

## Address 0x0E: IIR0 B1 Coefficient (IIR0B1<15:0>), Default: 0xF43A

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| IIR0_B1<15:0> | 15–0 | -3014 | B1 coefficient of the first biquad of the IIR filter. |

## Address 0x0F: IIR0 B2 Coefficient (IIR0B2<15:0>), Default: 0x0825

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| IIR0_B2<15:0> | 15–0 | 2085 | B2 coefficient of the first biquad of the IIR filter. |

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### Address 0x10: IIR0 A1 Coefficient (IIR0A1<15:0>), Default: 0xCEFF

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| IIR0_A1<15:0> | 15–0 | -12545 | A1 coefficient of the first biquad of the IIR filter. |

### Address 0x11: IIR0 A2 Coefficient (IIR0A2<15:0>), Default: 0x1613

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| IIR0_A2<15:0> | 15–0 | 5651 | A2 coefficient of the first biquad of the IIR filter. |

### Address 0x12: IIR1 2nd Biquad Configuration (IIR1CONF<8:0>), Default: 0x0ED

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| IIR1_CONF | 0 | 1 | Set to 1 to enable the second biquad of the IIR filter. Set to 0 to bypass the second biquad. |
| — | 8–1 | 01110110 | Reserved |

### Address 0x13: IIR1 B0 Coefficient (IIR1B0<15:0>), Default: 0x1DAA

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| IIR1_B0<15:0> | 15–0 | 7594 | B0 coefficient of the second biquad of the IIR filter. |

### Address 0x14: IIR1 B1 Coefficient (IIR1B1<15:0>), Default: 0xCBEF

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| IIR1_B1<15:0> | 15–0 | -13329 | B1 coefficient of the second biquad of the IIR filter. |

### Address 0x15: IIR1 B2 Coefficient (IIR1B2<15:0>), Default: 0x1DAA

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| IIR1_B2<15:0> | 15–0 | 7594 | B2 coefficient of the second biquad of the IIR filter. |

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### Address 0x16: IIR1 A1 Coefficient (IIR1A1<15:0>), Default: 0xC7F6

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| IIR1_A1<15:0> | 15–0 | -14346 | A1 coefficient of the second biquad of the IIR filter. |

### Address 0x17: IIR1 A2 Coefficient (IIR1A2<15:0>), Default: 0x1F4D

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| IIR1_A2<15:0> | 15–0 | 8013 | A2 coefficient of the second biquad of the IIR filter. |

### Address 0x18: Process Tuner Digital Settings 1 (DPTUN1<11:0>), Default: 0x3F4

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| PTUNEUPLIMIT <11:0> | 11–0 | 001111110100 | Used to set process tune ramp down limit of clock cycles. PTUNEUPLIMIT along with PTUNEHYS set up the RC time constant range for the filters. |

### Address 0x19: Process Tuner Digital Settings 2 (DPTUN2<11:0>), Default: 0x006

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| PTUNEHYS <11:0> | 11–0 | 000000000110 | Used to set process tune ramp down hysteresis range of clock cycles. PTUNEHYS along with PTUNEUPLIMIT set up the RC time constant range for the filters. |

### Address 0x1A: AGC Freeze Timer (FRZTIME<11:0>), Default: 0x5C6

| BIT NAME | LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|---|---|---|---|
| — | 5–0 | 00110 | Reserved |
| FRZTIMEOFF2 <5:0> | 11–6 | 10111 | Sets AGC gain freeze time offset. Internal timer is 12 bits and lower 6-bit word is 0x1C (1500 ADC clock-cycle delay). EN30U (bit 11) should be set to use this mode. |

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## Table 2. Process Tuner Configuration, PTUN1<5:0>, Address: 0x03, Default: 0x13

| BIT NAME | LOCATION | DEFAULT | FUNCTION |
|----------|----------|---------|----------|
| PTCLKMUX | 4, 3 | 10 | Process tuner clock selection:<br>00 or 01: REFCLK<br>10: RXCLK<br>11: TXCLK |

## Table 3. Summary of Calculations Needed when Process Tuner Clock Rate is Changed

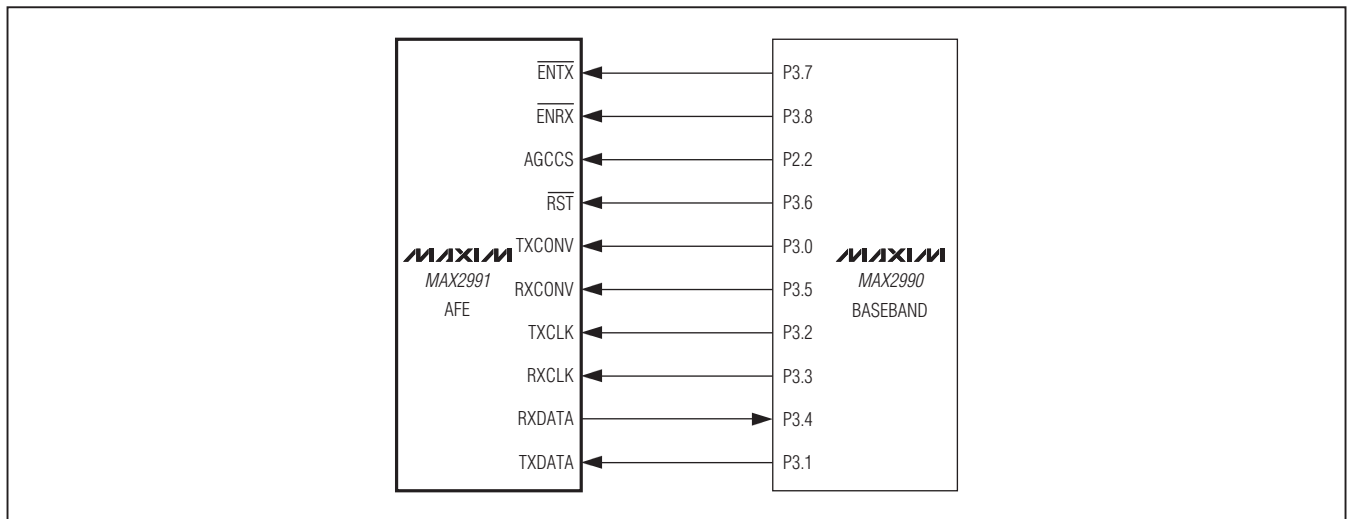| CLOCK RATE (MHz) | COUNTER LIMIT (52.7 x FREQUENCY) | DPTUN1 | HYSTERESIS RANGE (0.3125 x FREQUENCY) | DPTUN2 |
|---|---|---|---|---|
| 19.2 | 1011.84 | 0x3F4 | 6.0 | 0x006 |
| 9.6 | 505.92 | 0x1F9 | 3.0 | 0x003 |



*Figure 8. Interfacing with the MAX2990.*

## Applications Information

### Programming the Process Tuner Reference Clock

The MAX2991 uses a reference clock to tune Rx and Tx filters. In default mode, Rx clock is used as the reference source for the process tuner. Process tuner clock can be set to any one of RXCLK, TXCLK, or REFCLK clock sources. PTUN1<4:3> sets the clock source.

### Programming the MAX2991 for Different Sampling Rates

For clock rates other than 19.2MHz, update the DPTUN1 and DPTUN2 registers accordingly.

Table 3 summarizes the calculation for the default clock rate and another one.

The ADC sampling rate is the clock rate divided by 16. The sampling rate is adjustable from 200ksps to 1.2ksps in 200ksps steps.

### Interfacing to the MAX2990 Baseband

The interface to the MAX2991 AFE device uses a bidirectional bus to transfer the digital data from the ADC and to the DAC. Handshaking lines help accomplish the data transfer as well as operation of the AFE. Figure 8 shows the interface between the MAX2991 and the MAX2990.

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### Indirect Write and Read Configuration Mode

The MAX2990's single write configuration mode allows sending an arbitrary 16-bit SPI frame to the MAX2991's AFE interface. This mode allows configuring the internal registers without using the host SPI.

The SPI frame has 4 command bits labeled C3, C2, C1, and C0. These bits are normally set to 0 when transferring data frames to the DAC. The MAX2991 also responds to other command codes, shown in Table 4,

to allow reading and writing from/to its host SPI register space.

The MAX2990 does not support the read configuration mode of operation, as it cannot set the R/$\overline{W}$ bit to the required state. All configuration mode accesses are treated as writes. Set RDCONFMDEN in the RXCONF register to logic-high to enable the read configuration mode. Ensure RXCLK is active during read configuration mode read accesses. The AFE Rx interface must be inactive during read configuration mode transfers.

## Table 4. Configuration Bits

| COMMAND BITS | | | | DESCRIPTION |
|---|---|---|---|---|
| C3 | C2 | C1 | C0 | |
| 0 | 0 | 0 | 0 | Normal TXDATA packet (C2, C1, and C0 can be used to set the predriver gain dynamically). |
| 1 | 0 | 0 | 0 | Set the Indirect Address register and R/$\overline{W}$ bit. |
| 1 | 0 | 1 | 0 | Read most significant 8 bits when R/$\overline{W}$ = 1.<br>Trigger the indirect register read when R/$\overline{W}$ = 1.<br>Write most significant 8 bits to Indirect Data register when R/$\overline{W}$ = 0. |
| 1 | 0 | 0 | 1 | Read least significant 8 bits when R/$\overline{W}$ = 1.<br>Trigger the indirect register read when R/$\overline{W}$ = 1.<br>Write least significant 8 bits to Indirect Data register and trigger register write when R/$\overline{W}$ = 0.<br>Post increment the Indirect Address in both cases. |
| 1 | 0 | 1 | 1 | Reserved |
| 1 | 1 | X | X | Reserved |
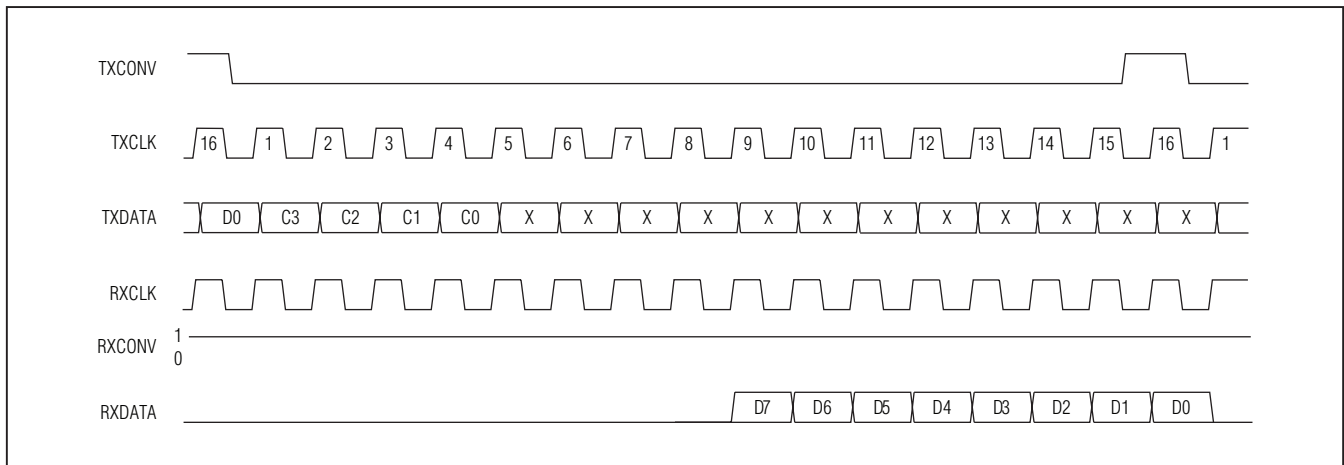


Figure 9. Communication Protocol for Indirect Read Access

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## Dynamic Predriver Gain Programming During the Data Transmission

During normal data transmission bit C3 (= 0) is used to indicate that a normal data packet is received and bits C2, C1, and C0 are used to change the predriver gain dynamically. In this case, C<2:0> maps onto predriver gain-control bits as shown in Table 5.

This mode of operation is enabled if the bit PREDRDYN in the Tx configuration register is set to 1.
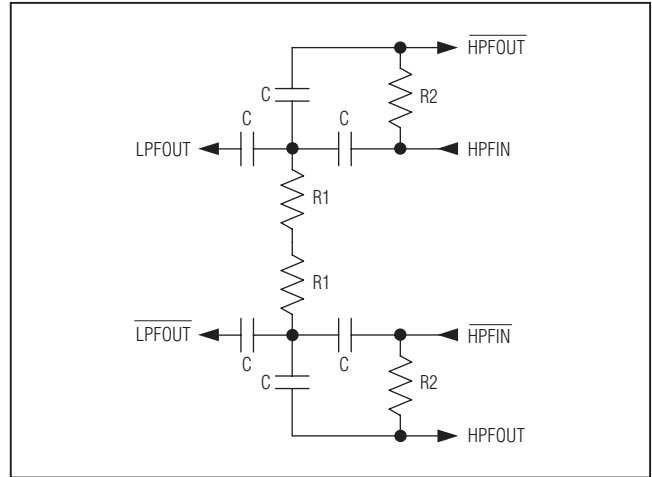
### External Highpass Filter



Figure 10. External Highpass Filter Circuitry

## Table 5. Predriver Dynamic Gain Programming

| C3 | C2 | C1 | C0 | PREDRIVER GAIN (dB) | PREDRVGAIN <3> | PREDRVGAIN <2> | PREDRVGAIN <1> | PREDRVGAIN <0> |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Unchanged | Unchanged | Unchanged | Unchanged | Unchanged |
| 0 | 0 | 0 | 1 | -8 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | -6 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | -4 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 2 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 4 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 6 | 1 | 0 | 0 | 0 |

## Table 6. External Highpass Filter Components for Different 3dB Frequencies

| 3dB CORNER (kHz) | C SELECTION (pF) | R1 (kΩ) 1% TOLERANCE | R2 (kΩ) 1% TOLERANCE |
|---|---|---|---|
| 9 | 1000 | 8.25 | 37.4 |
| 32 | 270 | 8.66 | 38.3 |
| 90 | 100 | 8.25 | 37.4 |
| 125 | 68 | 8.66 | 39.2 |
| 140 | 68 | 7.87 | 35.7 |

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## Table 7. Rx and Tx Filter Adjustment for Different 3dB Frequencies

| Rx 3dB FREQUENCY (kHz) | Tx 3dB FREQUENCY (kHz) | OFFSET | RXADJ/ TXADJ | TXADJ | PTUN2 |
|---|---|---|---|---|---|
| 130 | 125 | -15 | 79 | 79 | 0x27CF |
| 140 | 134 | 0 | 0 | 0 | 0x0000 |
| 146 | 140 | 9 | 9 | 9 | 0x0489 |
| 155 | 148 | 20 | 20 | 20 | 0x0A14 |

## Table 8. IIR Coefficients for CENELEC A Band (MAX2991 Default Mode)

| COEFFICIENT NAME | FLOATING POINT VALUE | Q13 FORMAT VALUE | REGISTER VALUE |
|---|---|---|---|
| IIR0B0 | 0.25454609117803 | 2085 | 0x0825 |
| IIR0B1 | -0.36787775183970 | -3014 | 0xF43A |
| IIR0B2 | 0.25454609117803 | 2085 | 0x0825 |
| IIR0A1 | -1.53137687683985 | -12545 | 0xCEFF |
| IIR0A2 | 0.68982207389294 | 5651 | 0x1613 |
| IIR1B0 | 0.92695273947877 | 7594 | 0x1DAA |
| IIR1B1 | -1.62702269373124 | -13329 | 0xCBEF |
| IIR1B2 | 0.92695273947877 | 7594 | 0x1DAA |
| IIR1A1 | -1.75120880788804 | -14346 | 0xC7F6 |
| IIR1A2 | 0.97809159311434 | 8013 | 0x1F4D |

### Programming Rx and Tx Filters for Different CENELEC Standards

To program the Rx and Tx filters for different CENELEC modes, program the filters in narrowband mode and adjust the cutoff frequency by providing a positive or negative offset. Typical PTUN2 register values for Rx and Tx adjustments are given in Table 7. The MAX2991 defaults to the CENELEC A mode.

### Programming the Integrated IIR Filters for Different Bands

IIR filters are used in the MAX2991 transmit path to achieve the desired attenuation at corner and out-of-band frequencies that comply with regulatory spectral mask. The filters are implemented as two cascaded second-order sections (SOS). Each filter implements a second-order transfer function:

$$H(z) = \frac{B_0 + B_1 z^{-1} + B_2 z^{-2}}{1 + A_1 z^{-1} + A_2 z^{-2}}$$

The coefficients are in Q13 format. For stable/minimum phase Butterworth IIR filter, the coefficients are between -2 and +2. Coefficients in the range of -4 to +4 are possible by using a 16-bit word.

The example in Table 8 shows the design steps used to generate the coefficients for the filter in CENELEC A band. For this design, it is desired to get a large attenuation with a sharp corner at around 95kHz. A 4th-order elliptic filter is used with the 91.9kHz passband frequency. The passband ripple is 1dB and the stopband attenuation is 12dB. For a 1.2Msps sampling frequency, the coefficients are shown in Table 8. Note that Q13 representation is found by multiplying the floating values by 8192 ($2^{13}$) and rounding the result to an integer.

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## Table 9. Purposed IIR Coefficients for FCC Band

| COEFFICIENT NAME | FLOATING POINT VALUE | Q13 FORMAT VALUE | REGISTER VALUE |
|---|---|---|---|
| IIR0B0 | 0.67910441874341 | 5563 | 0x15BB |
| IIR0B1 | 1.27553272646766 | 10449 | 0x28D1 |
| IIR0B2 | 0.67910441874341 | 5563 | 0x15BB |
| IIR0A1 | 1.24725754685134 | 10218 | 0x27EA |
| IIR0A2 | 0.54254301592170 | 4445 | 0x115D |
| IIR1B0 | 0.97169123170169 | 7960 | 0x1F18 |
| IIR1B1 | 1.62951057639590 | 13349 | 0x3425 |
| IIR1B2 | 0.97169123170169 | 7960 | 0x1F18 |
| IIR1A1 | 1.61392655185432 | 13221 | 0x33A5 |
| IIR1A2 | 0.95896648794496 | 7856 | 0x1EB0 |

The second example shows the design steps used to generate the IIR coefficients for the filter in the FCC band. For this design, a 4th-order elliptic filter is used with the 483kHz passband frequency. The passband ripple is 0.5dB and the stopband attenuation is 12dB. For a 1.2MHz sampling frequency, the coefficients are shown in Table 9.

The transmitter lowpass filter band is set by TXCONF<7:6> bits. The aforementioned floating point coefficients were generated using MATLAB® "*fdatool*" GUI.

## Chip Information

PROCESS: CMOS

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 48 LQFP | C48+2 | **21-0054** |

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