Quad Exclusive OR Gate

ELECTRICALLY TESTED PER:
5962-8755801

The 10H513 is a Quad Exclusive OR Gate with an enable common to all gates. The outputs may be wire-ORed together to perform a 4-bit comparison function (A = B). The enable is active LOW.

- 250 mW Max/Pkg (No Load)
- t_{pd} = 2.5 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	GND
A_{IN}	5	9	7	OPEN
B_{IN}	6	10	8	GND
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$\overline{Enable}$	9	13	12	OPEN
C_{IN}	10	14	13	GND
C_{IN}	11	15	14	OPEN
D_{IN}	12	16	15	GND
D_{IN}	13	1	17	OPEN
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Truth Table

Input		$\overline{E}$	Output
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
Ø	Ø	H	L

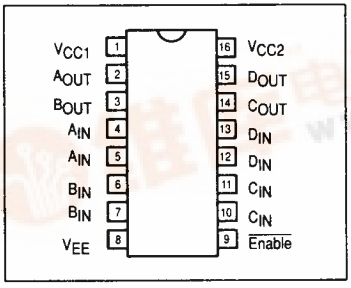
Ø = Don't Care

AVAILABLE AS

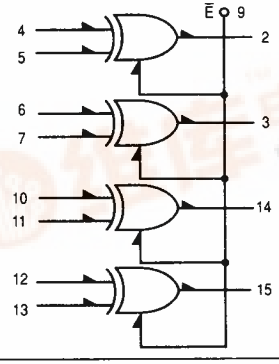
1) JAN: N/A
2) SMD: 5962-8755801
3) 883: 10H513/BXAJC
X = CASE OUTLINE AS FOLLOWS:

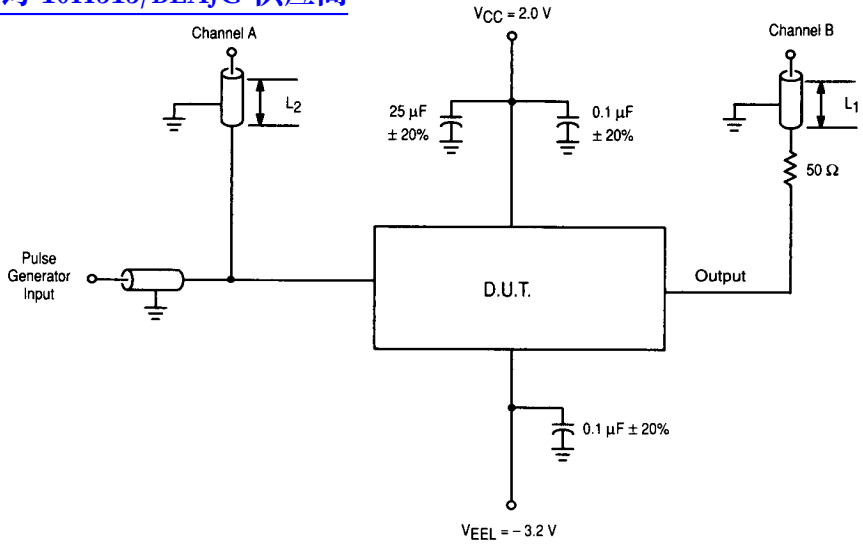
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



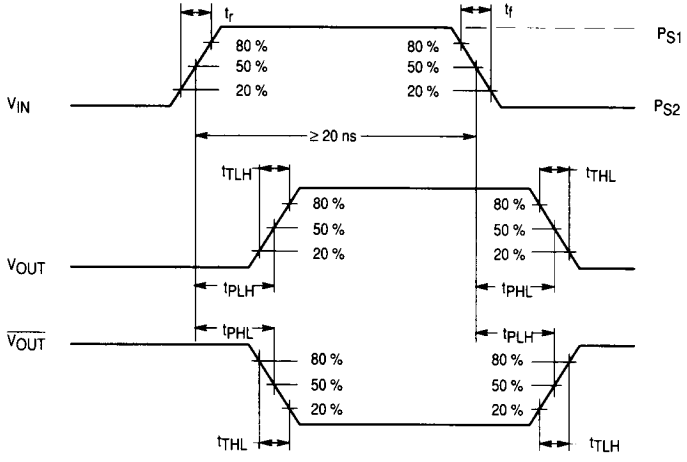
LOGIC DIAGRAM





NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. 2:1 divider may be used.
5. $L_1 = L_2$: Matched for equal time delays.



NOTES

1. $P_{IN} \geq 20$ ns.
2. $f_{IN} = 1.0$ MHz.
3. $t_r = t_f = 1.0$ ns ± 0.1 ns

Figure 1. Switching Test Circuit and Waveforms

10H513
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{IL2}	V_{IH2}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	0	-5.46	-4.94
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	0	-5.46	-4.94
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	0	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	4 - 7 11, 13				8		1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V					8		1, 16	2, 3, 14, 15
V_{OHA}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	4 - 7 10 - 13		4 - 7 10 - 13	4 - 7 10 - 13		8	1, 16	2, 3, 14, 15
V_{OLA}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	4 - 7 10 - 13		4 - 7 10 - 13	4 - 7 10 - 13		8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	-42		-46		-46		mA					8		1, 16	8
I_{IH1}	Input Current High		320		510		510	µA	4, 6 10, 12				8		1, 16	4, 6, 10, 12
I_{H2}	Input Current High		270		430		430	µA	5, 7 11, 13				8		1, 16	5, 7, 11, 3
I_{H3}	Input Current High		740		1100		1100	µA	9				8		1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7 9 - 11 13, 14			8		1, 16	4 - 7, 9 - 13

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Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{IL2}	V_{IH2}	V_{CC1}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	+2.0	-2.94
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	+2.0	-2.94
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	+2.0	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+25° C		+125° C		-55° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P.U.T.
t_{TLH}	Rise Time	0.6	1.9	0.6	2.0	0.5	1.8	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15
t_{THL}	Fall Time	0.6	1.9	0.6	2.0	0.5	1.8	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15
t_{PLH} Data	Propagation Delay Low to High (A or B to Out)	0.4	1.8	0.5	1.9	0.4	1.7	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15
t_{PHL} Data	Propagation Delay High to Low (A or B to Out)	0.4	1.8	0.5	1.9	0.4	1.7	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15
t_{PLH} Enable	Propagation Delay Low to High (Enable to Out)	0.5	2.4	0.6	2.5	0.5	2.3	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15
t_{PHL} Enable	Propagation Delay High to Low (Enable to Out)	0.5	2.4	0.6	2.5	0.5	2.3	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15