



## AD7711A\*

### FEATURES

- Charge Balancing ADC
- 24 Bits No Missing Codes
- ±0.0015% Nonlinearity
- Two-Channel Programmable Gain Front End
- Gains from 1 to 128
- Differential Inputs
- Low-Pass Filter with Programmable Filter Cutoffs
- Ability to Read/Write Calibration Coefficients
- Bidirectional Microcontroller Serial Interface
- Internal/External Reference Option
- Single or Dual Supply Operation
- Low Power (25 mW typ) with Power-Down Mode (7 mW typ)

### APPLICATIONS

RTD Transducers

### GENERAL DESCRIPTION

The AD7711A is a complete analog front end for low frequency measurement applications. The device accepts low level signals directly from a transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The part features two differential analog inputs and a differential reference input. Normally, one of the channels will be used as the main channel with the second channel used as an auxiliary input to periodically measure a second voltage. It can be operated from a single supply (by tying the  $V_{SS}$  pin to AGND) provided that the input signals on the analog inputs are more positive than  $-30$  mV. By taking the  $V_{SS}$  pin negative, the part can convert signals down to  $-V_{REF}$  on its inputs. The part also provides a  $400 \mu\text{A}$  current source that can be used to provide excitation for RTD transducers. The AD7711A thus performs all signal conditioning and conversion for a single or dual channel system.

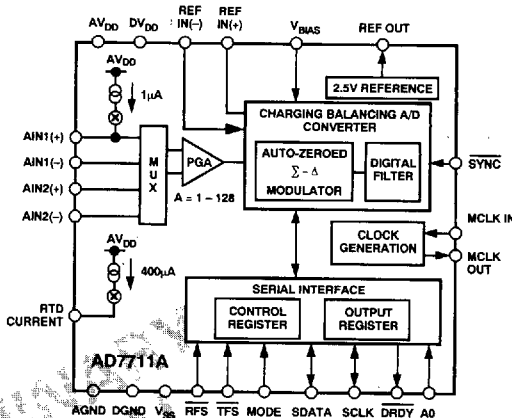
The AD7711A is ideal for use in smart, microcontroller based systems. Input channel selection, gain settings and signal polarity can be configured in software using the bidirectional serial port. The AD7711A contains self-calibration, system calibration and background calibration options and also allows the user to read and write the on-chip calibration registers.

\*Protected by U.S. Patent No. 5,134,401.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

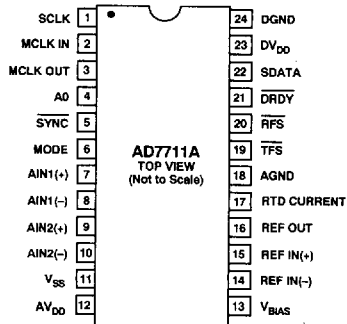
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### FUNCTIONAL BLOCK DIAGRAM



CMOS construction ensures low power dissipation and a software programmable power down mode reduces the standby power consumption to only 7 mW typical. The part is available in a 24-pin, 0.3 inch-wide, plastic and hermetic dual-in-line package (DIP) as well as a 24-lead small outline (SOIC) package.

### PIN CONFIGURATION DIP and SOIC



( $AV_{DD} = +5V \pm 5\%$ ;  $DV_{DD} = +5V \pm 5\%$ ;  $V_{SS} = 0V$  or  $-5V \pm 5\%$ ;  
 $REF\ IN(+)$  =  $+2.5V$ ;  $REF\ IN(-)$  =  $AGND$ ;  $MCLK\ IN = 10\ MHz$  unless  
 otherwise stated. All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

# AD7711A—SPECIFICATIONS

Parameter	Units	Conditions/Comments
<b>STATIC PERFORMANCE</b>		
No Missing Codes	24 22 18 15 12	Bits min Bits min Bits min Bits min Bits min
Output Noise	Tables I & II	Guaranteed by Design. For Filter Notches $\leq 60\ Hz$ For Filter Notch = $100\ Hz$ For Filter Notch = $250\ Hz$ For Filter Notch = $500\ Hz$ For Filter Notch = $1\ kHz$ Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity @ $25^{\circ}C$ $T_{MIN}$ to $T_{MAX}$	$\pm 0.0045$ $\pm 0.0075$	% of FSR max % of FSR max
Positive Full-Scale Error <sup>2, 3</sup> Full-Scale Drift <sup>5</sup>	See Note 4 3/GAIN 0.35	$\mu V/^{\circ}C$ typ $\mu V/^{\circ}C$ typ
Unipolar Offset Error <sup>2</sup> Unipolar Offset Drift <sup>5</sup>	See Note 4 2.5/GAIN 0.3	$\mu V/^{\circ}C$ typ $\mu V/^{\circ}C$ typ
Bipolar Zero Error <sup>2</sup> Bipolar Zero Drift <sup>5</sup>	See Note 4 2.5/GAIN 0.3	$\mu V/^{\circ}C$ typ $\mu V/^{\circ}C$ typ
Bipolar Negative Full-Scale Error <sup>2</sup> Bipolar Negative Full-Scale Drift <sup>5</sup>	$\pm 0.006$ 4/GAIN 0.5	% of FSR max $\mu V/^{\circ}C$ typ $\mu V/^{\circ}C$ typ
<b>ANALOG INPUTS/REFERENCE INPUTS</b>		
Common-Mode Rejection (CMR) $V_{SS}$ to $AV_{DD}$	92	dB min V min to V max
Common-Mode Voltage Range <sup>6</sup>	100	dB min
Normal Mode 50 Hz Rejection <sup>7</sup>	100	dB min
Normal Mode 60 Hz Rejection <sup>7</sup>	150	dB min
Common-Mode 50 Hz Rejection <sup>7</sup>	150	dB min
Common-Mode 60 Hz Rejection <sup>7</sup>	150	dB min
DC Input Leakage Current <sup>7</sup> @ $+25^{\circ}C$ $T_{MIN}$ to $T_{MAX}$	10 1	pA max nA max
Sampling Capacitance <sup>7</sup> Analog Inputs <sup>8</sup>	20	pF max
Input Voltage Range <sup>9</sup>	0 to $+V_{REF}^{10}$ $\pm V_{REF}$ See Table III	nom nom
Input Sampling Rate, $f_s$ Reference Inputs REF IN(+) - REF IN(-) Voltage <sup>11</sup>	$+2.5$ to $+5$	V min to V max
Input Sampling Rate, $f_s$	$f_{CLK\ IN}/512$	
<b>REFERENCE OUTPUT</b>		
Output Voltage	2.5	V nom
Initial Tolerance	$\pm 4$	% max
Drift	20	ppm/ $^{\circ}C$ typ
Output Noise	50	$\mu V$ typ
Line Regulation ( $AV_{DD}$ )	1	mV/V max
Load Regulation	1.5	mV/mA max
External Current	1	mA max

## NOTES

- Temperature ranges are as follows: A Version,  $-40^{\circ}C$  to  $+85^{\circ}C$ ; S Version  $-55^{\circ}C$  to  $+125^{\circ}C$ . See also Note 16.
- Applies after calibration at the temperature of interest.
- Positive full-scale error applies to both unipolar and bipolar input ranges.
- These errors will be of the order of the output noise of the part as shown in Table I.
- Recalibration at any temperature or use of the background calibration mode will remove these drift errors.
- This common-mode voltage range is allowed provided that the input voltage on AIN1(+) and AIN2(-) does not exceed  $AV_{DD} + 30\ mV$  and  $V_{SS} - 30\ mV$ .
- These numbers are guaranteed by design and/or characterization.
- The analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance depends on the selected gain (see Tables IV and V).
- The analog input voltage range on the AIN1(+) and AIN2(+) inputs is given here with respect to the voltage on the AIN1(-) and AIN2(-) inputs. The absolute voltage on the analog inputs should not go more positive than  $AV_{DD} + 30\ mV$  or go more negative than  $V_{SS} - 30\ mV$ .
- $V_{REF} = REF\ IN(+)$  -  $REF\ IN(-)$ .
- The reference input voltage range may be restricted by the input voltage range requirement on the  $V_{BIAS}$  input.

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Parameter	A, S Versions <sup>1</sup>	Units	Conditions/Comments
$V_{BIAS}$ INPUT <sup>12</sup> Input Voltage Range	$AV_{DD} - 0.85 \times V_{REF}$ or $AV_{DD} - 3$  or $AV_{DD} - 2.1$ $V_{SS} + 0.85 \times V_{REF}$ or $V_{SS} + 3$  or $V_{SS} + 2.1$ 65 to 85	V max  V max  V min  V min dB typ	See $V_{BIAS}$ Input Section Whichever Is Smaller; +5 V/-5 V or +10 V/0 V Nominal $AV_{DD}/V_{SS}$ Whichever Is Smaller; +5 V/0 V Nominal $AV_{DD}/V_{SS}$ See $V_{BIAS}$ Input Section Whichever Is Greater; +5 V/-5 V or +10 V/0 V Nominal $AV_{DD}/V_{SS}$ Whichever Is Greater; +5 V/0 V Nominal $AV_{DD}/V_{SS}$ Increasing with Gain
$V_{BIAS}$ Rejection			
LOGIC INPUTS			
Input Current All Inputs Except MCLK IN	$\pm 10$	$\mu A$ max	
$V_{INL}$ , Input Low Voltage	0.8	V max	
$V_{INH}$ , Input High Voltage	2.0	V min	
MCLK IN Only			
$V_{INL}$ , Input Low Voltage	0.8	V max	
$V_{INH}$ , Input High Voltage	3.5	V min	
LOGIC OUTPUTS			
$V_{OL}$ , Output Low Voltage	0.4	V max	$I_{SINK} = 1.6$ mA
$V_{OH}$ , Output High Voltage	$DV_{DD} - 1$	V min	$I_{SOURCE} = 100$ $\mu A$
Floating State Leakage Current	$\pm 10$	$\mu A$ max	
Floating State Output Capacitance <sup>13</sup>	9	pF typ	
TRANSDUCER BURN-OUT			
Current	100	nA nom	
Initial Tolerance	$\pm 10$	% typ	
Drift	0.1	%/°C typ	
RTD EXCITATION CURRENT			
Output Current	400	$\mu A$ nom	
Initial Tolerance	$\pm 20$	$\mu A$ max	
Drift	20	ppm/°C typ	
Line Regulation ( $AV_{DD}$ )	400	nA/V max	$AV_{DD} = +5$ V
Load Regulation	400	nA/V max	
Output Compliance	$AV_{DD} - 2$	V max	
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit <sup>14</sup>	$(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit <sup>14</sup>	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit <sup>15</sup>	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span <sup>15</sup>	$0.8 \times V_{REF}/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(2.1 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)

## NOTES

<sup>12</sup>The AD7711A is tested with the following  $V_{BIAS}$  voltages. With  $AV_{DD} = +5$  V and  $V_{SS} = 0$  V,  $V_{BIAS} = +2.5$  V; with  $AV_{DD} = +10$  V and  $V_{SS} = 0$  V,  $V_{BIAS} = +5$  V and with  $AV_{DD} = +5$  V and  $V_{SS} = -5$  V,  $V_{BIAS} = 0$  V.

<sup>13</sup>Sample tested at +25°C to ensure compliance.

<sup>14</sup>After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale then the device will output all 0s.

<sup>15</sup>These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed  $AV_{DD} + 30$  mV or go more negative than  $V_{SS} - 30$  mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

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# AD7711A—SPECIFICATIONS

Parameter	A, S Versions <sup>1</sup>	Units	Conditions/Comments
<b>POWER REQUIREMENTS</b>			
Power Supply Voltages			
AV <sub>DD</sub> Voltage <sup>16</sup>	+5 to +10	V nom	±5% for Specified Performance
DV <sub>DD</sub> Voltage <sup>17</sup>	+5	V nom	±5% for Specified Performance
AV <sub>DD</sub> -V <sub>SS</sub> Voltage	+10.5	V max	For Specified Performance
Power Supply Currents			
AV <sub>DD</sub> Current	4	mA max	
DV <sub>DD</sub> Current	4.5	mA max	
V <sub>SS</sub> Current	1.5	mA max	V <sub>SS</sub> = -5 V
Power Supply Rejection <sup>18</sup>			Rejection w.r.t. AGND; Assumes V <sub>BIAS</sub> Is Fixed
Positive Supply (AV <sub>DD</sub> )	See Note 19	dB typ	
Negative Supply (V <sub>SS</sub> )	90	dB typ	
Power Dissipation			
Normal Mode	45	mW max	AV <sub>DD</sub> = DV <sub>DD</sub> = +5 V, V <sub>SS</sub> = 0 V; Typically 25 mW
Normal Mode	52.5	mW max	AV <sub>DD</sub> = DV <sub>DD</sub> = +5 V, V <sub>SS</sub> = -5 V; Typically 30 mW
Standby (Power-Down) Mode	15	mW max	AV <sub>DD</sub> = DV <sub>DD</sub> = +5 V, V <sub>SS</sub> = 0 V or -5 V; Typically 7 mW

## NOTES

<sup>16</sup>The AD7711A is specified with a 10 MHz clock for AV<sub>DD</sub> voltages of +5 V ±5%. It is specified with an 8 MHz clock for AV<sub>DD</sub> voltages greater than 5.25 V and less than 10.5 V. Operation with AV<sub>DD</sub> voltages in the range 5.25 V to 10.5 V is only guaranteed over the 0 to +70°C temperature range.

<sup>17</sup>The ±5% tolerance on the DV<sub>DD</sub> input is allowed provided that DV<sub>DD</sub> does not exceed AV<sub>DD</sub> by more than 0.3 V.

<sup>18</sup>Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 10 Hz, 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 10 Hz, 30 Hz or 60 Hz.

<sup>19</sup>PSRR depends on gain: Gain of 1: 70 dB typ; Gain of 2: 75 dB typ; Gain of 4: 80 dB typ; Gains of 8 to 128: 85 dB typ. These numbers can be improved (to 95 dB typ) by deriving the V<sub>BIAS</sub> voltage (via Zener diode or reference) from the AV<sub>DD</sub> supply.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS\*

(T<sub>A</sub> = +25°C, unless otherwise noted)

AV <sub>DD</sub> to DV <sub>DD</sub>	-0.3 V to +12 V
AV <sub>DD</sub> to V <sub>SS</sub>	-0.3 V to +12 V
AV <sub>DD</sub> to AGND	-0.3 V to +12 V
AV <sub>DD</sub> to DGND	-0.3 V to +12 V
DV <sub>DD</sub> to AGND	-0.3 V to +6 V
DV <sub>DD</sub> to DGND	-0.3 V to +6 V
V <sub>SS</sub> to AGND	+0.3 V to -6 V
V <sub>SS</sub> to DGND	+0.3 V to -6 V
Analog Input Voltage to AGND	..... V <sub>SS</sub> - 0.3 V to AV <sub>DD</sub> + 0.3 V
Reference Input Voltage to AGND	..... V <sub>SS</sub> - 0.3 V to AV <sub>DD</sub> + 0.3 V
REF OUT to AGND	..... -0.3 V to AV <sub>DD</sub>

## CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

Digital Input Voltage to DGND	..... -0.3 V to AV <sub>DD</sub> + 0.3 V
Digital Output Voltage to DGND	..... -0.3 V to DV <sub>DD</sub> + 0.3 V
Operating Temperature Range	
Commercial (A Version)	..... -40°C to +85°C
Extended (S Version)	..... -55°C to +125°C
Storage Temperature Range	..... -65°C to +150°C
Lead Temperature (Soldering, 10 secs)	..... +300°C
Power Dissipation (Any Package) to +75°C	..... 450 mW
Derates Above +75°C	..... 6 mW/°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Option <sup>2</sup>
AD7711AAN	-40°C to +85°C	N-24
AD7711AAR	-40°C to +85°C	R-24

## NOTES

<sup>1</sup>To order MIL-STD-883B, Class B processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.

<sup>2</sup>N = Plastic DIP; R = SOIC. For outline information see Package Information section.

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## CONTROL REGISTER (24 BITS)

A write to the device with the A0 input low writes data to the control register. A read to the device with the A0 input low accesses the contents of the control register. The control register is 24-bits wide and when writing to the register 24 bits of data must be written otherwise the data will not be loaded to the control register. In other words, it is not possible to write just the first 12-bits of data into the control register. If more than 24 clock pulses are provided before  $\overline{\text{TFS}}$  returns high, then all clock pulses after the 24th clock pulse are ignored. Similarly, a read operation from the control register should access 24 bits of data.

MSB

MD2	MD1	MD0	G2	G1	G0	CH	PD	WL	IO	BO	B/U
-----	-----	-----	----	----	----	----	----	----	----	----	-----

FS11*	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
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LSB

\*Must always be 0 to ensure correct operation of the device.

Operating Mode			Operating Mode
MD2	MD1	MD0	
0	0	0	Normal Mode. This is the normal mode of operation of the device whereby a read to the device with A0 high accesses data from the data register. This is the default condition of these bits after the internal power on reset.
0	0	1	Activate Self-Calibration. This activates self-calibration on the channel selected by CH. This is a one-step calibration sequence, and when complete, the part returns to normal mode (with MD2, MD1, MD0 of the control register returning to 0, 0, 0). The $\overline{\text{DRDY}}$ output indicates when this self-calibration is complete and valid data is available in the output register. For this calibration type, the zero scale calibration is done internally on shorted (zeroed) inputs and the full-scale calibration is done internally on $V_{\text{REF}}$ .
0	1	0	Activate System Calibration. This activates system calibration on the channel selected by CH. This is a two-step calibration sequence, with the zero scale calibration done first on the selected input channel and $\overline{\text{DRDY}}$ indicating when this zero scale calibration is complete. The part returns to normal mode at the end of this first step in the two-step sequence.
0	1	1	Activate System Calibration. This is the second step of the system calibration sequence with full-scale calibration being performed on the selected input channel. Once again, $\overline{\text{DRDY}}$ indicates when the full-scale calibration is complete. When this calibration is complete, the part returns to normal mode.
1	0	0	Activate System Offset Calibration. This activates system offset calibration on the channel selected by CH. This is a one-step calibration sequence and, when complete, the part returns to normal mode with $\overline{\text{DRDY}}$ indicating when this system offset calibration is complete. For this calibration type, the zero scale calibration is done on the selected input channel and the full-scale calibration is done internally on $V_{\text{REF}}$ .
1	0	1	Activate Background Calibration. This activates background calibration on the channel selected by CH. If the background calibration mode is on, then the AD7711A provides continuous self-calibration of the reference and shorted (zeroed) inputs. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the device when there is a change in the ambient temperature. In this mode, the shorted (zeroed) inputs and $V_{\text{REF}}$ , as well as the analog input voltage, are continuously monitored and the calibration registers of the device are automatically updated.
1	1	0	Read/Write Zero Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the zero scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the zero scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Therefore, when writing to the calibration register 24 bits of data must be written, otherwise the new data will not be transferred to the calibration register.
1	1	1	Read/Write Full-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the full-scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the full-scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Therefore, when writing to the calibration register 24 bits of data must be written, otherwise the new data will not be transferred to the calibration register.

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# AD7711A

## PGA Gain

G2	G1	G0	Gain	(Default Condition After the Internal Power-On Reset)
0	0	0	1	
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

## Channel Selection

CH	Channel	(Default Condition After the Internal Power-On Reset)
0	AIN1	
1	AIN2	

## Power-Down

PD	Power-Down	(Default Condition After the Internal Power-On Reset)
0	Normal Operation	
1	Power-Down	

## Word Length

WL	Output Word Length	(Default Condition After Internal Power-On Reset)
0	16-Bit	
1	24-Bit	

## RTD Excitation Current

IO	RTD Excitation Current	(Default Condition After Internal Power-On Reset)
0	Off	
1	On	

## Burn-Out Current

BO	Burn-Out Current	(Default Condition After Internal Power-On Reset)
0	Off	
1	On	

## Bipolar/Unipolar Selection (Both Inputs)

B/U	Bipolar/Unipolar Selection	(Default Condition After Internal Power-On Reset)
0	Bipolar	
1	Unipolar	

## Filter Selection (FS11–FS0)

The on-chip digital filter provides a  $\text{Sinc}^3$  (or  $(\text{Sinx}/x)^3$ ) filter response. The 12 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device.

The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency =  $(f_{\text{CLK IN}}/512)/\text{code}$  where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 2,000. With the nominal  $f_{\text{CLK IN}}$  of 10 MHz, this results in a first notch frequency range from 9.76 Hz to 1.028 kHz. To ensure correct operation of the AD7711A, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I and II and Figure 2 show the effect of the filter notch frequency and gain on the effective resolution of the AD7711A. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1 kHz, a new word is available every 1 ms.

The settling time of the filter to a full-scale step input change is worst case  $4 \times 1/(\text{output data rate})$ . This settling time is to 100% of the final value. For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. If the first notch is at 1 kHz, the settling time of the filter to a full-scale input step is 4 ms max. This settling time can be reduced to  $3 \times 1/(\text{output data rate})$  by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with  $\overline{\text{SYNC}}$  low, the settling time will be  $3 \times 1/(\text{output data rate})$ . If a change of channels takes place, the settling time is  $3 \times 1/(\text{output data rate})$  regardless of the SYNC input.

The  $-3$  dB frequency is determined by the programmed first notch frequency according to the relationship: filter  $-3$  dB frequency =  $0.262 \times \text{first notch frequency}$ .

All other features and functions of the AD7711A are as per the AD7710. Refer to the AD7710/AD7712 data sheet for detailed description.

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