REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated drawing to reference MIL-STD-1835. Made the following changes to table I: output low voltage, changed I_{OL} from -1.6 mA to 1.6 mA; interrupt pulse width, PW_{IRQ}, changed units from ns to t_{cyc}; conversion time, changed max limit from t_{cyc}+32000 to t_{cyc}+40000; delay time, t_{ASED}, changed min limit from 105.5 to 95.5. Modified figure 1, case outline Y. Editorial changes throughout.	92-12-04	Monica L. Poelking

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS															
REV	A	A	A	A	A	A		A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
11 October 1990

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, HIGH SPEED CMOS, 8-BIT MICROCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89527
A	67268	

SHEET 1 OF 34

DESC FORM 193
JUL 91

5962-E585-92

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89527	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	68HC811E2	8-bit microcontroller, EEPROM 2K bytes, RAM 256 bytes

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T48 or CDIP2-T48	48	Dual-in-line
Y	See figure 1	52	Square leaded chip carrier

1.3 Absolute maximum ratings.

Supply voltage range	-0.3 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.75 W
Lead temperature (soldering, 5 seconds)	+270°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction to case (Θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	4.5 V dc minimum to 5.5 V dc maximum
High level input voltage (V_{IH})	0.8 x V_{DD}
Low level input voltage range (V_{IL})	V_{SS} to 0.2 V dc x V_{DD}
Maximum high level output voltage (V_{OH})	V_{DD}-0.1 V dc
Maximum low level output voltage (V_{OL})	0.4 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Frequency of operation	DC to 2.1 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be as specified on figure 1 and in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

TABLE I. Electrical performance characteristics.

Test		Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$ $V_{SS} = 0\ V\ dc$ $-55°C \le T_C \le +125°C$	Group A subgroups	Limits		Unit
					Min	Max	
Output high voltage: All outputs except RESET, XTAL, and MODA		V_{OH}	$I_{OH} = -0.8\ mA$ $V_{DD} = 4.5\ V$ 1/	1,2,3	V_{DD} -0.8		V
Output low voltage: All outputs except XTAL		V_{OL}	$I_{OL} = 1.6\ mA$ $V_{DD} = 4.5\ V$	1,2,3		0.4	V
Input high voltage	All inputs except RESET	V_{IH}	$V_{DD} = 4.5\ V$	1,2,3	0.7 V_{DD}	V_{DD}	V
	RESET				0.8 V_{DD}	V_{DD}	
Input low voltage: All inputs		V_{IL}		1,2,3	V_{SS}	0.2 V_{DD}	V
I/O ports, three-state leakage PA3, PA7, PC0-PC7, PD0-PD5, AS/STRA, MODA/LIR, RESET		I_{OZ}	$V_{DD} = 5.5\ V$ $V_{IN} = V_{IH}$ or V_{IL}	1,2,3		±10	µA
Input current	PA0 - PA2, IRQ, XIRQ	I_{IN}	$V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 5.5\ V$	1,2,3		±1	µA
	MODB/V_{stby}		2/			±10	
RAM standby voltage powerdown		V_{SB}		1,2,3	4.0	V_{DD}	V
RAM standby current powerdown		I_{SB}		1,2,3		20	µA
Total supply current 3/	RUN:	I_{DD}	$V_{DD} = 5.5\ V$ Single chip	1,2,3		20	mA
			$V_{DD} = 5.5\ V$ Expanded multiplexed			30	
	WAIT: All peripheral functions shut down	WI_{DD}	$V_{DD} = 5.5\ V$ Single-chip	1,2,3		10	
			$V_{DD} = 5.5\ V$ Expanded multiplexed			15	
	STOP: No clocks	SI_{DD}	$V_{DD} = 5.5\ V$ Single-chip	1,2,3		300	µA
Input capacitance	PA0-PA2, PE0-PE7, EXTAL, IRQ, XIRQ	C_{IN}	$V_{IN} = 0\ V$ $f_{IN} = 1\ MHz$ See 4.3.1b	4		8	pF
	PA7, PA3, PC0-PC7, PD0-PD5, AS/STRA MODA/LIR, RESET					14	
Functional tests			$V_{DD} = 4.5\ V, 5.5\ V$	7,8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$ $V_{SS} = 0\ V\ dc$ $-55°C \le T_C \le +125°C$	Group A subgroups	1.0 MHz		2.1 MHz		Unit
				Min	Max	Min	Max	
Control timing								
Frequency of operation	f_o	V_{DD} = 4.5 V See figure 4	9,10,11	0	1.0	0	2.1	MHz
E clock period	t_{cyc}		9,10,11	1000.0		476.0		ns
Crystal frequency	f_{XTAL}		9,10,11		4.0		8.4	MHz
External oscillator frequency	f_{oEX}		9,10,11	0	4.0	0	8.4	MHz
Processor control setup	t_{PCS}		9,10,11	200.0		69.0		ns
Reset input pulse width: To guarantee external reset vector 4/	PW_{RSTL}		9,10,11	8.0		8.0		t_{cyc}
Reset input pulse width: Minimum input time may be preempted by internal reset	PW_{RSTL}		9,10,11	1.0		1.0		t_{cyc}
Mode programming setup time	t_{MPS}		9,10,11	2.0		2.0		t_{cyc}
Mode programming hold time	t_{MPH}		9,10,11	0.0		0.0		ns
Interrupt pulse width IRQ edge sensitive mode	PW_{IRQ}		9,10,11	2.0		2.0		t_{cyc}
Wait recovery startup time	t_{WRS}		9,10,11		4.0		4.0	t_{cyc}
Timer pulse width input capture, pulse accumulator input	PW_{TIM}		9,10,11	1020.0		496.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$ $V_{SS} = 0\ V\ dc$ $-55°C \le T_C \le +125°C$	Group A subgroups	1.0 MHz		2.1 MHz		Unit
				Min	Max	Min	Max	
Peripheral port timing 5/								
Frequency of operation (E clock frequency)	f_o	V_{DD} = 4.5 V See figure 4	9,10,11	1.0	1.0	2.1	2.1	MHz
E clock period	t_{cyc}		9,10,11	1000.0		476.0		ns
Peripheral data setup time MCU read of ports A, C, D, and E	t_{PDSU}		9,10,11	100.0		100.0		ns
Peripheral data hold time MCU read of ports A, C, D, and E	t_{PDH}		9,10,11	50.0		50.0		ns
Delay time, peripheral data write: MCU write to port A	t_{PWD}		9,10,11		175		175	ns
Delay time, peripheral data write: MCU write to port B, C, and D	t_{PWD}		9,10,11		340.0		209.0	ns
Input data setup time (port C)	t_{IS}		9,10,11	60.0		60.0		ns
Input data hold time (port C)	t_{IH}		9,10,11	100.0		100.0		ns
Delay time, E fall to STRB	t_{DEB}		9,10,11		350.0		219.0	ns
Setup time, STRA asserted to E fall 6/	t_{AES}		9,10,11	0.0		0.0		ns
Delay time, STRA asserted to port C, data output valid	t_{PCD}		9,10,11		100.0		100.0	ns
Hold time, STRA negated to port C data	t_{PCH}		9,10,11	10.0		10.0		ns
Three-state hold time	t_{PCZ}		9,10,11		150.0		150.0	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$ $V_{SS} = 0\ V\ dc$ $-55°C \le T_C \le 125°C$ $750\ kHz \le E \le 2.1\ MHz$	Group A subgroups	Limits		Unit
				Min	Max	
A/D converter						
Resolution	RES	Number of bits resolved by the A/D	4,5,6	8		Bits
Non-linearity	NLI	Maximum deviation from the ideal and A/D transfer characteristics	4,5,6		±1/2	LSB
Zero error	ZER	Difference between the output of an ideal and an actual A/D for zero input voltage	4,5,6		±1/2	LSB
Full-scale error	FSE	Difference between the output of an ideal and an actual A/D for full-scale input voltage	4,5,6		±1/2	LSB
Total unadjusted error	TUE	Maximum sum of non-linearity, zero error, and full-scale error	4,5,6		±1/2	LSB
Quantization error	QTE	Uncertainty due to converter resolution	4,5,6		±1/2	LSB
Absolute accuracy	AAC	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	4,5,6		±1	LSB
Conversion range	COR	Analog input voltage range	4,5,6	V_{RL}	V_{RH}	V
Maximum analog reference voltage	V_{RH}	7/	4,5,6	V_{RL}	$V_{DD}+0.1$	V
Minimum analog reference voltage	V_{RL}	7/	4,5,6	$V_{SS}-0.1$	V_{RH}	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test		Symbol	Conditions 4.5 V ≤ V_{DD} ≤ 5.5 V V_{SS} = 0 V dc -55°C ≤ T_C ≤ +125°C 750 kHz ≤ E ≤ 2.1 MHz		Group A subgroups	Limits		Unit
						Min	Max	
Minimum difference between V_{RH} and V_{RL}		ΔV_R	7/		4,5,6	3		V
Conversion time	E clock	CONT	Total time to perform a single analog-to-digital conversion		4,5,6		32 8/	t_{cyc}
	Internal RC oscillator 8/						t_{cyc} +40000	ns
Monotonicity		MON	Conversion result never decreases with an increase in input voltage and has no missing codes 9/		4,5,6			
Zero input reading		ZIR	Conversion result when V_{IN} = V_{RL}		4,5,6	00		Hex
Full scale reading		FSR	Conversion result when V_{IN} = V_{RH}		4,5,6		FF	Hex
Sample acquisition time		SAT	Analog input acquisition sampling time	E clock 10/	4,5,6	12		t_{cyc}
				Internal RC oscillator 11/			12	µs
Input leakage		I_{IN}	Input leakage on A/D pins	PE0-PE7	9,10,11		400	nA
				V_{RL}, V_{RH}			1.0	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$ $V_{SS} = 0\ V\ dc$ $-55°C \le T_C \le +125°C$	Group A subgroups	1.0 MHz		2.1 MHz		Unit
				Min	Max	Min	Max	
Expansion bus timing								
Frequency of operation (E clock frequency)	f_o	V_{DD} = 4.5 V See figure 4	9,10,11	1.0	1.0	2.1	2.1	MHz
Cycle time	t_{cyc}		9,10,11	1000.0		476.0		ns
Pulse width, E low	PW_{EL}		9,10,11	477.0		215.0		ns
Pulse width, E high	PW_{EH}		9,10,11	472.0		210.0		ns
E and AS rise time	t_r		9,10,11		20.0		20.0	ns
E and AS fall time	t_f		9,10,11		20.0		20.0	ns
Address hold time	t_{AH}		9,10,11	95.5		30.0		ns
Non-muxed address valid time to E rise 8/	t_{AV}		9,10,11	281.5		85.0		ns
Read data setup time	t_{DSR}		9,10,11	30.0		30.0		ns
Read data hold time	t_{DHR}		9,10,11	10.0	145.5	10.0	80.0	ns
Write data delay time 8a/	t_{DDW}		9,10,11		190.5		125.0	ns
Write data hold time 8a/	t_{DHW}		9,10,11	95.5		30.0		ns
Muxed address valid time to E rise 8b/	t_{AVM}		9,10,11	271.5		75.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$ $V_{SS} = 0\ V\ dc$ $-55°C \le T_C \le +125°C$	Group A subgroups	1.0 MHz		2.1 MHz		Unit
				Min	Max	Min	Max	
Muxed address valid time to AS fall	t_{ASL}	V_{DD} = 4.5 V See figure 4	9,10,11	151.0		20.0		ns
Muxed address hold time 8b/	t_{AHL}		9,10,11	95.5		30.0		ns
Delay time, E to AS rise 8b/	t_{ASD}		9,10,11	115.5		50.0		ns
Pulse width, AS high	PW_{ASH}		9,10,11	221.0		90.0		ns
Delay time, AS to E rise 8b/	t_{ASED}		9,10,11	95.5		40.0		ns
MPU address access time 8b/	t_{ACCA}		9,10,11	733.5		275.0		ns
MPU access time	t_{ACCE}		9,10,11		442.0		180.0	ns
Muxed address delay (previous cycle MPU read) 8a/	t_{MAD}		9,10,11	145.5		80.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test		Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$ $V_{SS} = 0\ V\ dc$ $-55°C \le T_C \le +125°C$	Group A subgroups	Limits		Unit
					Min	Max	
Serial peripheral interface (SPI) timing							
Operating frequency	Master slave	$f_{op(m)}$ $f_{op(s)}$	V_{DD} = 4.5 V See figure 4	9,10,11 9,10,11	0 0	0.5 2.1	MHz
Cycle time	Master	$t_{cyc(m)}$		9,10,11	2.0		t_{cyc}
	slave	$t_{cyc(s)}$		9,10,11	480		ns
Enable lead time	Master slave	$t_{lead(m)}$ $t_{lead(s)}$		9,10,11 9,10,11	12/ 240		ns
Enable lag time	Master slave	$t_{lag(m)}$ $t_{lag(s)}$		9,10,11 9,10,11	12/ 240		ns
Clock (SCK) high time	Master slave	$t_{w(SCKH)m}$ $t_{w(SCKH)s}$		9,10,11 9,10,11	340 190		ns
Clock (SCK) low time	Master slave	$t_{w(SCKL)m}$ $t_{w(SCKL)s}$		9,10,11 9,10,11	340 190		ns
Data setup time	Master slave	$t_{su(m)}$ $t_{su(s)}$		9,10,11 9,10,11	100 100		ns
Data hold time	Master slave	$t_{h(m)}$ $t_{h(s)}$		9,10,11 9,10,11	100 100		ns
Access time (time to data active from high impedance state) slave		t_a		9,10,11	0	120	ns
Disable time (hold time to high-impedance state) slave		t_{dis}		9,10,11		240	ns
Data valid (after enable edge) 13/		$t_{v(s)}$		9,10,11		240	ns
Data hold time (outputs, after enable edge)		t_{ho}		9,10,11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test		Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$ $V_{SS} = 0\ V\ dc$ $-55°C \le T_C \le +125°C$		Group A subgroups	Limits		Unit
						Min	Max	
Rise time 9/	SCK, MOSI, and MISO	t_{rm}	V_{DD} = 4.5 V See figure 4	20% V_{DD} to 70% V_{DD} C_L = 200 pF	9,10,11		100	ns
	SCK, MOSI, MISO, and $\overline{SS}$	t_{rs}			9,10,11		2.0	µs
Fall time 9/	SCK, MOSI, and MISO	t_{fm}		70% V_{DD} to 20% V_{DD} C_L = 200 pF	9,10,11		100	ns
	SCK, MOSI, MISO, and $\overline{SS}$	t_{fs}			9,10,11		2.0	µs
Programming time	14/ 2.1 MHz		V_{DD} = 4.5 V Not shown		9,10,11	25		ms
	RC oscillator 15/ enabled					25		
Erase time	Byte, row, and bulk				9,10,11	25		ms
Write/erase endurance						5,000		cycles
Data retention 16/						10		years

1/ V_{OH} specification for $\overline{RESET}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wire-OR mode.
2/ See A/D specification for leakage current for port E.
3/ All ports configured as inputs, $V_{IL} \le 0.2$ V, $V_{IH} \ge V_{DD} - 0.2$ V, no dc loads, EXTAL driven with a square wave, and t_{cyc} = 476.5 ns.
4/ RESET will be recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt.
5/ Ports C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).
6/ If this setup time is met, STRB will acknowledge in the next cycle. If it is not met, the response may be delayed one more cycle.
7/ Performance verified down to 2.5 V ΔV_R, but accuracy is tested and guaranteed at ΔV_R = 5 V ± 10 percent. Source impedances greater than 10 kΩ will adversely affect accuracy, due mainly to input leakage.
8/ Input clocks with duty cycles other than 50 percent will affect bus performance. Timing parameters affected by input clock duty cycle are identified by "a" and "b". To recalculate the approximate bus timing values, substitute the following expressions in place of 1/8 t_{cyc} in the above formulas where applicable:
   a. $(1-dc) \times (1/4 \times t_{cyc})$
   b. $DC \times (1/4 \times t_{cyc})$
   Where dc is the decimal value of duty cycle percentage (high time).
9/ Subgroups 4, 5, and 6 shall be guaranteed for all bits.
10/ Absolute (shall be exact value).
11/ Conversions using internal RC oscillator not tested at -55°C.
12/ Signal production depends on software.
13/ Assumes 200 pF load on all SPI pins.
14/ Programming time tested at 2.1 MHz with internal RC oscillator disabled for all three temperatures.
15/ Programming time with internal RC oscillator enabled is tested at 500 kHz. Recommend that internal RC oscillator be used when frequency falls below 1.0 MHz or when temperature exceeds 85°C and frequency falls below 2.0 MHz.
16/ The 10 years specified is based on an average operating temperature of 70°C.

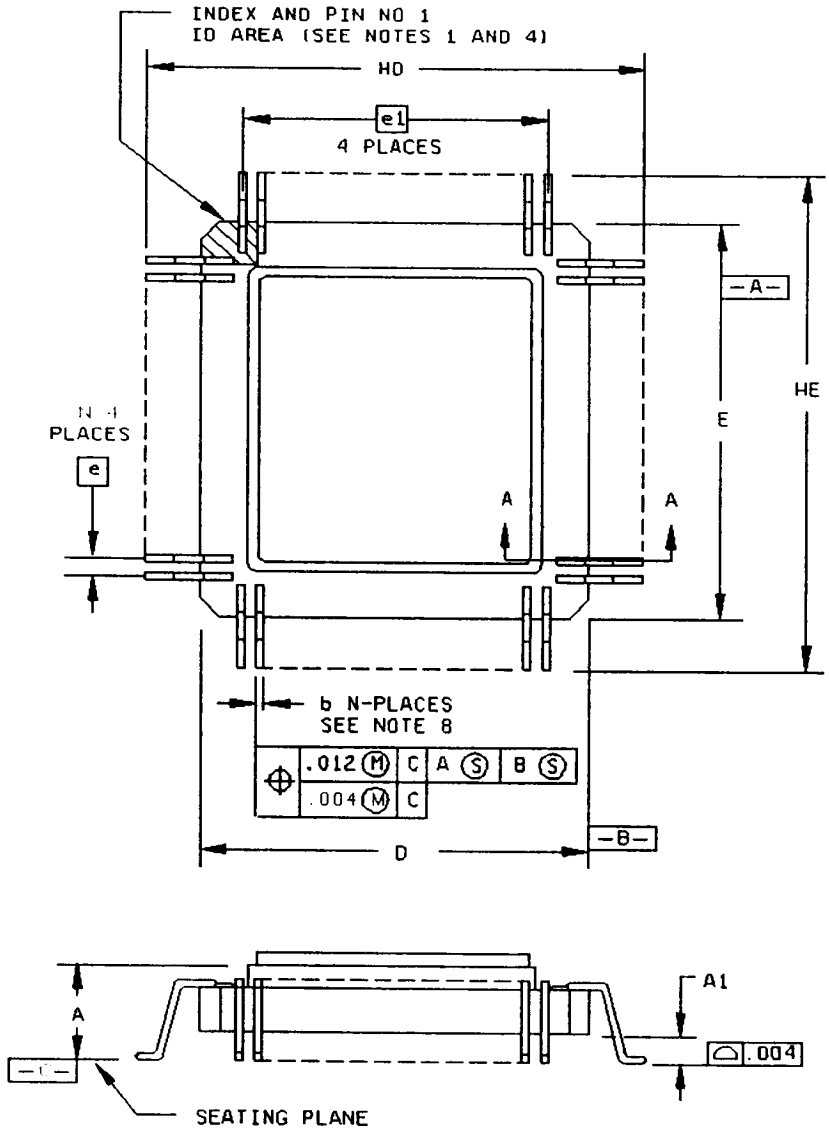
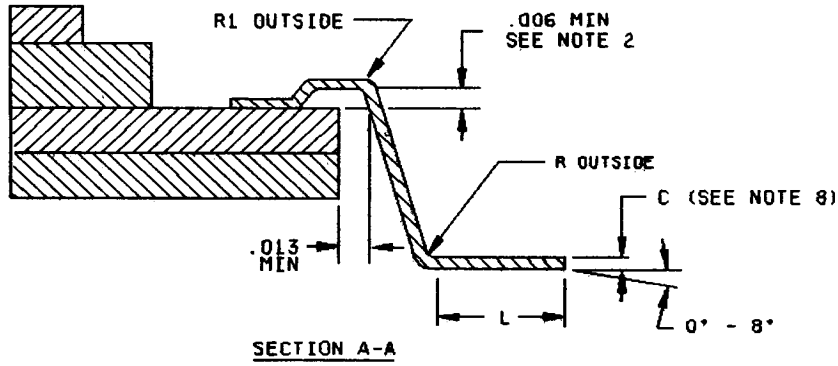


FIGURE 1. Case outlines.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89527
		REVISION LEVEL A	SHEET 13

Case outline Y



Case Y				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		.125		3.175
A1	.018	.035	0.457	0.889
b	.018	.030	0.457	0.762
c	.005	.010	0.127	0.254
D/E	.940	.960	23.88	24.38
e	.050 BSC		---	
e1	.600 BSC		---	
HD/HE	1.133	1.147	28.78	29.13
L	.024	.040	0.610	1.016
N	52		52	
R	.011	.034	0.279	0.864
R1	.009	---	0.229	---

NOTES:
1. A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.
2. Generic lead attach dogleg depiction.
3. Dimension N: Number of terminals.
4. Corner shapes (square, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
5. Metric equivalents are given for general information only.
6. Controlling dimension: Inch.
7. Datums X and Y to be determined where center leads exit the body.
8. Dimensions b and c include lead finish.

FIGURE 1. Case outlines - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	PA7/PAI/OC1	25	MODA/$\overline{LIR}$
2	PA6/OC2/OC1	26	STRA/AS
3	PA5/OC3/OC1	27	E
4	PA4/OC4/OC1	28	STRB/R/$\overline{W}$
5	PA3/OC5/OC1	29	EXTAL
6	PA2/IC1	30	XTAL
7	PA1/IC2	31	PC0/AD0
8	PA0/IC3	32	PC1/AD1
9	PB7/A15	33	PC2/AD2
10	PB6/A14	34	PC3/AD3
11	PB5/A13	35	PC4/AD4
12	PB4/A12	36	PC5/AD5
13	PB3/A11	37	PC6/AD6
14	PB2/A10	38	PC7/AD7
15	PB1/A9	39	$\overline{RESET}$
16	PB0/A8	40	$\overline{XIRQ}$
17	PE0/AN0	41	$\overline{IRQ}$
18	PE1/AN1	42	PD0/RxD
19	PE2/AN2	43	PD1/TxD
20	PE3/AN3	44	PD2/MISO
21	V_{RL}	45	PD3/MOSI
22	V_{RH}	46	PD4/SCK
23	V_{SS}	47	PD5/$\overline{SS}$
24	MODB/V_{stby}	48	V_{DD}

FIGURE 2. Terminal connections.

Device type	01		
Case outline	Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	XTAL	27	PA0/IC3
2	PC0/AD0	28	PB7/A15
3	PC1/AD1	29	PB6/A14
4	PC2/AD2	30	PB5/A13
5	PC3/AD3	31	PB4/A12
6	PC4/AD4	32	PB3/A11
7	PC5/AD5	33	PB2/A10
8	PC6/AD6	34	PB1/A9
9	PC7/AD7	35	PB0/A8
10	$\overline{\text{RESET}}$	36	PE0/AN0
11	$\overline{\text{XIRQ}}$	37	PE4/AN4
12	$\overline{\text{IRQ}}$	38	PE1/AN1
13	PD0/RxD	39	PE5/AN5
14	PD1/TxD	40	PE2/AN2
15	PD2/MISO	41	PE6/AN6
16	PD3/MOSI	42	PE3/AN3
17	PD4/SCK	43	PE7/AN7
18	PD5/$\overline{\text{SS}}$	44	V_{RL}
19	V_{DD}	45	V_{RH}
20	PA7/PAI/OC1	46	V_{SS}
21	PA6/OC2/OC1	47	MODB/V_{stby}
22	PA5/OC3/OC1	48	MODA/$\overline{\text{LIR}}$
23	PA4/OC4/OC1	49	STRA/AS
24	PA3/OC5/OC1	50	E
25	PA2/IC1	51	STRB/R/$\overline{\text{W}}$
26	PA1/IC2	52	EXTAL

FIGURE 2. Terminal connections - Continued.

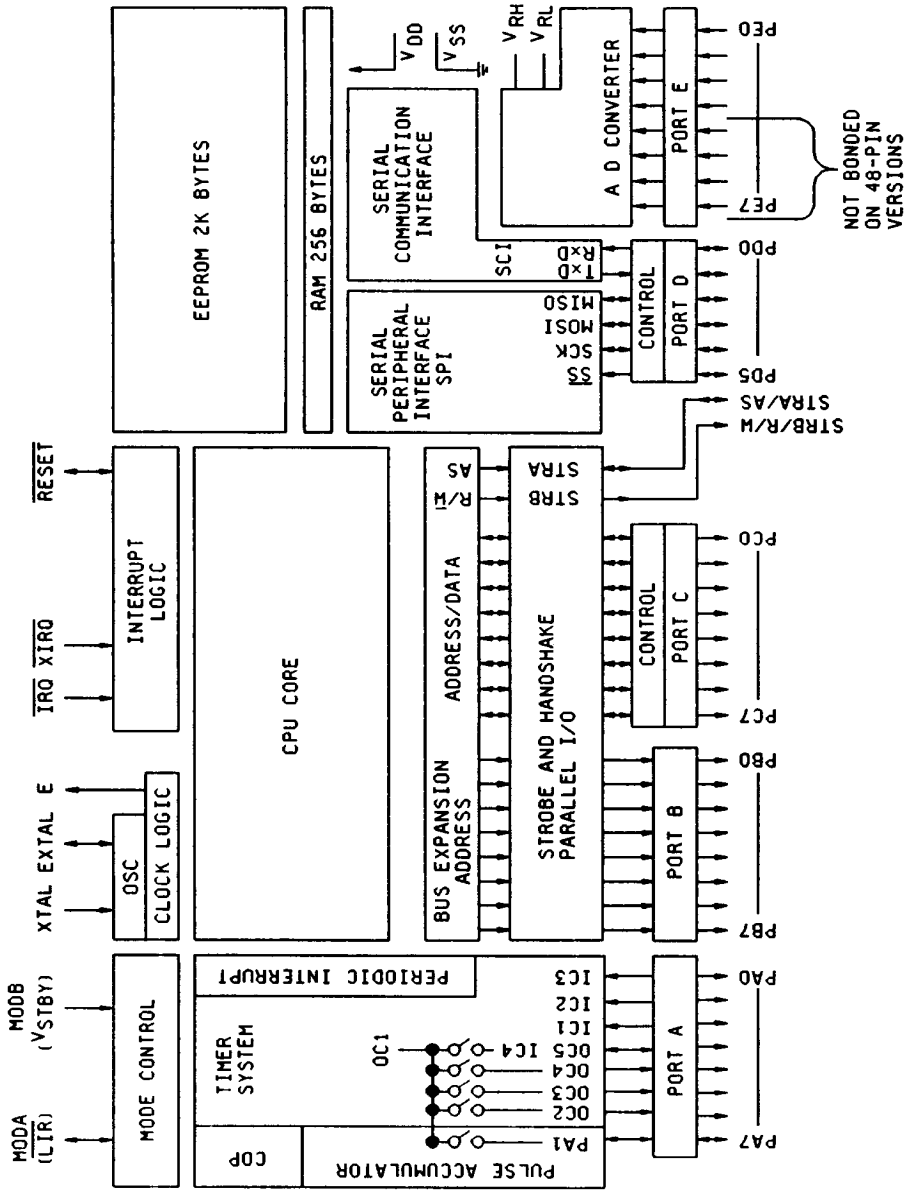


FIGURE 3. Block diagram.

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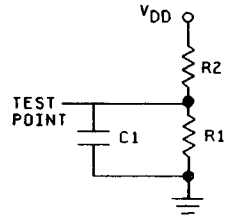
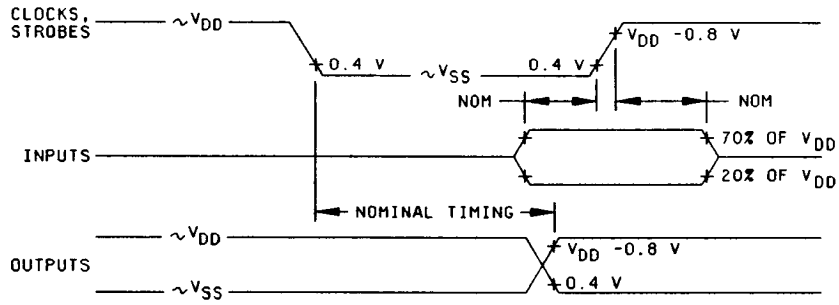
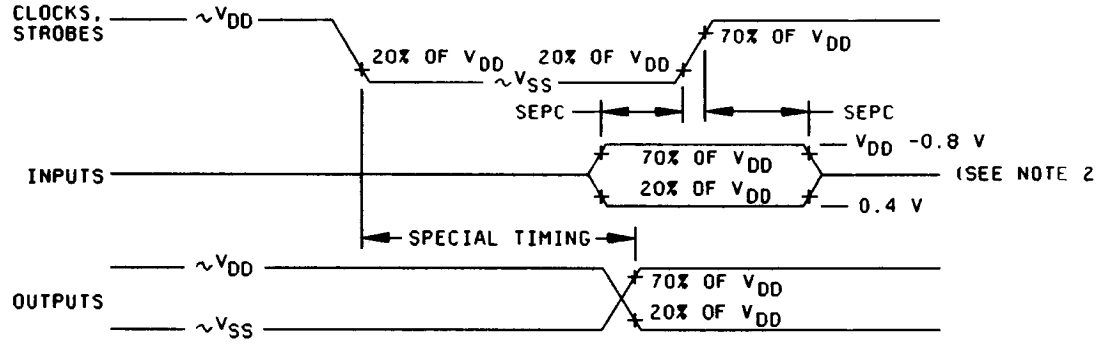
Equivalent test load



Pins	R1	R2	C1
PA3-PA7 PB0-PB7 PC0-PC7 PD0-PD5 E, AS, R/$\overline{W}$	3.26 k	2.38 k	90 pF
PD1-PD4	3.26 k	2.38 k	200 pF



DC testing

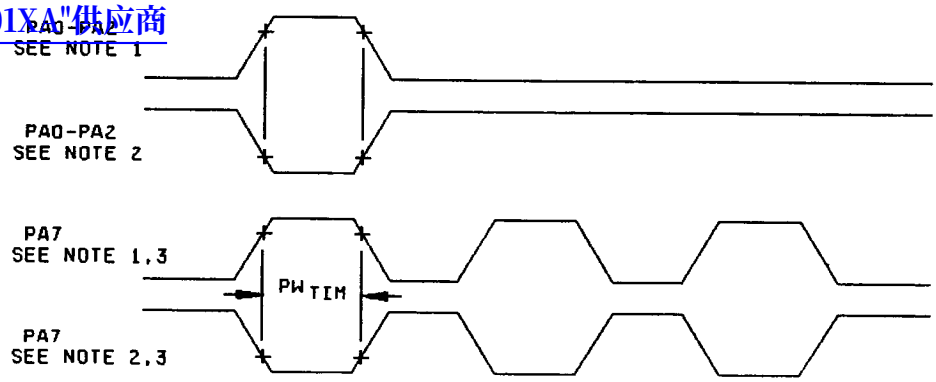


AC testing

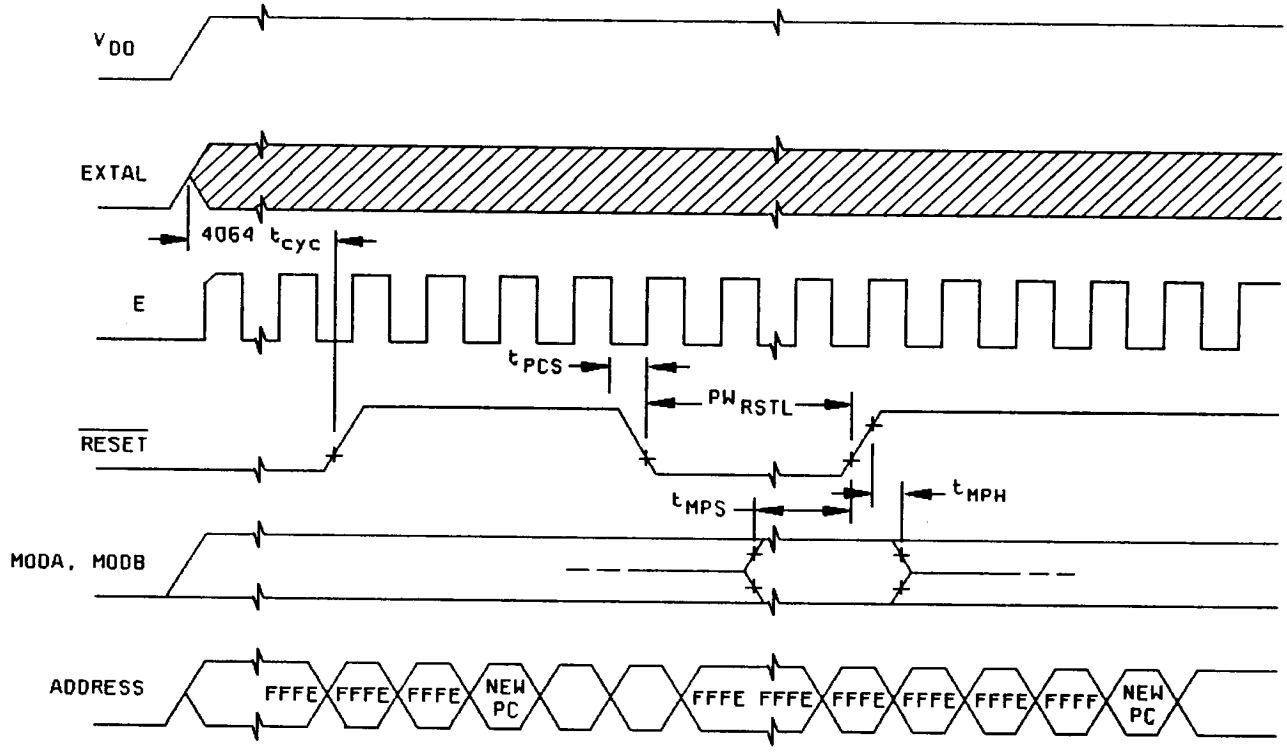
NOTES:
1. Full test loads are applied during all ac electrical tests and ac timing measurements.
2. During ac timing measurements, inputs are driven to 0.4 volt and V_{DD} -0.8 volt while timing measurements are taken at the 20 percent and 70 percent of V_{DD} points.

FIGURE 4. Test circuit and waveforms.

Timer inputs timing



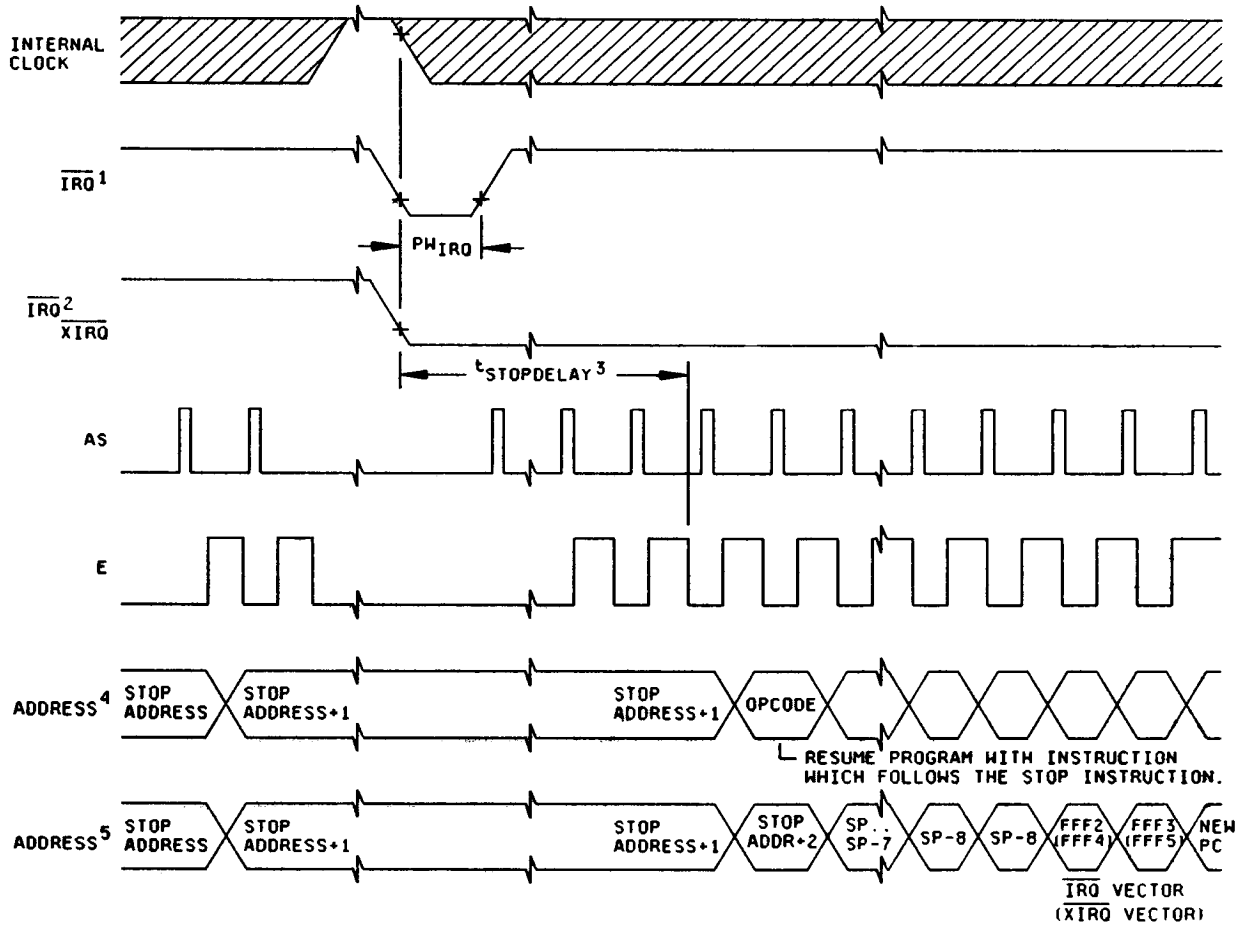
POR external reset timing



NOTES:
1. Rising edge sensitive input.
2. Falling edge sensitive input.
3. Maximum pulse accumulator clocking rate is E frequency divided by 2.

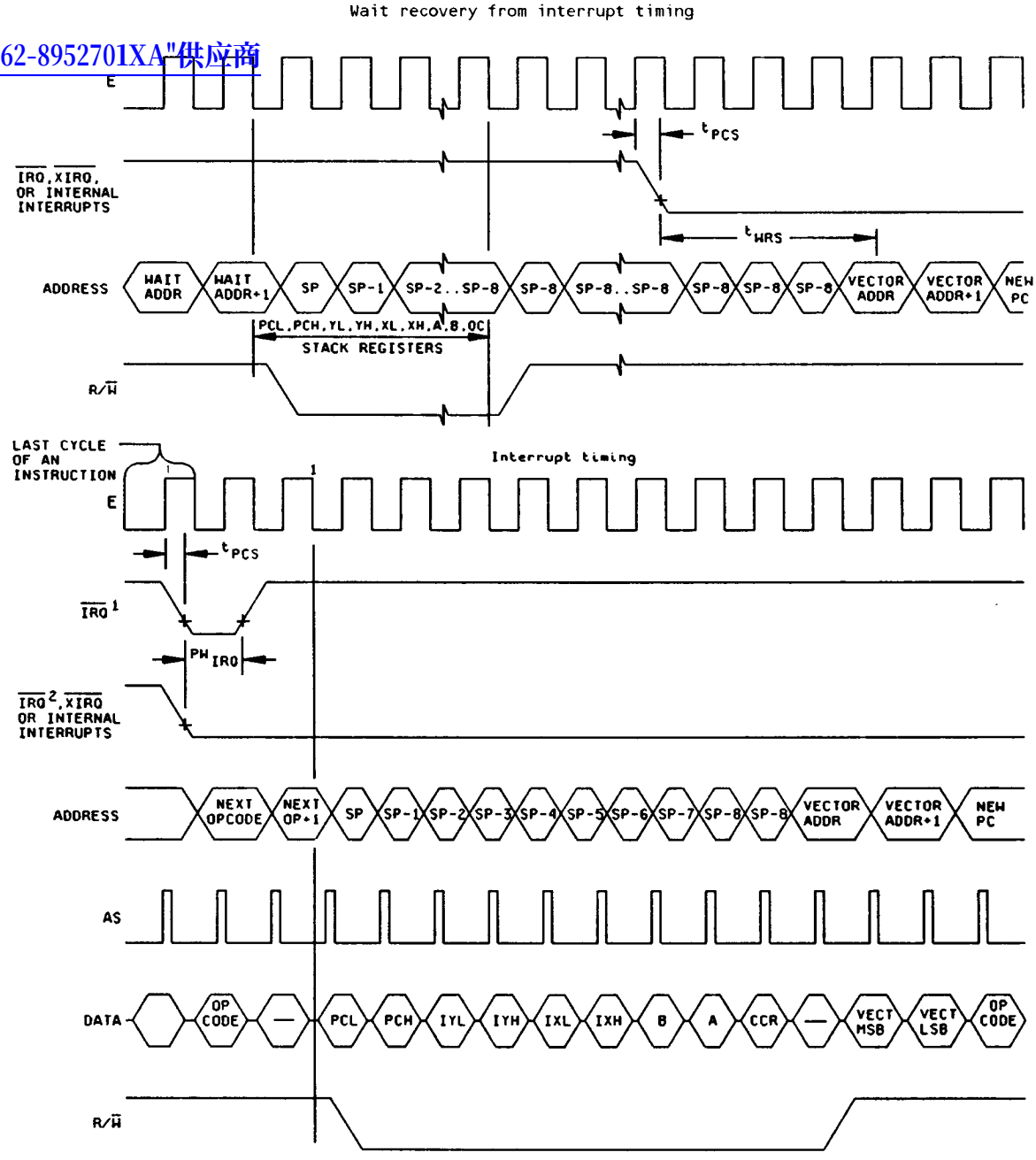
FIGURE 4. Test circuit and waveforms - Continued.

Stop recovery timing



NOTES:
1. Edge sensitive IRQ pin (IRQE bit = 1).
2. Level sensitive IRQ pin (IRQE bit = 0).
3. $t_{STOPDELAY}$ = 4064 t_{cyc} if DLY bit = 1 or 4 t_{cyc} if DLY = 0.
4. XIRQ with X bit in CCR = 1.
5. IRQ or XIRQ with X bit in CCR = 0.

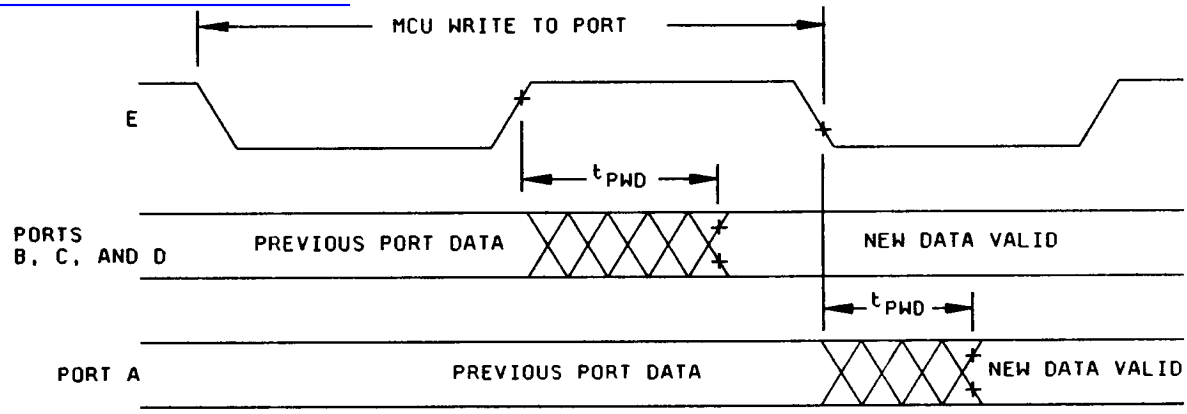
FIGURE 4. Test circuit and waveforms - Continued.



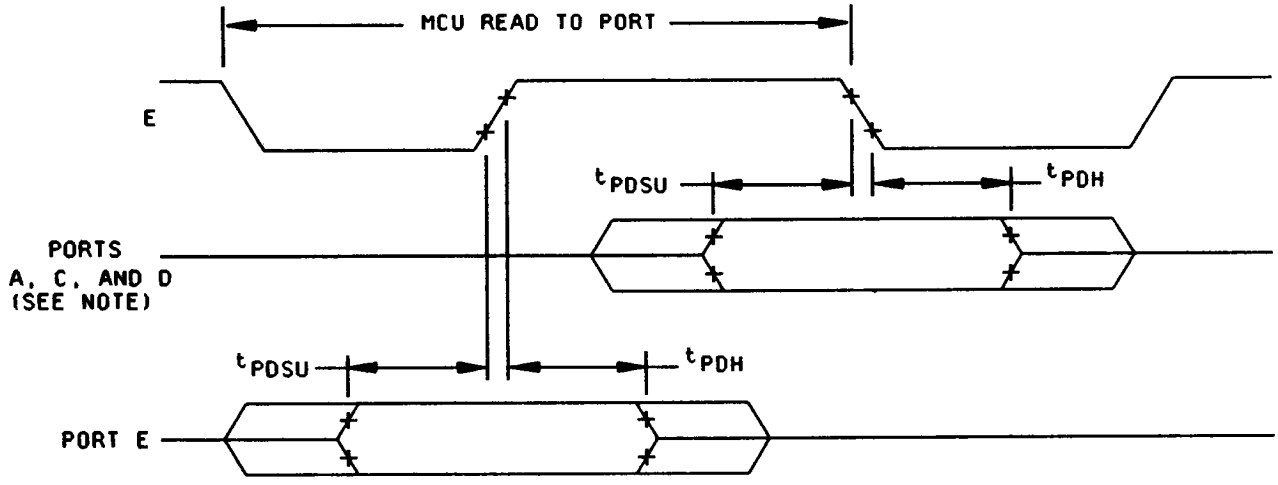
NOTES:
1. Edge sensitive $\overline{\text{IRQ}}$ pin (IRQE bit = 1).
2. Level sensitive $\overline{\text{IRQ}}$ pin (IRQE bit = 0).

FIGURE 4. Test circuit and waveforms - Continued.

Port write timing



Port read timing



NOTE: For nonlatched operation of port C.

FIGURE 4. Test circuit and waveforms - Continued.

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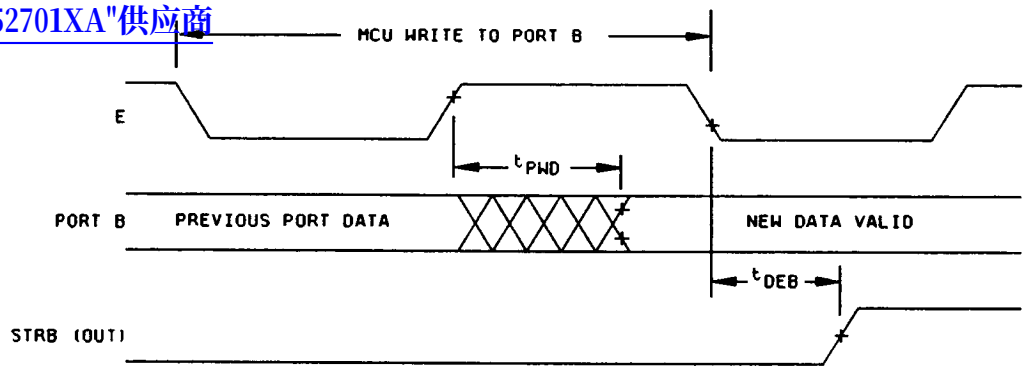
Simple output strobe timing



Simple input strobe timing

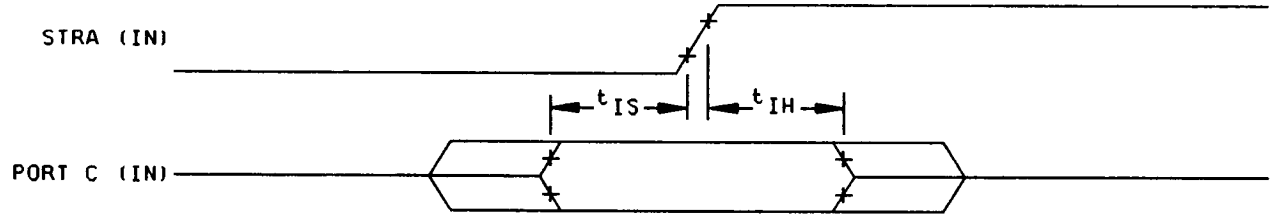
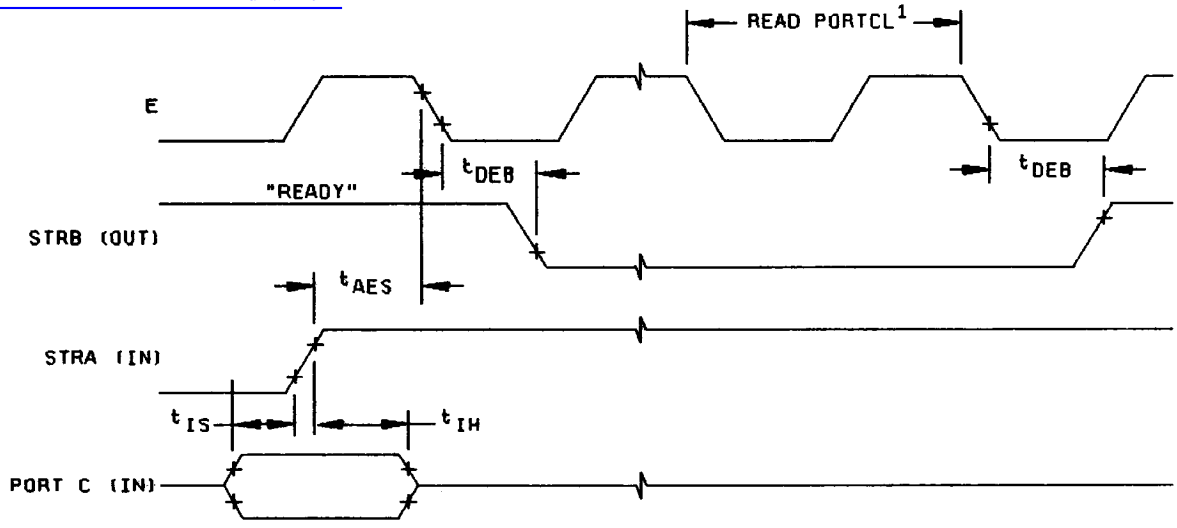
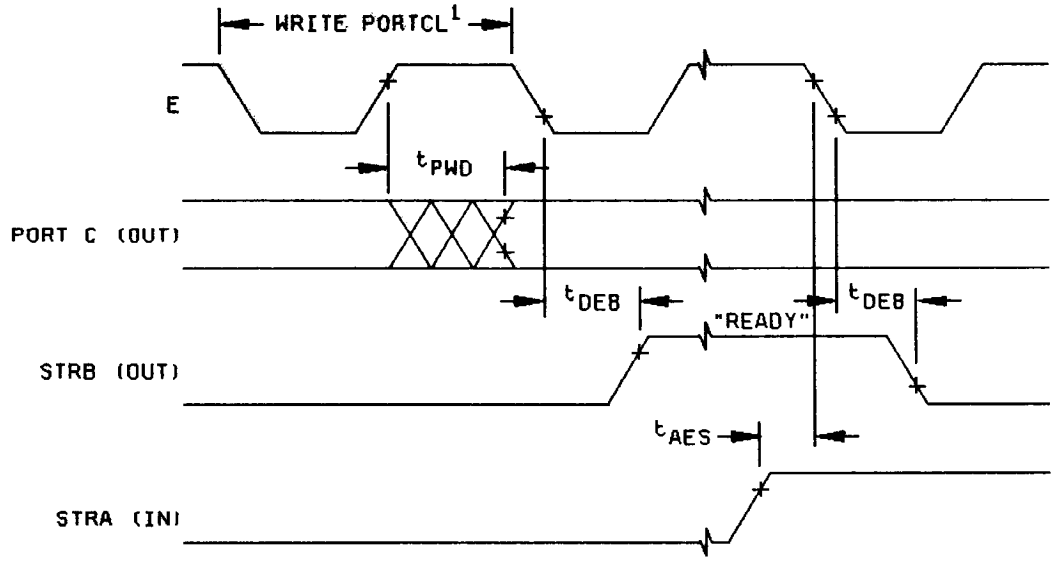


FIGURE 4. Test circuit and waveforms - Continued.

Port C input handshake timing



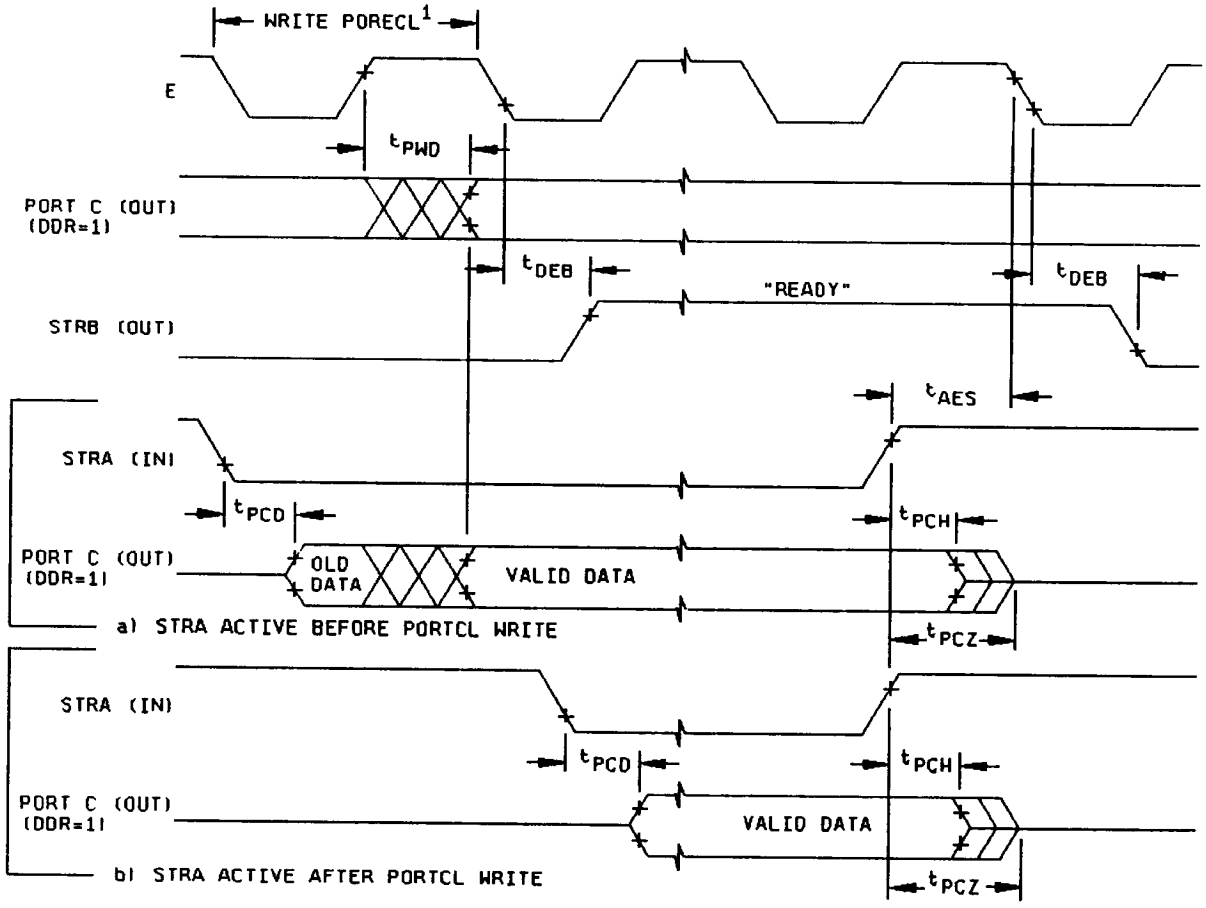
Port C output handshake timing



NOTES:
1. After reading PIOC with STAF set.
2. Figures show rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

FIGURE 4. Test circuit and waveforms - Continued.

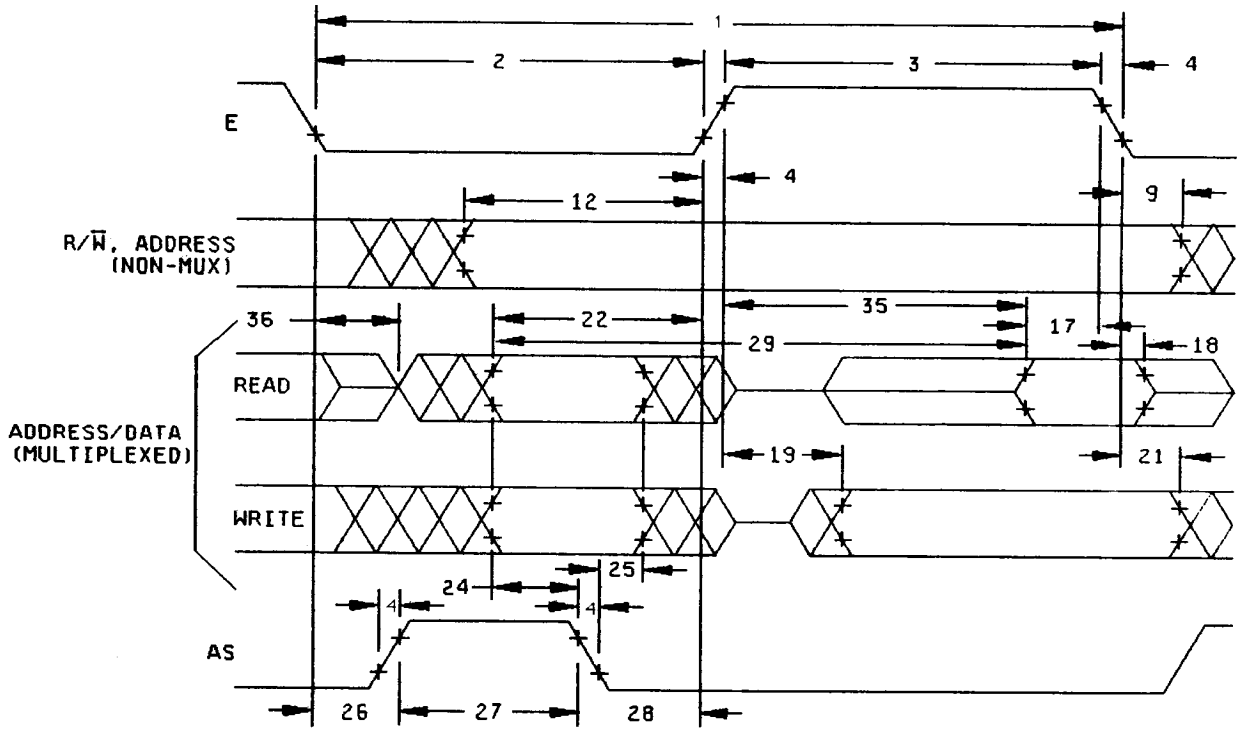
Three-state variation of output handshake timing
(STRA enables output buffer)



NOTES:
1. After reading PIOC with STAF set.
2. Figures show rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

FIGURE 4. Test circuit and waveforms - Continued.

Expansion bus timing

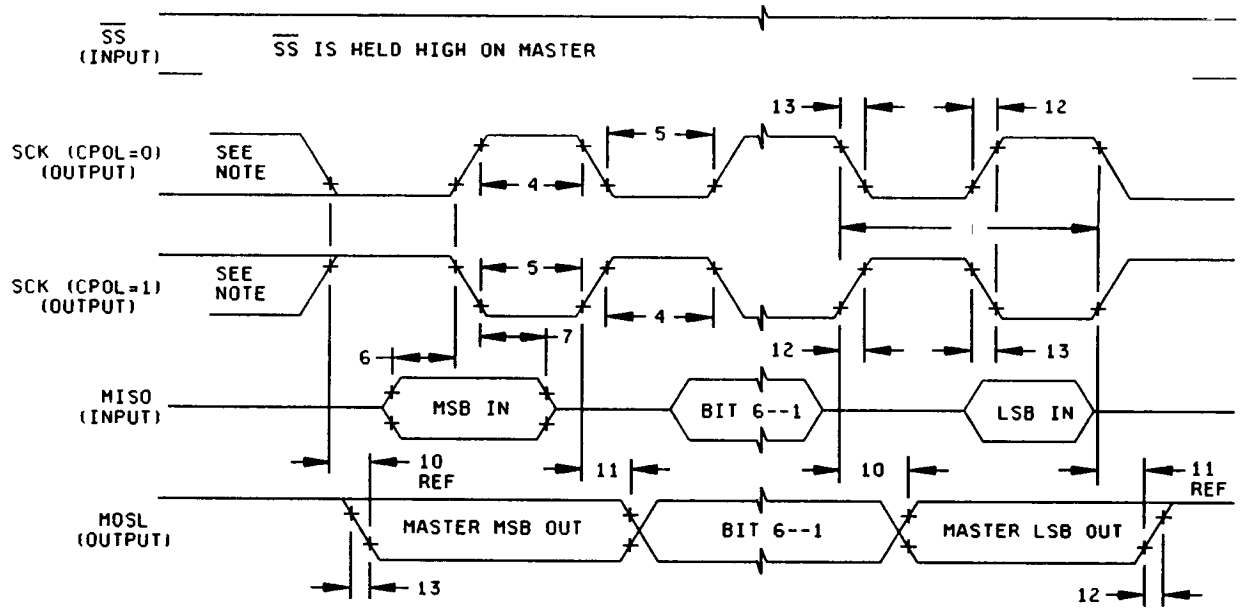


NOTE: Measurement points shown are 20 percent and 70 percent V_{DD}.

Waveform number references.

Number	Symbol	Number	Symbol	Number	Symbol	Number	Symbol
1	t_{cyc}	2	PW_{EL}	3	PW_{EH}	4	t_r, t_f
9	t_{AH}	12	t_{AV}	17	t_{DSR}	18	t_{DHR}
19	t_{DDW}	21	t_{DHW}	22	t_{AVM}	24	t_{ASL}
25	t_{AHL}	26	t_{ASD}	27	PW_{ASH}	28	t_{ASED}
29	t_{ACCA}	35	t_{ACCE}	36	t_{MAD}		

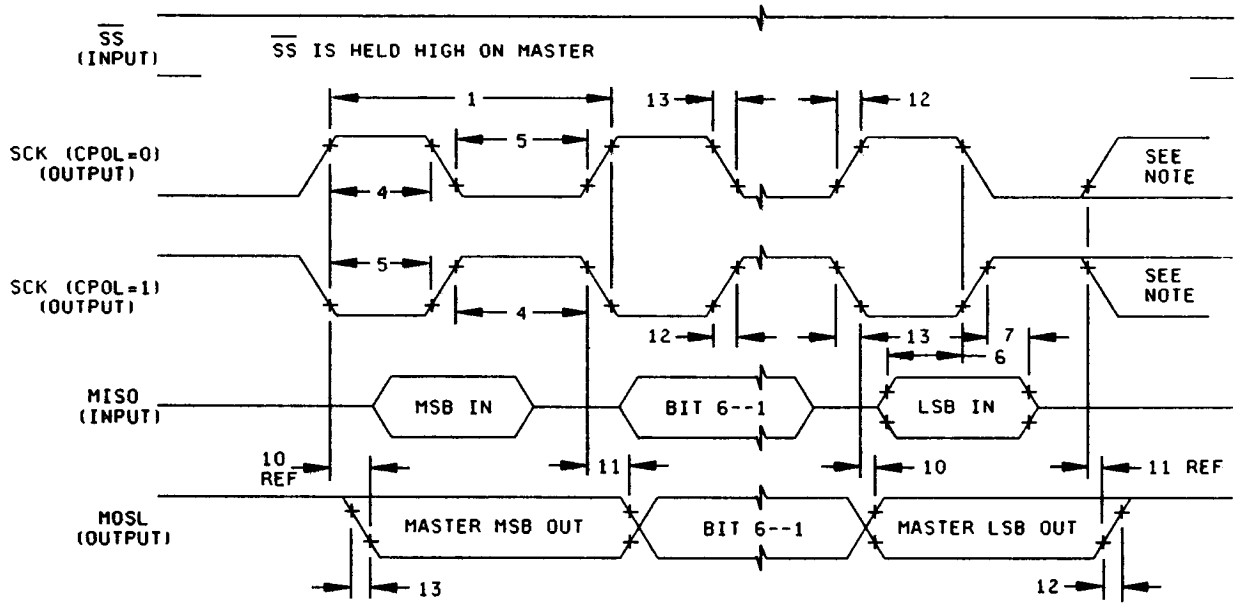
FIGURE 4. Test circuit and waveforms - Continued.



NOTE: This first clock edge is generated internally but is not seen at the SCK pin. SPI MASTER TIMING (CPHA = 0).

FIGURE 4. Test circuit and waveforms - Continued.

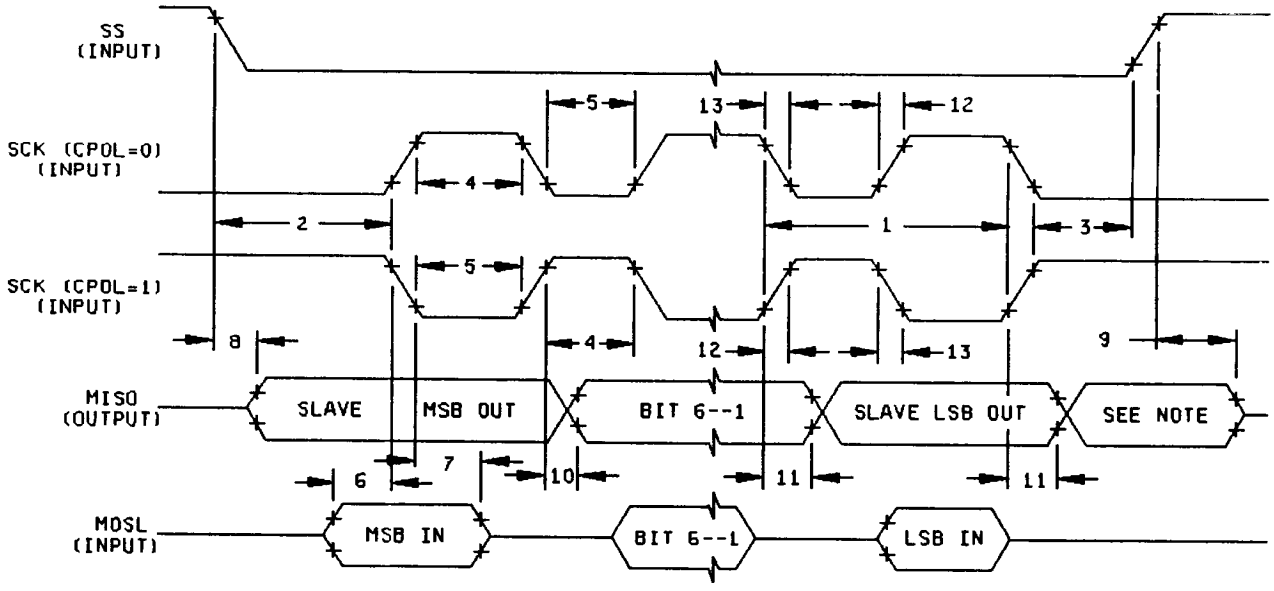
SPI timing



NOTE: This last clock edge is generated internally but is not seen at the SCK pin. SPI MASTER TIMING (CPHA = 0).

FIGURE 4. Test circuit and waveforms - Continued.

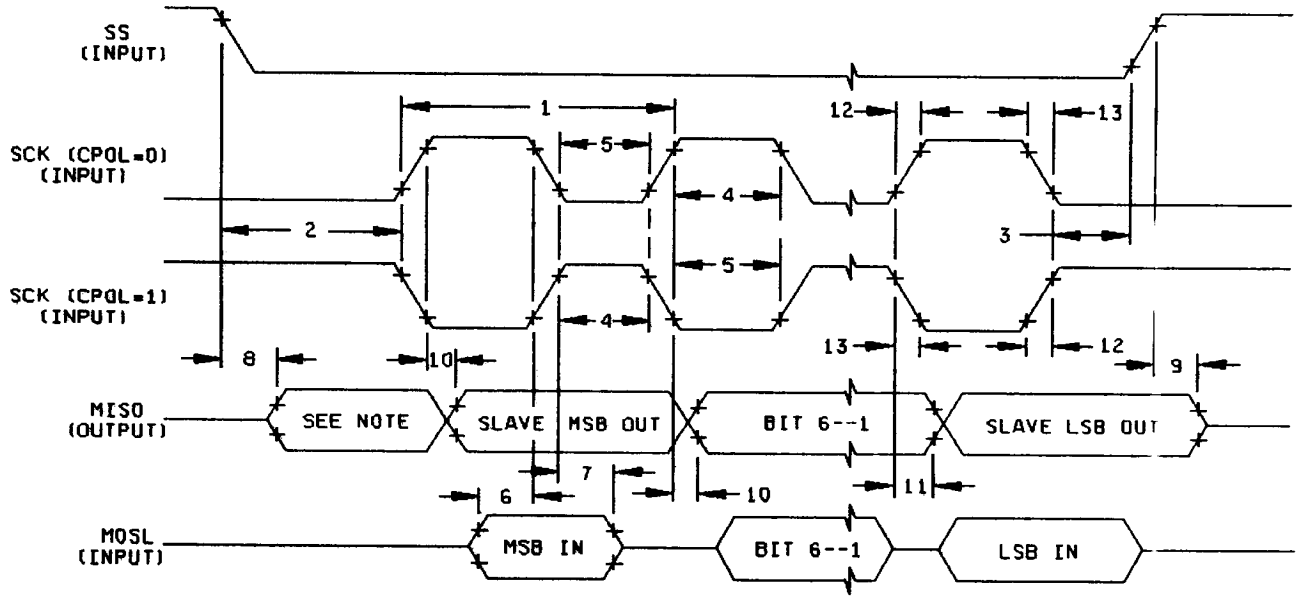
SPI timing



NOTE: Not defined but normally MSB of character just received. SPI SLAVE TIMING (CPHA = 0).

FIGURE 4. Test circuit and waveforms - Continued.

SPI timing



NOTE: Not defined but normally LSB of character previously transmitted. SPI SLAVE TIMING (CPHA = 0).

Waveform number references - SPI timing.

Number	Symbol	Master/slave	Number	Symbol	Master/slave
1	t_{cyc}	m,s	2	t_{lead}	m,s
3	t_{lag}	m,s	4	$t_{w(SCKH)}$	m,s
5	$t_{w(SCKL)}$	m,s	6	t_{su}	m,s
7	t_{h}	m,s	8	t_{a}	
9	t_{dis}		10	t_{v}	s
11	t_{ho}		12	t_{r}	m,s
13	t_{f}	m,s			

FIGURE 4. Test circuit and waveforms - Continued.

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EEPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EEPROM. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.10.2 Programmability of EEPROM. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.10.3 Verification of erasure or programmability of EEPROM. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. An endurance/data retention test prior to burn-in, in accordance with method 1033 of MIL-STD-883, shall be included as part of the screening procedure with the following conditions:

(1) Cycling may be block, byte, or page at +125°C and shall cycle all bytes for a minimum of 1000 cycles and the devices shall remain at +125°C for 24 hours.

(2) After cycling, perform a high temperature unbiased bake for 72 hours at 150°C (minimum). The storage time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship:

$A_F = \exp(-E_A/K*(1/T1 - 1/T2))$ where:

A_F = acceleration factor (unitless quantity) = t_1/t_2
T = temperature in Kelvin
t_1 = time (hrs) at temperature T1
t_2 = time (hrs) at temperature T2
K = Boltzmann's constant = 8.62 x 10^{-5}eV/°K using an apparent activation energy (E_A) of 0.6 V.

The maximum storage temperature shall not exceed 200°C for packaged devices or 300°C for unassembled devices.

(3) Read the data retention pattern and test using subgroups 1, 7, and 9 (minimum, e.g., high temperature equivalent subgroups 2, 8A, and 10 may be used) after cycling and bake, prior to burn-in. Devices having bits not in the proper state after storage shall constitute a device failure.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

c. All devices selected for testing shall have the EEPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

d. Subgroups 7 and 8 shall consist of verifying the EEPROM pattern specified and the instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available from the approved source of supply upon request.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

c. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. An endurance test, in accordance with method 1033 of MIL-STD-883, shall be added to group C1 inspection prior to performing the steady-state life test (see 4.3.2c) and extended data retention (see 4.3.2e).

Cycling may be block, byte, or page from devices passing group A after the completion of the requirements of 4.2 herein.

(1) All bytes shall be cycled for a minimum of 4,000 cycles at +25°C.

(2) Perform group A subgroups 1 and 7.

e. Extended data retention shall consist of:

(1) All devices shall be programmed with a charge on all memory cells in each device, such that the cell will read opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern, see 4.2c(2)).

(2) Perform a high temperature unbiased bake for 1000 hours at 150°C (minimum). The storage time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship:

$A_F = \exp(-E_A/K*(1/T1 - 1/T2))$ where:

A_F = acceleration factor (unitless quantity) = t_1/t_2
T = temperature in Kelvin
t_1 = time (hrs) at temperature T1
t_2 = time (hrs) at temperature T2
K = Boltzmann's constant = 8.62×10^{-5} eV/°K using an apparent activation energy (E_A) of 0.6 V.

The maximum storage temperature shall not exceed 200°C for packaged devices or 300°C for unassembled devices.

(3) Read the pattern after bake and perform endpoint electrical tests for table II herein for group C.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1, 7, 9
Final electrical test parameters (method 5004)	1*, 2, 3, 5, 6, 7, 8a, 9, 10, 11
Group A test requirements (method 5005)	1*, 2, 3, 4, 5, 6, 7, 8a, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

4.5 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Signal pin description

Pin name	Description
$\overline{\text{RESET}}$	Reset: This active low bidirectional control pin is used as an input to initialize the MCU to a known startup state and as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or the computer operating properly (COP) circuit.
XTAL, EXTAL	Crystal driver and external clock input: These pins provide the interface for either a crystal or a CMOS-compatible clock to control the internal clock generator circuitry. The frequency applied shall be four times higher than the desired clock rate.
E	E clock output: This pin provides an output for the internally generated E clock which can be used for timing reference. The frequency of the E output is one fourth that of the input frequency at the XTAL and EXTAL pins.
$\overline{\text{IRQ}}$	Interrupt request: This pin provides the capability for asynchronously applying interrupts to the MCU. Either negative edge-sensitive or level-sensitive triggering is program selectable. This pin is configured to level-sensitive during reset. An external resistor connected V_{DD} is required on IRQ.
$\overline{\text{XIRQ}}$	Non-maskable interrupt: This pin provides the capability for asynchronously applying non-maskable interrupts to the MCU after a power on reset (POR). During reset, the X bit in the condition code register is set, and any interrupt is masked until enabled by software. This input is level-sensitive and requires an external pullup resistor to V_{DD}.
MODA/$\overline{\text{LIR}}$ and MODB/V_{stby}	During reset, these pins are used to control the two basic operating modes and the two special operating modes. The LIR output can be used as an aid in debugging once reset is completed. The open-drain LIR pin goes to an active low during the first E-clock cycle of each instruction and remains low for the duration of that cycle. The Vstby (voltage standby) is used to retain RAM contents during device powerdown. The mode selections are shown below.
VRL, VRH	A/D converter reference voltages: These pins provide the reference voltage for the A/D converter.
V_{SS}	GND

MODB	MODA	Mode selected
1	0	Single chip
1	1	Expanded multiplexed
0	0	Special bootstrap
0	1	Special test

6.7 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.