NB6HQ14M

2.5V 5GHz / 6.5Gbps Differential Input to 1.8V / 2.5V 1:4 CML Clock / Data Fanout Buffer w/ Selectable Input Equalizer

Multi−Level Inputs w/ Internal Termination

ON Semiconductor®

http://onsemi.com

Description

The NB6HQ14M is a high performance differential 1:4 CML fanout buffer with a selectable Equalizer receiver. When placed in series with a Clock /Data path operating up to 5 GHz or 6.5 Gb/s, respectively, the NB6HQ14M inputs will compensate the degraded signal transmitted across a FR4 PCB backplane or cable interconnect and output four identical CML copies of the input signal. Therefore, the serial data rate is increased by reducing Inter−Symbol Interference (ISI) caused by losses in copper interconnect or long cables. The EQualizer ENable pin (EQEN) allows the IN/$\overline{IN}$ inputs to either flow through or bypass the Equalizer section. Control of the Equalizer function is realized by setting EQEN; When EQEN is set Low, the IN/$\overline{IN}$ inputs bypass the Equalizer. When EQEN is set High, the IN/$\overline{IN}$ inputs flow through the Equalizer. The default state at start−up is LOW. As such, NB6HQ14M is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications.

The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VT pin. This feature allows the NB6HQ14M to accept various logic level standards, such as LVPECL, CML or LVDS. The outputs have the flexibility of being powered by either a 2.5 V or 1.8 V supply. The 1:4 fanout design was optimized for low output skew applications.

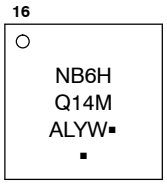
The NB6HQ14M is a member of the ECLinPS MAX™ family of high performance clock products.

Features

- Input Data Rate > 6.5 Gb/s
- Input Clock Frequency > 5 GHz
- 170 ps Typical Propagation Delay
- 35 ps Typical Rise and Fall Times
- < 15 ps Output Skew
- < 0.8 ps RMS Clock Jitter
- < 10 ps pp of Data Dependent Jitter
- Differential CML Outputs, 400 mV Peak−to−Peak, Typical
- Selectable Input Equalization
- Operating Range: V_{CC} = 2.375 V to 2.625 V, V_{CCO} = 1.71 V to 2.625 V
- Internal Input Termination Resistors, 50 Ω
- −40°C to +85°C Ambient Operating Temperature
- These are Pb−Free Devices

QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*

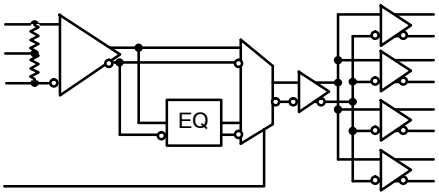


A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

SIMPLIFIED BLOCK DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

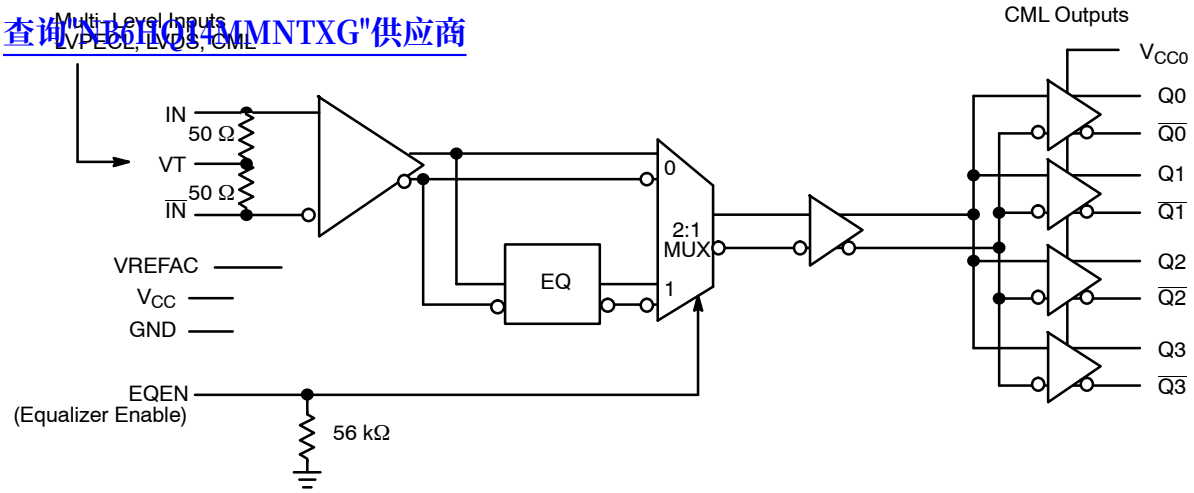


Figure 1. Detailed Block Diagram of NB6HQ14M

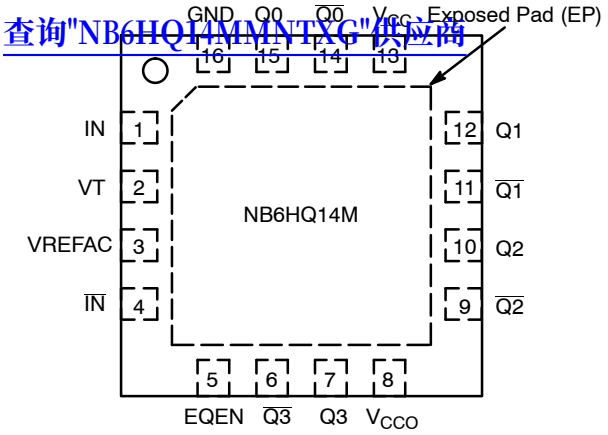


Figure 2. QFN−16 Pinout (Top View)

Table 1. EQUALIZER ENABLE FUNCTION

EQEN	Function
0	IN / $\overline{IN}$ Inputs By−pass the Equalizer section
1	Inputs flow through the Equalizer

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	IN	LVPECL, CML, LVDS Input	Non−inverted Differential Input. Note 1.
2	VT		Internal 100 Ω Center−tapped Termination Pin for IN / $\overline{IN}$
3	VREFAC		Output Voltage Reference for Capacitor−Coupled Inputs, only
4	$\overline{IN}$	LVPECL, CML, LVDS Input	Inverted Differential Input. Note 1.
5	EQEN	LVCMOS Input	Equalizer Enable Input; pin will default LOW when left open (has internal pull−down resistor)
6	$\overline{Q3}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
7	Q3	CML Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
8	VCCO	–	1.8 V or 2.5 V Positive Supply Voltage for the Qn / $\overline{Qn}$ CML Outputs
9	$\overline{Q2}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
10	Q2	CML Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
11	$\overline{Q1}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
12	Q1	CML Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
13	VCC	–	2.5 V Positive Supply Voltage for the core
14	$\overline{Q0}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
15	Q0	CML Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
16	GND	–	Negative Supply Voltage
–	EP	–	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pin (VT) is connected to a common termination voltage or left open, and if no signal is applied on IN / $\overline{IN}$ input, then, the device will be susceptible to self−oscillation.
2. All VCC, VCCO and GND pins must be externally connected to a power supply for proper operation.

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200V
R_{PD} – EQEN Input Pulldown Resistor		56 kΩ
Moisture Sensitivity (Note 3)	16–QFN	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in
Transistor Count		277
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply – Core	GND = 0 V		3.0	V
V_{CCO}	Positive Power Supply – Outputs	GND = 0 V		3.0	V
V_{IO}	Positive Input/Output Voltage	GND = 0 V		–0.5 to V_{CC} + 0.5	V
V_{INPP}	Differential Input Voltage |IN – $\overline{IN}$|			1.89	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)			±40	mA
I_{OUT}	Output Current Through R_T (50 Ω Resistor)			±40	mA
$I_{VFREFAC}$	VREFAC Sink/Source Current			±1.5	mA
T_A	Operating Temperature Range	16 QFN		–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) (Note 4)	0 lfpm 500 lfpm	16 QFN 16 QFN	42 35	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case) (Note 4)		16 QFN	4	°C/W
T_{sol}	Wave Solder Pb–Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS, MULTI−LEVEL INPUTS V_{CC} = 2.375 V to 2.625 V; V_{CCO} = 1.71 V to 2.625 V; GND = 0 V; T_A = −40°C to 85°C (Note 5)

Symbol	Characteristic		Min	Typ	Max	Unit
POWER SUPPLY / CURRENT						
V_{CC} V_{CCO}	Power Supply Voltage	V_{CC} = 2.5 V V_{CCO} = 2.5 V V_{CCO} = 1.8 V	2.375 2.375 1.71	2.5 2.5 1.8	2.625 2.625 1.89	V
I_{CC} I_{CCO}	Power Supply Current for VCC (Inputs and Outputs Open) Power Supply Current for VCCO (Inputs and Outputs Open)			75 65	110 90	mA
CML OUTPUTS (Note 6)						
V_{OH}	Output HIGH Voltage	V_{CCO} = 2.5 V V_{CCO} = 1.8 V	V_{CCO} − 30 2470 1770	V_{CCO} − 10 2490 1790	V_{CCO} 2500 1800	mV
V_{OL}	Output LOW Voltage	V_{CCO} = 2.5 V V_{CCO} = 1.8 V	V_{CCO} − 550 1950 1250	V_{CCO} − 450 2050 1350	V_{CCO} − 300 2200 1500	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (see Figure 5 & 7) (Note 7)						
V_{IH}	Single−ended Input HIGH Voltage		Vth + 100		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage		GND		Vth −100	mV
V_{th}	Input Threshold Reference Voltage Range (Note 8)		1100		V_{CC} − 100	mV
V_{ISE}	Single−ended Input Voltage Amplitude (V_{IH} − V_{IL})		200		2800	mV
VREFAC						
V_{REFAC}	Output Reference Voltage @100 μA for capacitor− coupled inputs, only		V_{CC} − 1325	V_{CC} − 1125	V_{CC} − 925	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figure 6 & 8) (Note 9)						
V_{IHD}	Differential Input HIGH Voltage		1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage		0		V_{IHD} − 100	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})		100		1200	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 10) (Figure 9)		1050		V_{CC} − 50	mV
I_{IH}	Input HIGH Current IN / $\overline{IN}$, (VT Open)		−150		150	uA
I_{IL}	Input LOW Current IN / $\overline{IN}$, (VT Open)		−150		150	uA
CONTROL INPUTS (EQEN)						
V_{IH}	Input HIGH Voltage for Control Pins		V_{CC} x 0.65		V_{CC}	V
V_{IL}	Input LOW Voltage for Control Pins		GND		V_{CC} x 0.35	V
I_{IH}	Input HIGH Current		−150		150	μA
I_{IL}	Input LOW Current		−150		150	μA
TERMINATION RESISTORS						
R_{TIN}	Internal Input Termination Resistor		45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor		45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input parameters vary 1:1 with V_{CC}. Output parameters vary 1:1 with V_{CCO}.
6. CML outputs loaded with 50 Ω to V_{CCO} for proper operation.
7. Vth, V_{IH}, $V_{IL,}$, and V_{ISE} parameters must be complied with simultaneously.
8. Vth is applied to the complementary input when operating in single−ended mode.
9. V_{IHD}, $V_{ILD,}$ V_{ID} and V_{CMR} parameters must be complied with simultaneously.
10. V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the crosspoint side of the differential input signal.

Table 5. AC CHARACTERISTICS (V_{EE} = −2.375 V to 2.625 V; V_{CCO} = 1.71 V to 2.625 V; GND = 0 V; T_A = −40°C to 85°C (Note 11)

Symbol	Characteristic		Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency;	$V_{OUT} \geq$ 200 mV	5	7		GHz
$f_{DATAMAX}$	Maximum Operating Data Rate (PRBS23)		6.5	10		Gbps
V_{OUTPP}	Output Voltage Amplitude, EQEN = 0 or 1 (Note 15) (See Figures 3 and 10)	$f_{in} \leq$ 5 GHz	200	400		mV
t_{PLH}, t_{PHL}	Propagation Delay, EQEN = 0 or 1	IN to Q	150	220	275	ps
t_{SKEW}	Duty Cycle Skew (Note 12) Output − Output Within Device Skew Device to Device Skew			 3 10	15 15 50	ps
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	f_{in} = 1 GHz	45	50	55	%
Φ_N	Phase Noise, fin = 1 GHz	10 kHz 100 kHz 1 MHz 10 MHz 20 MHz 40 MHz		−132 −135 −145 −146 −147 −148		dBc
$t_{\int \Phi N}$	Integrated Phase Jitter f_{in} = 1 GHz, 12 kHz − 20 MHz Offset (RMS)			50		fs
t_{JITTER}	RMS Random Clock Jitter (Note 13)	$f_{in} \leq$ 5 GHz		0.2	0.8	ps rms
	Peak−to−Peak Data Dependent Jitter (Note 14)	$f_{in} \leq$ 3.0 Gb/s EQEN = 0 ($\leq$ 3" FR4) EQEN = 1 (12" FR4)			 15 10	 ps pk−pk ps pk−pk
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 15)		100		1200	mV
t_r t_f	Output Rise/Fall Times @ 1.0 GHz (20% − 80%)	Qx, $\overline{Qx}$	15	30	60	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured by forcing V_{INPP} min from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CCO}. Input edge rates 40 ps (20% − 80%).
12. Skew is measured between outputs under identical transitions and conditions @ 0.5 GHz. Duty cycle skew is measured between differential outputs using the deviations of the sum of Tpw− and Tpw+ @ 0.5 GHz.
13. Additive RMS jitter with 50% duty cycle clock signal.
14. Additive peak−to−peak data dependent jitter with input NRZ data at PRBS23. For applications requiring equalization, the vertical eye height is also a critical figure of merit. See Figure 4 for equalized eye height versus data rate.
15. Input and output voltage swings are single−ended measurements operating in a differential mode.

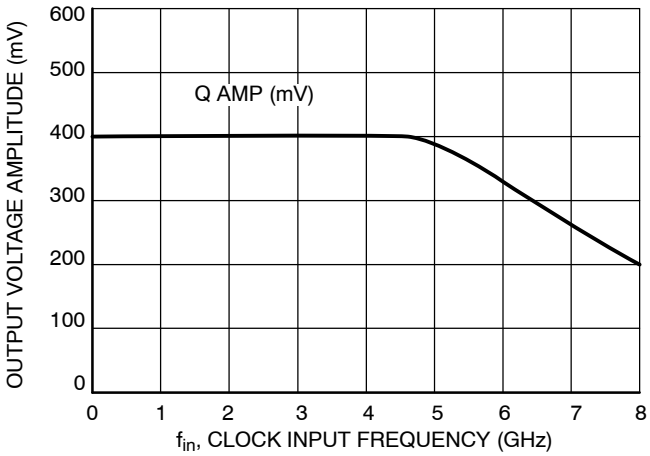


Figure 3. CLOCK Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

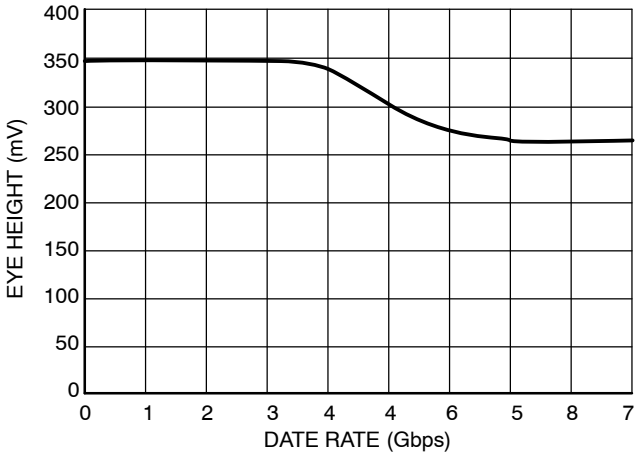


Figure 4. NB6HQ14M Eye Height vs. Data Rate

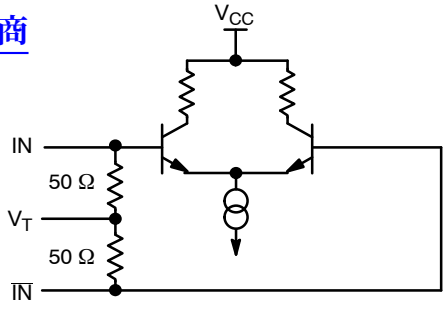


Figure 5. Input Structure

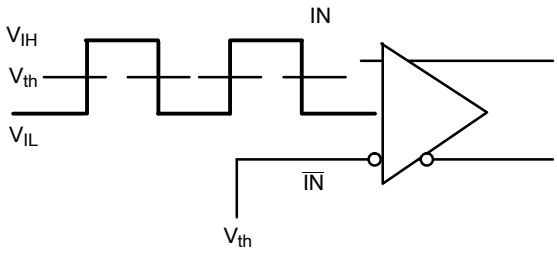


Figure 6. Differential Input Driven Single−Ended

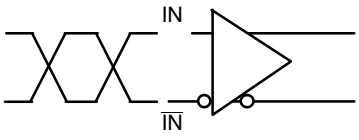


Figure 7. Differential Inputs Driven Differentially

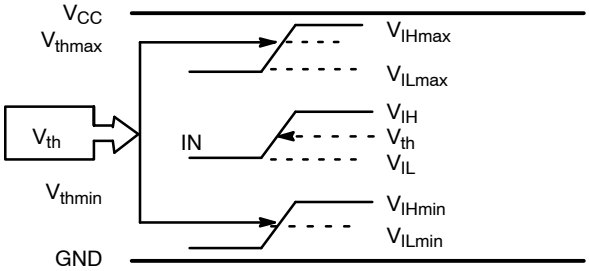


Figure 8. V_{th} Diagram

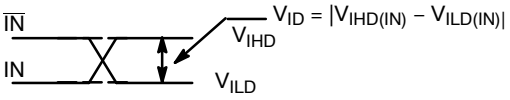


Figure 9. Differential Inputs Driven Differentially

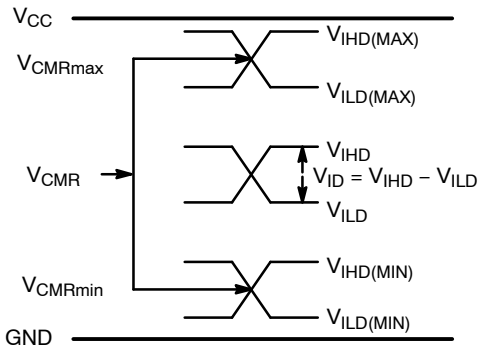


Figure 10. V_{CMR} Diagram

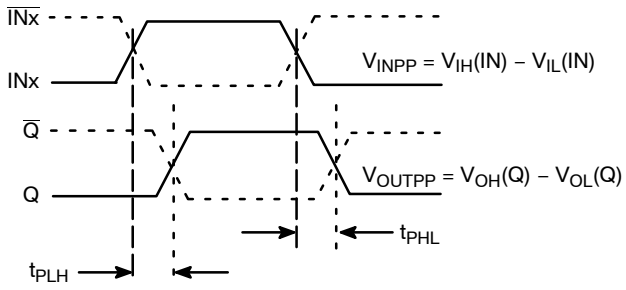


Figure 11. AC Reference Measurement

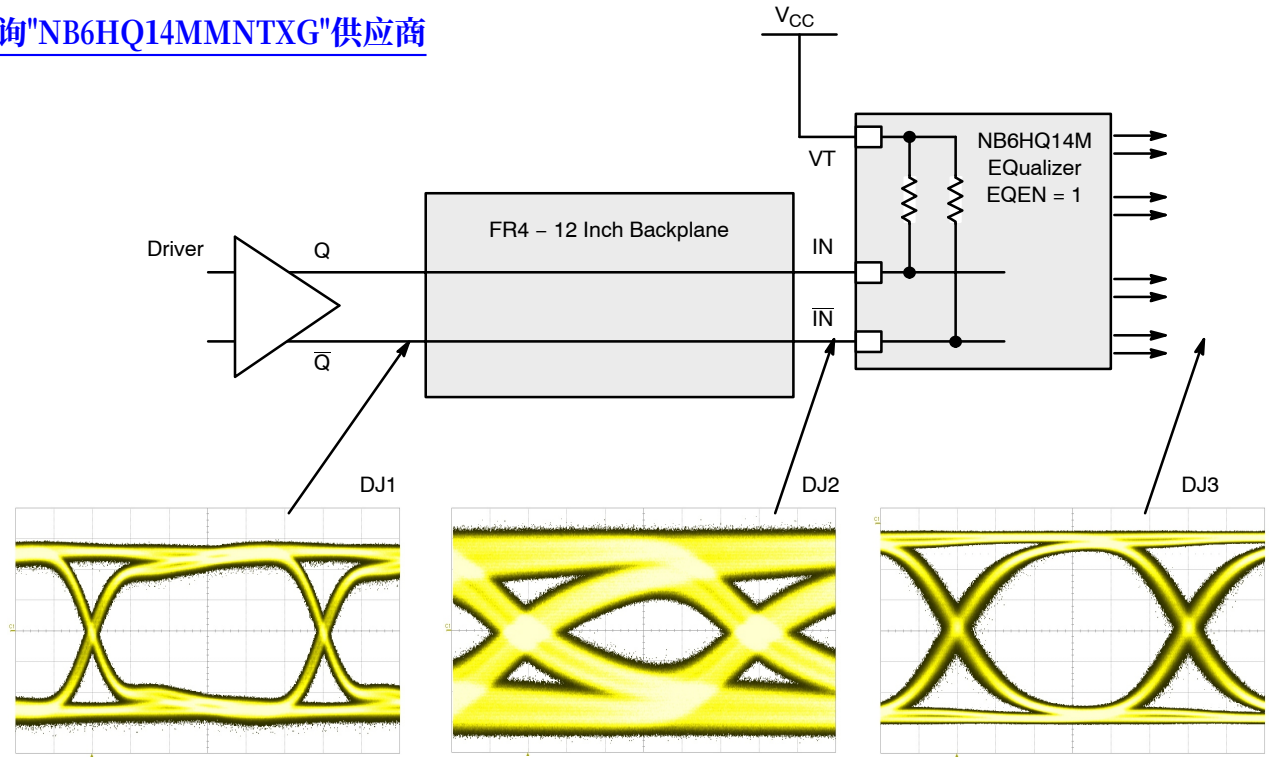


Figure 12. Typical NB6HQ14M Equalizer Application and Interconnect with PRBS23 pattern at 6.5 Gbps, EQEN = 1

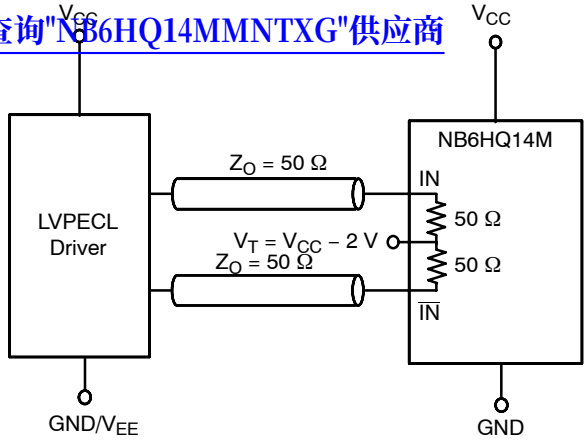


Figure 13. LVPECL Interface

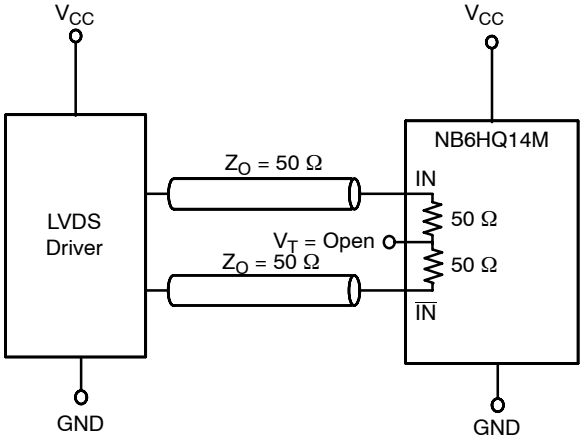


Figure 14. LVDS Interface

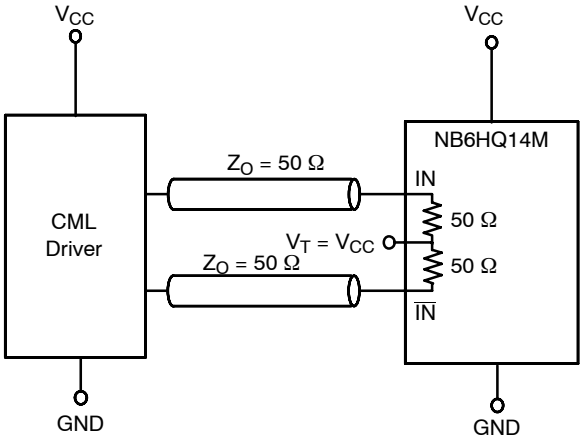


Figure 15. Standard 50 Ω Load CML Interface

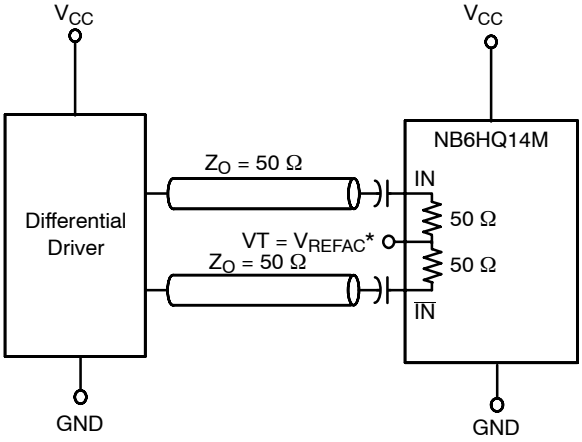


Figure 16. Capacitor−Coupled Differential Interface (V_T Connected to V_{REFAC})

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor

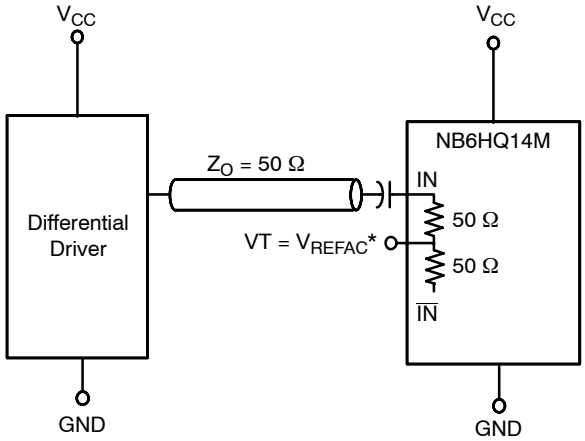


Figure 17. Capacitor−Coupled Single−Ended Interface (V_T Connected to V_{REFAC})

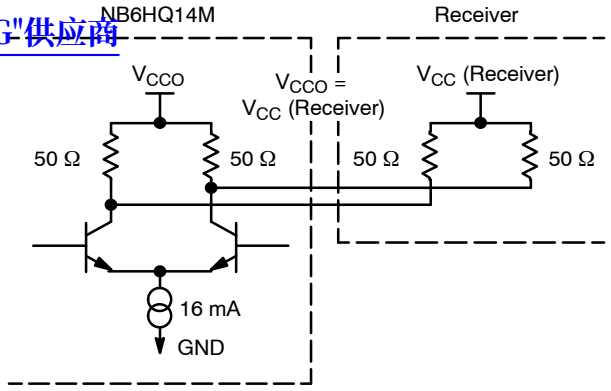


Figure 18. Typical CML Output Structure and Termination

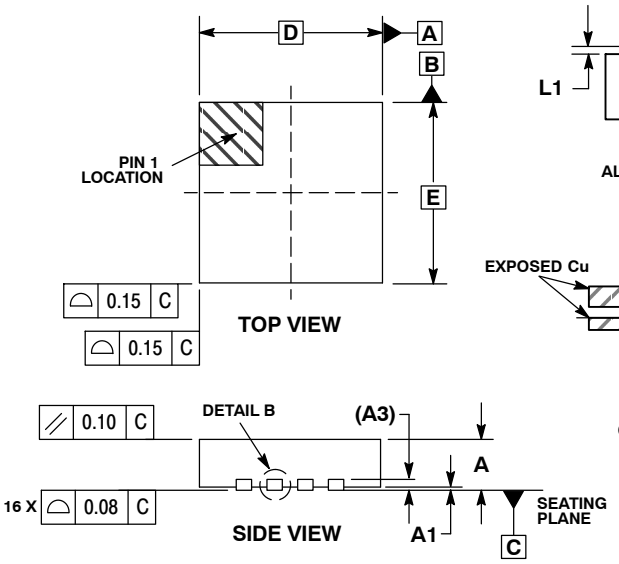
ORDERING INFORMATION

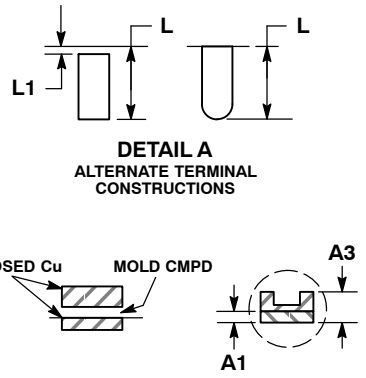
Device	Package	Shipping†
NB6HQ14MMNG	QFN−16 (Pb−Free)	123 Units / Rail
NB6HQ14MMNHTBG	QFN−16 (Pb−Free)	100 / Tape & Reel
NB6HQ14MMNTXG	QFN−16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

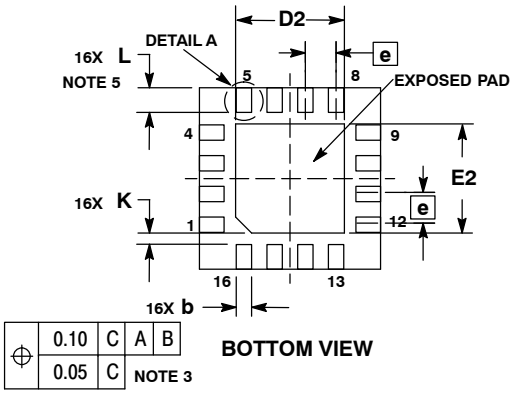
16 PIN QFN
CASE 485G−01
ISSUE D



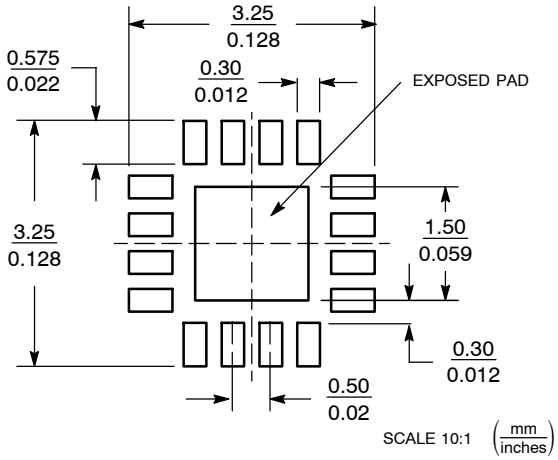


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50
L1	0.00	0.15



SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

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