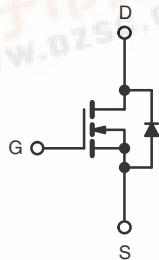
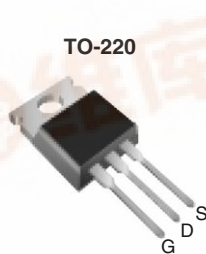


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	400	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.55
$Q_g$ (Max.) (nC)	36	
$Q_{gs}$ (nC)	9.9	
$Q_{gd}$ (nC)	16	
Configuration	Single	



N-Channel MOSFET

### FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective  $C_{OSS}$  Specified
- Compliant to RoHS Directive 2002/95/EC



RoHS\*  
COMPLIANT

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High Speed Power Switching

### TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset (Both for US Line Input Only)

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRF740APbF
	SiHF740A-E3
SnPb	IRF740A
	SiHF740A

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	400	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25^\circ\text{C}$	10
		$T_C = 100^\circ\text{C}$	6.3
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	40	A
Linear Derating Factor		1.0	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	630	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	10	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	12.5	mJ
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	125
Peak Diode Recovery $dV/dt^c$		$dV/dt$	5.9
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>
Mounting Torque	6-32 or M3 screw		10
			1.1


#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50$  V, starting  $T_J = 25^\circ\text{C}$ ,  $L = 12.6$  mH,  $R_G = 25$   $\Omega$ ,  $I_{AS} = 10$  A (see fig. 12).
- $I_{SD} \leq 10$  A,  $dV/dt \leq 330$  A/ $\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply



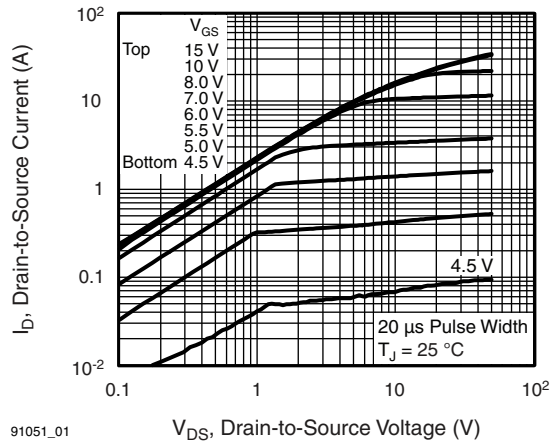
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	400	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.48	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6.0\text{ A}^b$	-	-	0.55	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 6.0\text{ A}^b$	4.9	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$	-	1030	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$		-	170	-	
Reverse Transfer Capacitance	$C_{rss}$		-	7.7	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}, V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	1490	-	$\mu\text{F}$
		$V_{GS} = 0\text{ V}, V_{DS} = 320\text{ V}, f = 1.0\text{ MHz}$	-	52	-	
Effective Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 320\text{ V}$	-	61	-	$\mu\text{F}$
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}, V_{DS} = 320\text{ V}, \text{ see fig. 6 and 13}^b$	-	-	36	nC
Gate-Source Charge	$Q_{gs}$		-	-	9.9	
Gate-Drain Charge	$Q_{gd}$		-	-	16	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 200\text{ V}, I_D = 10\text{ A}, R_g = 10\text{ }\Omega, R_D = 19.5\text{ }\Omega, \text{ see fig. 10}^b$	-	10	-	ns
Rise Time	$t_r$		-	35	-	
Turn-Off Delay Time	$t_{d(off)}$		-	24	-	
Fall Time	$t_f$		-	22	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	10	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	40	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 10\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	2.0	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	240	360	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	1.9	2.9	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

### Notes

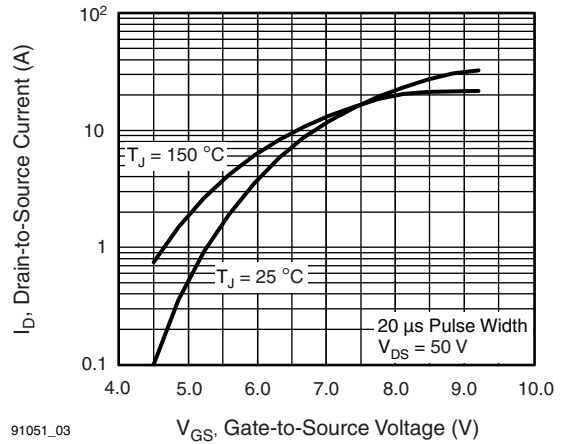
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



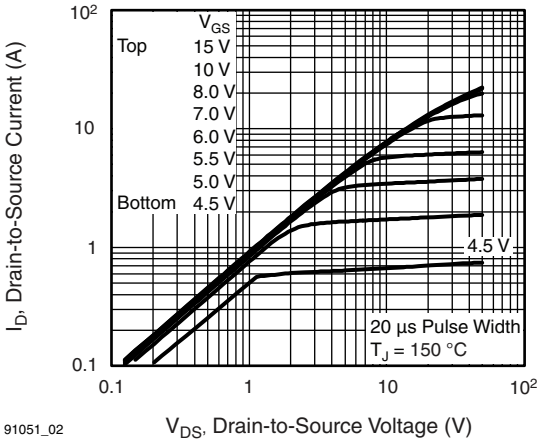
91051\_01

**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$**



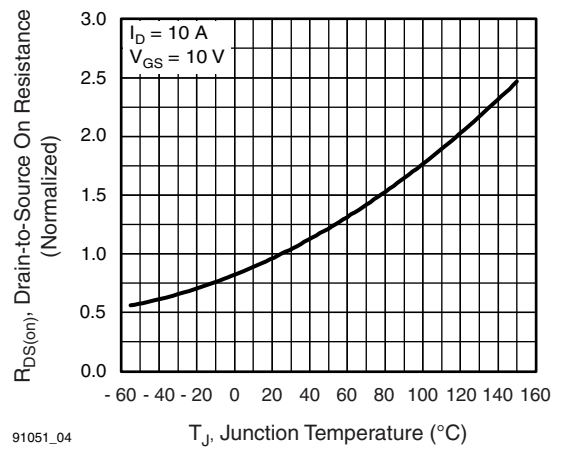
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**Fig. 3 - Typical Transfer Characteristics**



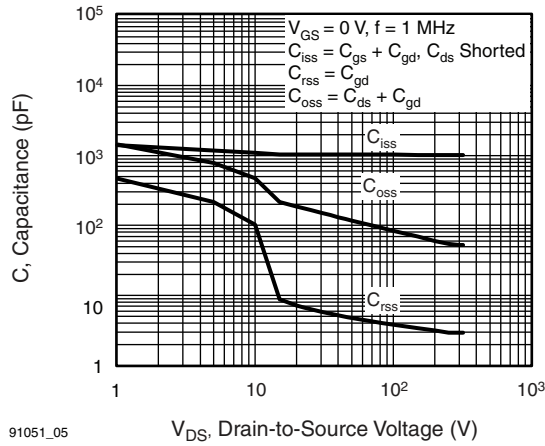
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**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$**

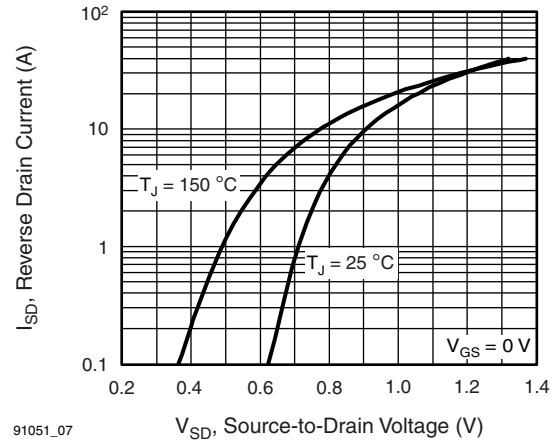


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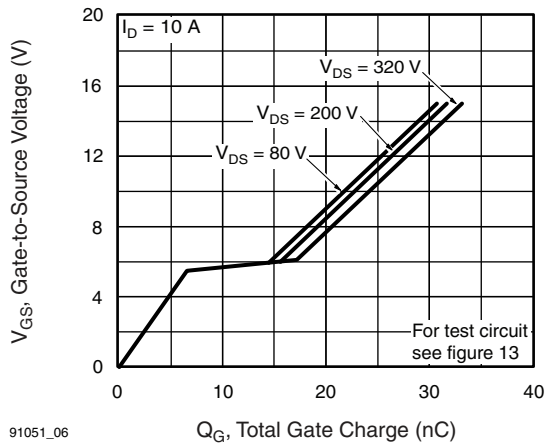
**Fig. 4 - Normalized On-Resistance vs. Temperature**



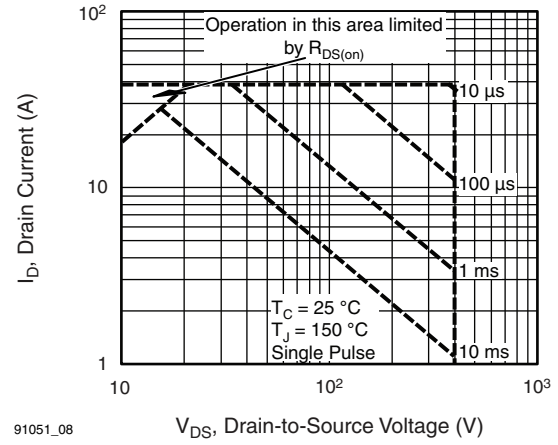
91051\_05 **Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



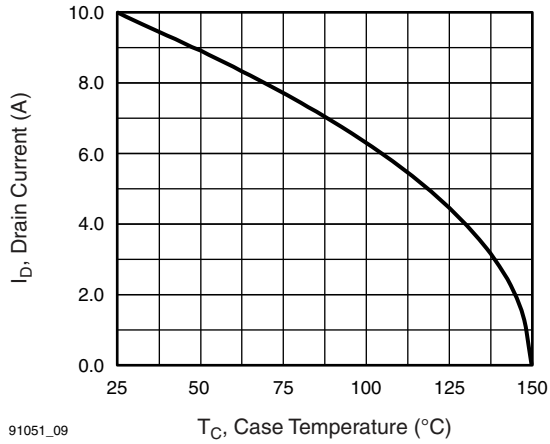
91051\_07 **Fig. 7 - Typical Source-Drain Diode Forward Voltage**



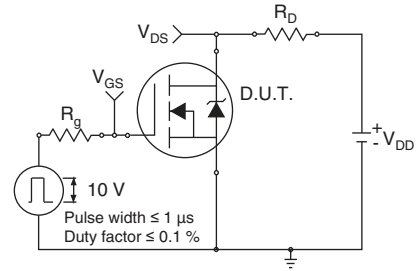
91051\_06 **Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



91051\_08 **Fig. 8 - Maximum Safe Operating Area**



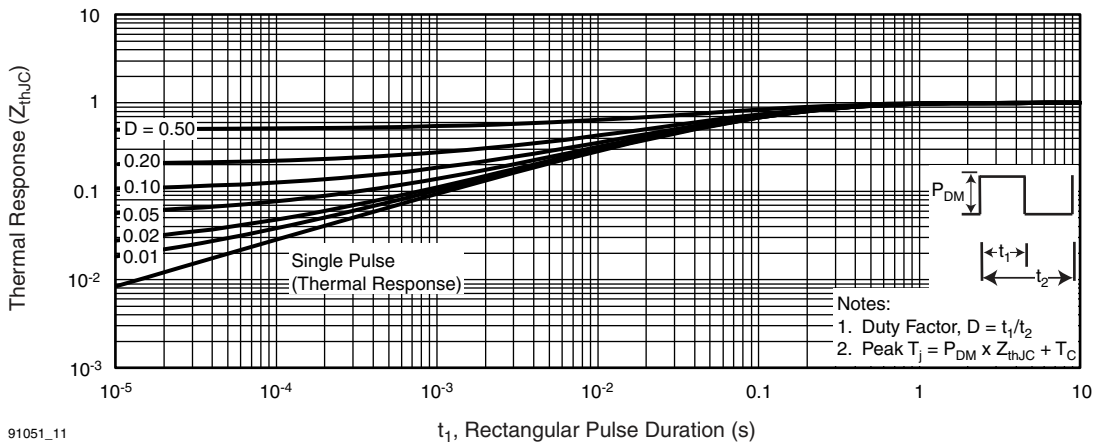
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



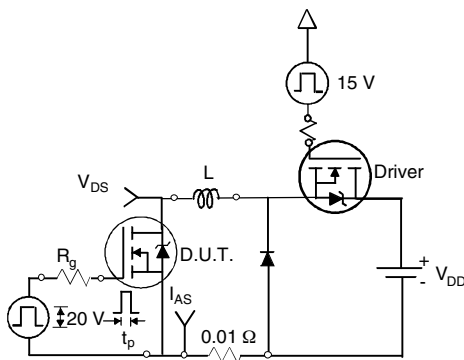
**Fig. 10a - Switching Time Test Circuit**



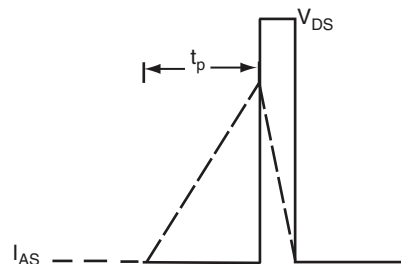
**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



**Fig. 12a - Unclamped Inductive Test Circuit**



**Fig. 12b - Unclamped Inductive Waveforms**

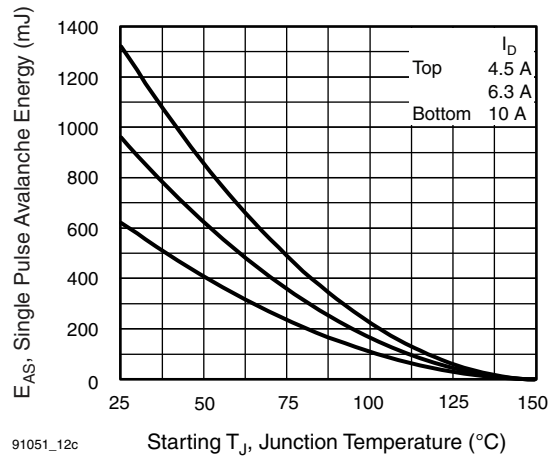


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

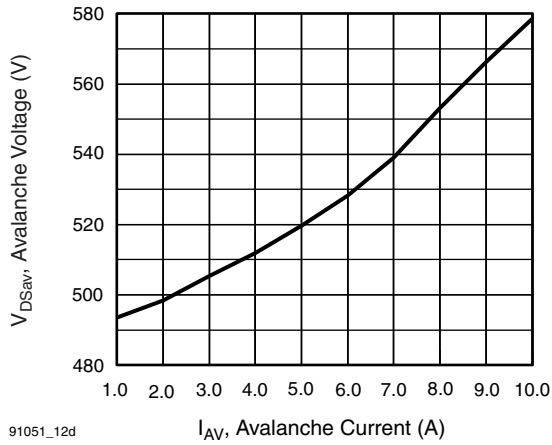
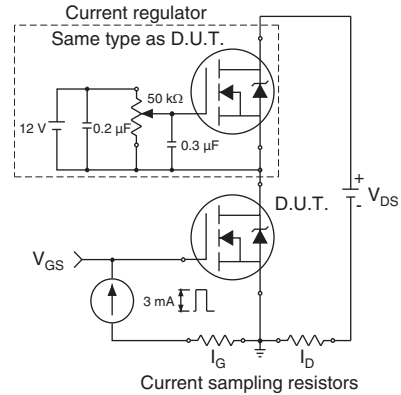
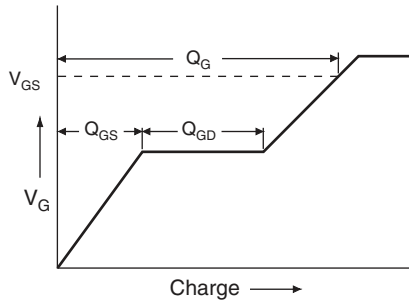
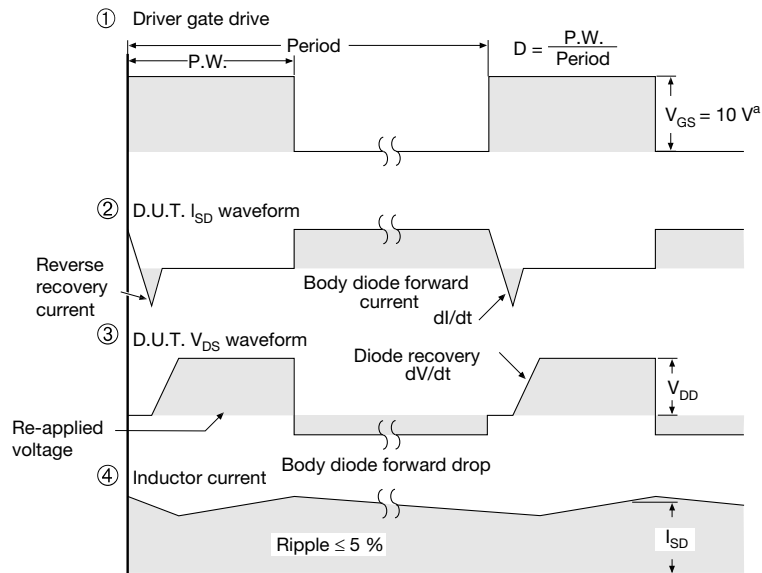
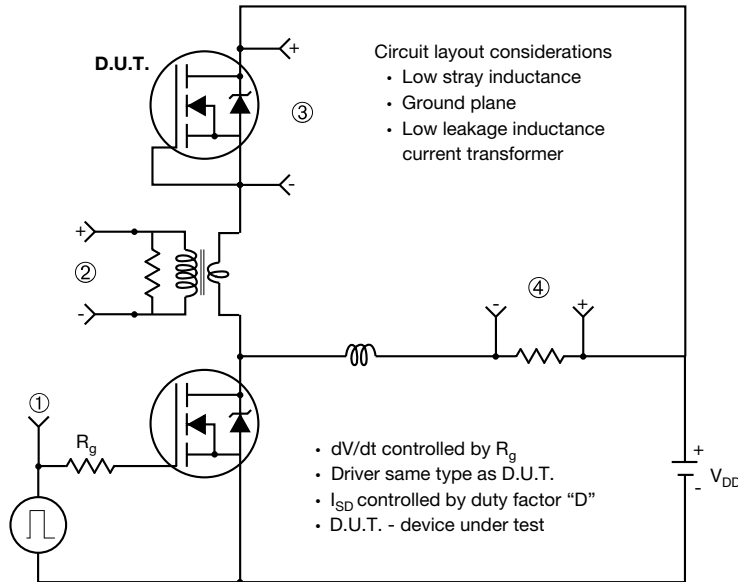


Fig. 12d - Typical Drain-to-Source Voltage Vs. Avalanche Current

**Peak Diode Recovery dV/dt Test Circuit**



**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

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