NIPPON PRECISION CIRCUITS INC.

ΣDECO SM588× series

Audio 3rd-order ΣΔ D/A Converter

OVERVIEW

The ΣDECO SM588× series, fabricated using NPC's Molybdenum-gate CMOS process, are D/A converter ICs for digital audio, that provide all the basic converter functions in miniature 8-pin packages. They each feature built-in 8-times oversampling digital filter, ΣΔ jitter-compensated D/A converter, and post-analog lowpass filter converter stages required for digital audio. They can sample at up to 96kHz for 16 or 24-bit input word length. A type with built-in deemphasis filter is also available for applications requiring deemphasis.

FEATURES

3-wire Input

- 2-channel stereo configuration
- 256fs, 384fs, or 512fs system clock (applied by product / version)
- Input format
  3-wire serial, MSB first, rear-packed
  16 or 24-bit (applied by product / version)
- 8-times oversampling digital filter
  - 32 dB stopband attenuation
  - ±0.05 dB passband ripple
- ΣΔ 2-channel D/A converter
  - 3rd-order noise shaper
  - Oversampling operation
- 3rd-order post-analog lowpass filter
- 4.5 to 5.5 V supply voltage
- 8-pin SOP
- Molybdenum-gate CMOS process

2-wire Input with Deemphasis Filter

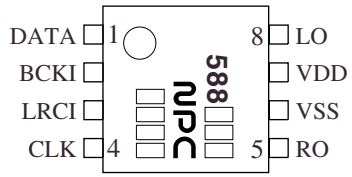
- 2-channel stereo configuration
- 256fs, 384fs, or 512fs system clock (applied by product / version)
- Input format
  2-wire serial, MSB first, rear-packed
  16 or 24-bit (applied by product / version)
- Deemphasis filter (fs = 44.1 kHz sample rate)
- 8-times oversampling digital filter
  - 32 dB stopband attenuation
  - ±0.05 dB passband ripple
- ΣΔ 2-channel D/A converter
  - 3rd-order noise shaper
  - Oversampling operation
- 3rd-order post-analog lowpass filter
- 4.5 to 5.5 V supply voltage
- 8-pin SOP
- Molybdenum-gate CMOS process

APPLICATIONS

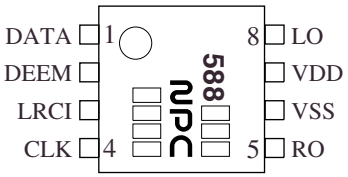
- Audio equipment

PINOUTS

3-wire input



2-wire input with built-in deemphasis filter



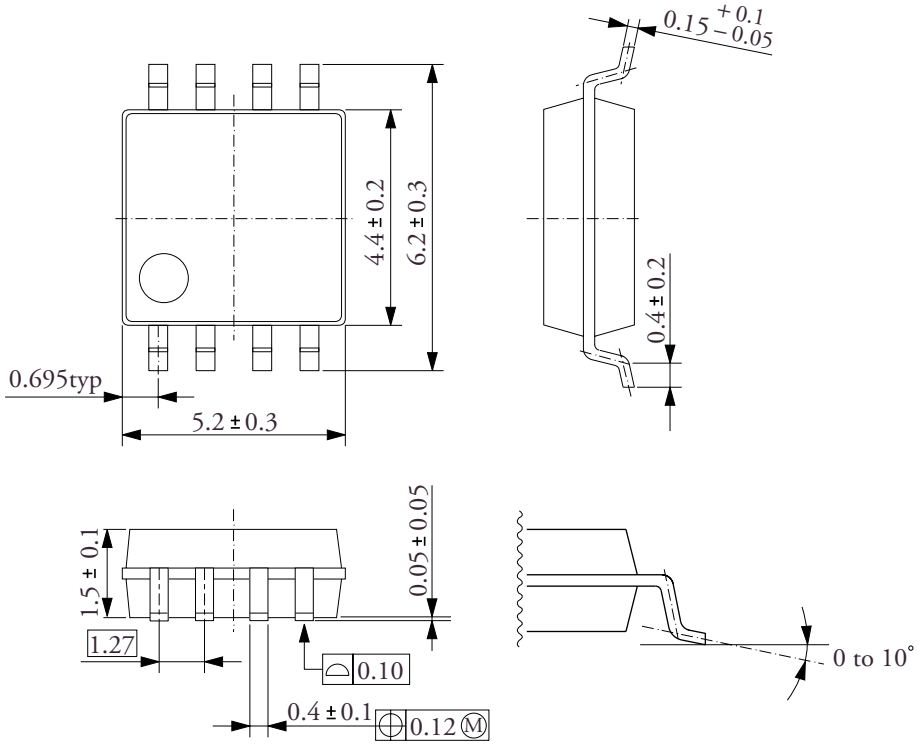
ORDERING INFORMATION

Device	Package
SM5882AS	8-pin SOP
SM5883AS	
SM5883BS	
SM5885CS	

PACKAGE DIMENSIONS

(Unit : mm)

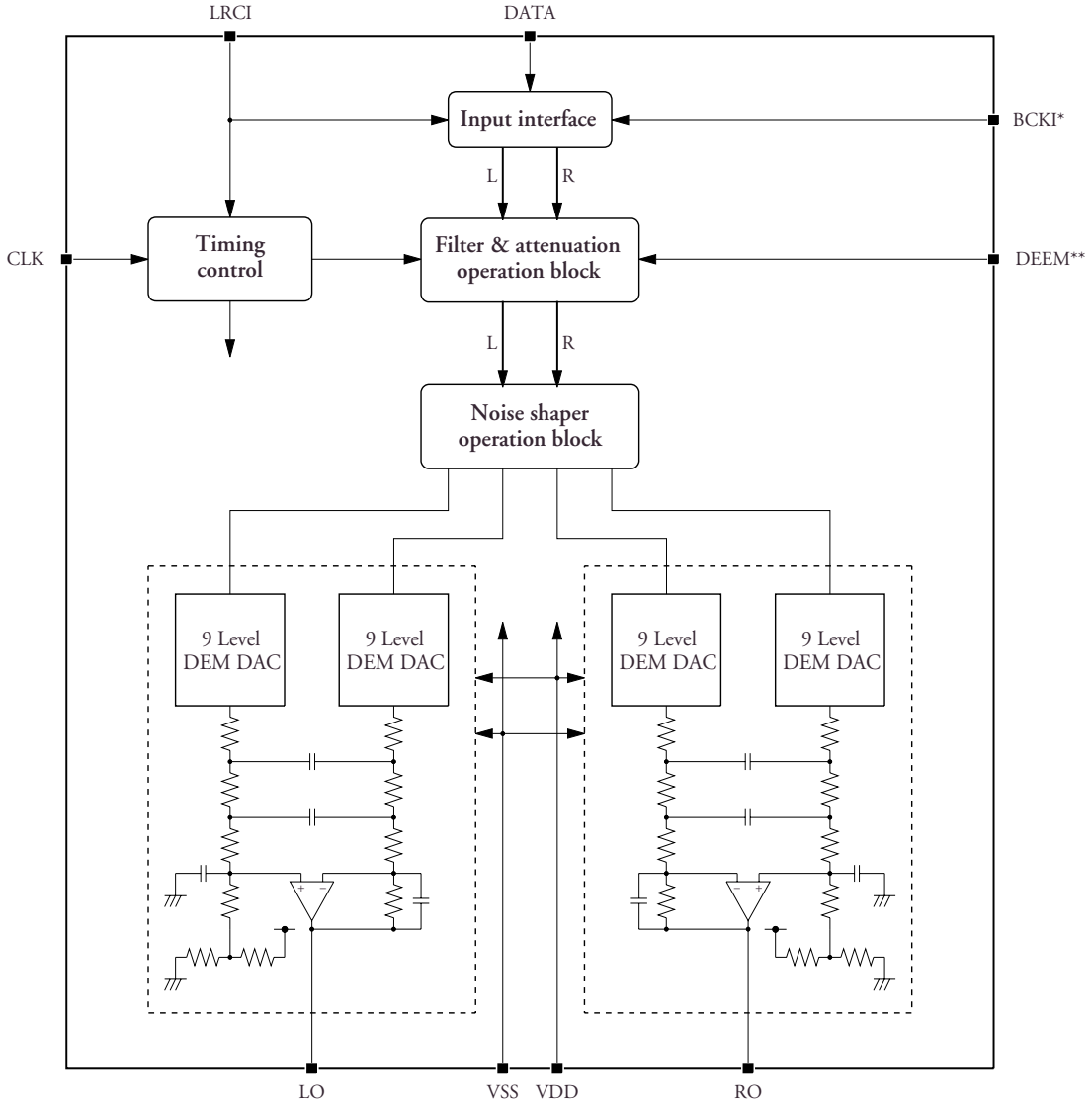
Weight : 0.07g



SERIES LINEUP

Device	Input length	Type	Pin 2 function	Master clock
SM5882AS	16	2-wire input	Deemphasis control	384fs
SM5883AS	16	3-wire input	Bit clock input	384fs
SM5883BS	16	3-wire input	Bit clock input	256fs
SM5885CS	24	3-wire input	Bit clock input	512fs

BLOCK DIAGRAM



* : Not available for 2-wire input type
** : Not available for 3-wire input type

PIN DESCRIPTION

Number	Name	I/O	Description
1	DATA	I	Serial data input
2	BCKI[1]	I	Bit clock input
	DEEM[2]	I	Deemphasis ON/OFF control (44.1 kHz, ON when HIGH)
3	LRCI	I	Sample rate (fs) clock input. Left-channel input when HIGH, and right-channel input when LOW.
4	CLK	I	External clock input
5	RO	O	Right-channel analog output
6	VSS	–	Ground
7	VDD	–	Supply
8	LO	O	Left-channel analog output

1. 3-wire type
2. 2-wire type with built-in deemphasis filter

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range[1]	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{STG}	–55 to 125	°C
Power dissipation	P_D	300	mW

1. All inputs
Also applicable during supply switching.

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	4.5 to 5.5	V
Operating temperature	T_{OPR}	–40 to 85	°C

DC Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption[1]	I_{DD}		–	12.5	25.0	mA
CLK HIGH-level input voltage	V_{IH1}	Clock input	0.7V_{DD}	–	–	V
CLK LOW-level input voltage	V_{IL1}	Clock input	–	–	0.3V_{DD}	V
CLK AC-coupled input voltage	V_{INAC}		0.7	–	–	V_{p-p}
HIGH-level input voltage[2]	V_{IH2}		0.5V_{DD}	–	–	V
LOW-level input voltage[2]	V_{IL2}		–	–	0.2V_{DD}	V
CLK HIGH-level input current	I_{IH}	V_{IN} = V_{DD}	20	62	170	µA
CLK LOW-level input current	I_{IL}	V_{IN} = 0 V	20	62	170	µA
Input leakage current[2]	I_{LH}	V_{IN} = V_{DD}	–	–	1.0	µA
	I_{LL}	V_{IN} = 0 V	–	–	1.0	µA

1. V_{DD} = 5 V, CLK clock input frequency f_{CLK} = 16.9344 MHz (384fs type)/11.2896 MHz (256fs type)/22.5792MHz (512fs type), no output load. Input data: NPC pattern.
2. Pins BCKI (3-wire type), DEEM (2-wire type with deemphasis filter), DATA, LRCI

AC Digital Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C

System clock (CLK)

256fs type

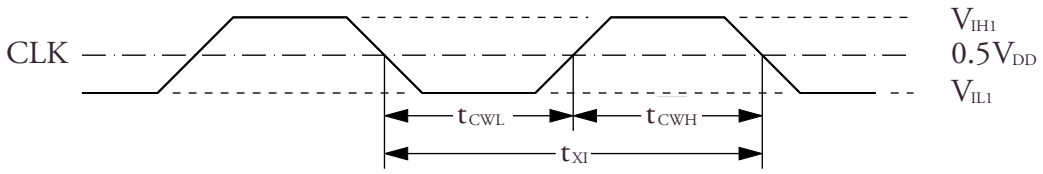
Parameter	Symbol	Rating			Unit
		min	typ	max	
HIGH-level clock pulsewidth	t_{CWH}	20.0	–	125	ns
LOW-level clock pulsewidth	t_{CWL}	20.0	–	125	ns
Clock pulse cycle	t_{XI}	40.0	–	250	ns

384fs type

Parameter	Symbol	Rating			Unit
		min	typ	max	
HIGH-level clock pulsewidth	t_{CWH}	13.15	–	125	ns
LOW-level clock pulsewidth	t_{CWL}	13.15	–	125	ns
Clock pulse cycle	t_{XI}	26.3	–	250	ns

512fs type

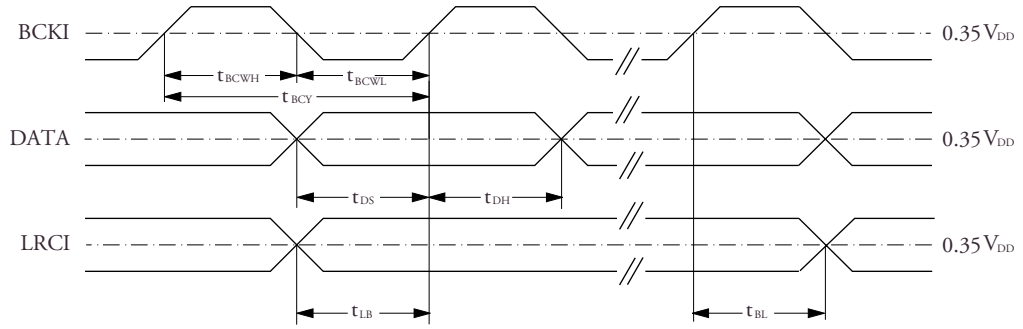
Parameter	Symbol	Rating			Unit
		min	typ	max	
HIGH-level clock pulsewidth	t_{CWH}	10	–	125	ns
LOW-level clock pulsewidth	t_{CWL}	10	–	125	ns
Clock pulse cycle	t_{XI}	20	–	250	ns



Serial inputs

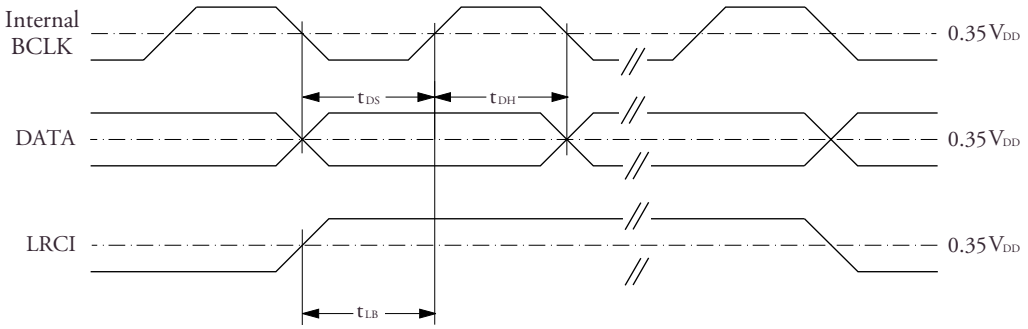
3-wire type (BCKI, DATA, LRCI)

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	50.0	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL}	50.0	–	–	ns
BCKI pulse cycle	t_{BCY}	1/(64fs)	–	–	ns
DATA setup time	t_{DS}	50.0	–	–	ns
DATA hold time	t_{DH}	50.0	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB}	50.0	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BL}	50.0	–	–	ns



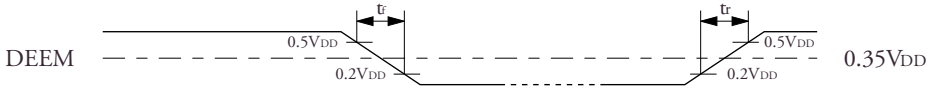
2-wire type (DATA, LRCI)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DATA setup time	t_{DS}		50	–	–	ns
DATA hold time	t_{DH}		50	–	–	ns
LRCI edge to internal BCLK rising edge	t_{LB}	256fs/512fs	$1.5t_{XI}$	–	$2.5t_{XI}$	ns
		384fs	$3.5t_{XI}$	–	$4.5t_{XI}$	ns



Control input (DEEM: 2-wire type)

Parameter	Symbol	Rating			Unit
		min	typ	max	
Rise time	t_r	–	–	50	ns
Fall time	t_f	–	–	50	ns



AC Analog Characteristics

256fs type specification (SM5883BS) : V_{SS} = 0 V, V_{DD} = 5 V, 16-bit input type, crystal oscillator frequency f_{OSC} = 11.2896 MHz, Ta = 25 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion	THD + N	1 kHz, 0 dB	–	0.0035	0.0130	%
LSI output level	V_{OUT1}	1 kHz, 0 dB	–	1.09	–	V_{rms}
Evaluation board output level	V_{OUT2}	1 kHz, 0 dB	–	1.33	–	V_{rms}
Dynamic range	D.R	1 kHz, –60 dB	90.4	96.4	–	dB
Signal-to-noise ratio	S/N	1 kHz, 0dB/ –∞	92.8	98.8	–	dB
Channel separation	Ch. Sep	1 kHz, –∞ –0dB	87.5	93.5	–	dB

Note: These parameters are measured using the measurement block diagram (page 8) and the measurement circuit (page 9).

384fs type specification (SM5882AS, SM5883AS) : V_{SS} = 0 V, V_{DD} = 5 V, DEEM = 0 V (2-wire type), 16-bit input type, crystal oscillator frequency f_{OSC} = 16.9344 MHz, Ta = 25 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion	THD + N	1 kHz, 0 dB	–	0.003	0.0120	%
LSI output level	V_{OUT1}	1 kHz, 0 dB	–	1.09	–	V_{rms}
Evaluation board output level	V_{OUT2}	1 kHz, 0 dB	–	1.33	–	V_{rms}
Dynamic range	D.R	1 kHz, –60 dB	90.4	96.4	–	dB
Signal-to-noise ratio	S/N	1 kHz, 0dB/ –∞	93.0	99.0	–	dB
Channel separation	Ch. Sep	1 kHz, –∞ –0dB	88.5	94.5	–	dB

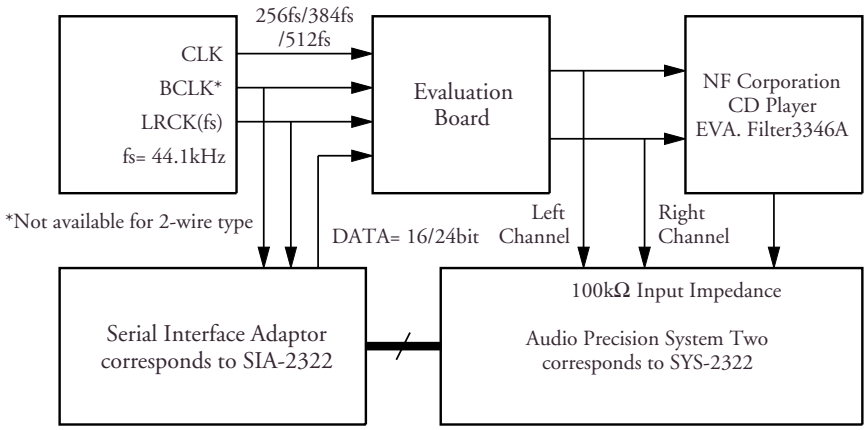
Note: These parameters are measured using the measurement block diagram (page 8) and the measurement circuit (page 9).

512fs type specification (SM5885CS) : V_{SS} = 0 V, V_{DD} = 5 V, 24-bit input type, crystal oscillator frequency f_{OSC} = 22.5792MHz, Ta = 25 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion	THD + N	1 kHz, 0 dB	–	0.0035	0.0130	%
LSI output level	V_{OUT1}	1 kHz, 0 dB	–	1.09	–	V_{rms}
Evaluation board output level	V_{OUT2}	1 kHz, 0 dB	–	1.33	–	V_{rms}
Dynamic range	D.R	1 kHz, –60 dB	92.0	98.0	–	dB
Signal-to-noise ratio	S/N	1 kHz, 0dB/ –∞	92.8	98.8	–	dB
Channel separation	Ch. Sep	1 kHz, –∞ –0dB	87.5	93.5	–	dB

Note: These parameters are measured using the measurement block diagram (page 8) and the measurement circuit (page 9).

AC analog measurement block diagram

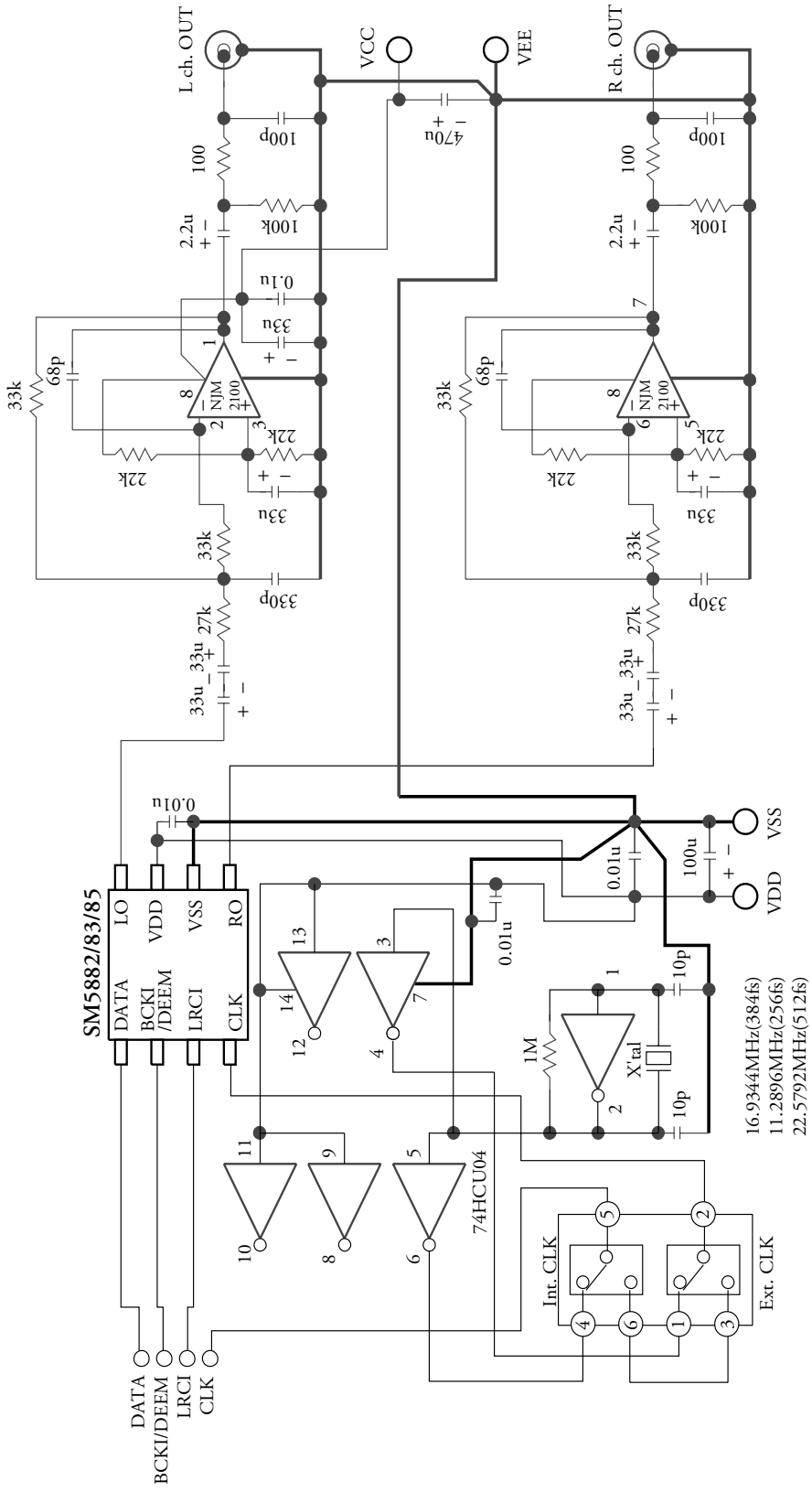


AC analog measurement conditions

Parameter[1]	Symbol	3346A left/right-channel selector switch	Audio Precision System Two audio analyzer with built-in filter
Total harmonic distortion	THD + N	Not used	20 kHz lowpass filter
Output level	V_{OUT}		
Dynamic range	D.R	D-RANGE	
Signal-to-noise ratio	S/N	Not used	22 kHz lowpass filter A-WTD
Channel separation	Ch. Sep	Not used	20 kHz lowpass filter

1. Pins LO and RO should have an output load of 10 kΩ (min).

AC analog measurement circuit

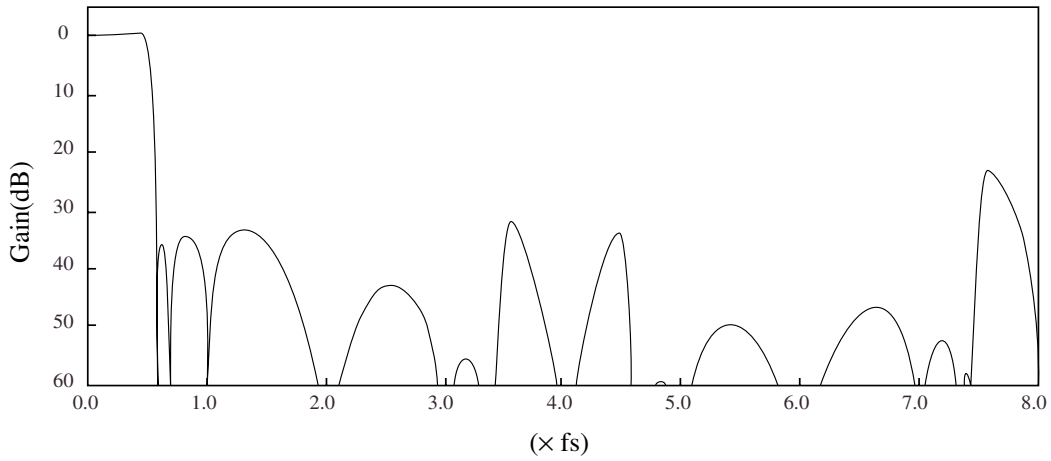


Theoretical Filter Characteristics

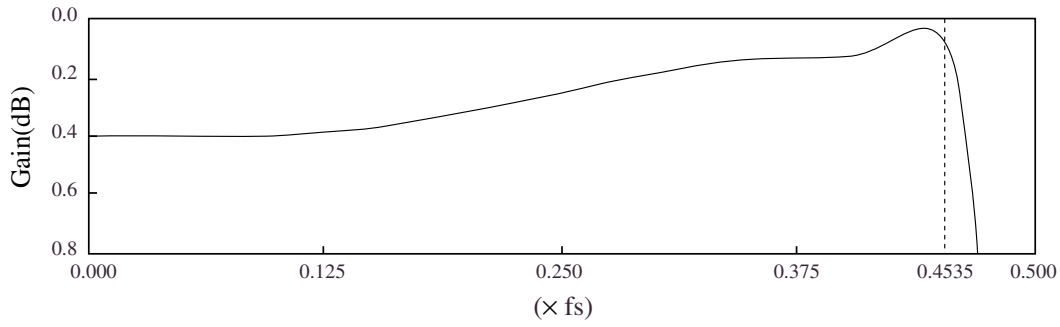
Overall characteristics

Parameter	Frequency band		Attenuation (dB)		
	f	@ fs = 44.1 kHz	min	typ	max
Passband ripple	0 to 0.4535fs	0 to 20.0 kHz	–0.05	–	+0.05
Stopband attenuation	0.5465fs to 7.4535fs	24.1 to 328.7 kHz	32	–	–
Built-in analog LPF compensation	0.4535fs	20.0 kHz	–	–0.34	–

Overall frequency characteristic



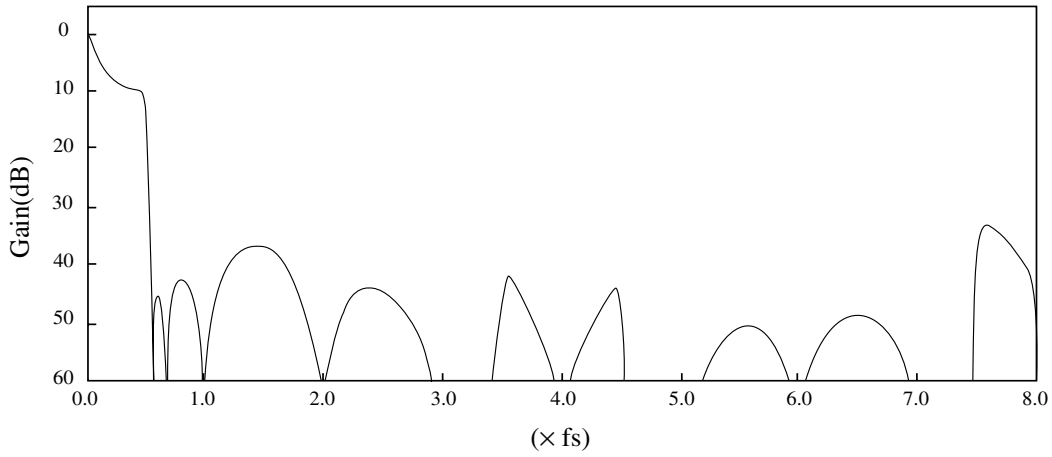
Passband characteristic



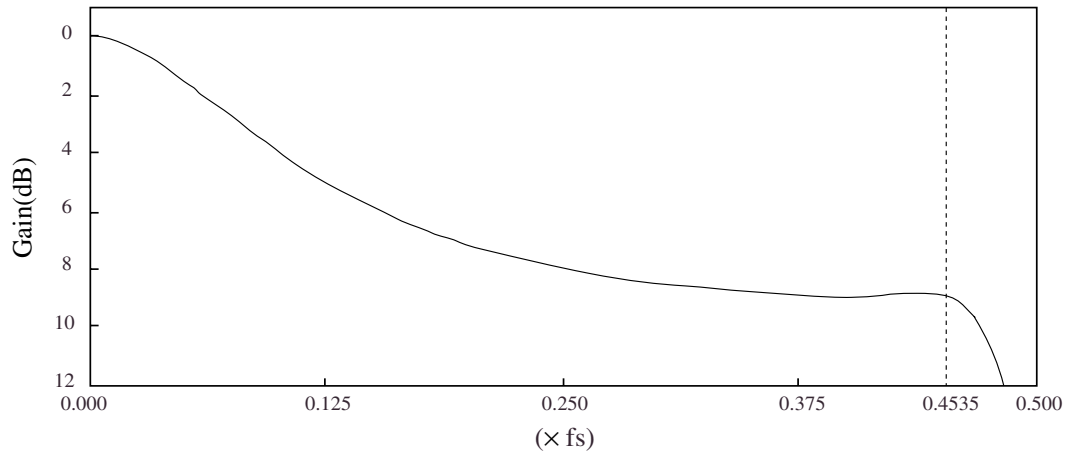
2-wire input, deemphasis ON overall characteristics

Parameter	Frequency band		Attenuation (dB)		
	f	@ fs = 44.1 kHz	min	typ	max
Passband ripple	0 to 0.4535fs	0 to 20.0 kHz	–0.09	–	+0.23
Stopband attenuation	0.5465fs to 7.4535fs	24.1 to 328.7 kHz	36	–	–
Built-in analog LPF compensation	0.4535fs	20.0 kHz	–	–0.34	–

Deemphasis ON overall frequency characteristic



Deemphasis ON passband characteristic



FUNCTIONAL DESCRIPTION

System Clock (CLK)

The system clock CLK frequency varies with device within the series as shown below, where fs is the input frequency on LRCI.

Note that the input clock accuracy and signal-to-noise ratio greatly influence the AC analog characteristics.

The D/A converter operates at the speed shown in the following table.

Table 1. System clock

Device	Master clock	DAC oversampling operation
A version	384fs	48fs
B, C version	256/512fs	32fs

System Reset

The SM588× series devices incorporate a built-in power-ON reset circuit for system reset.

When power is applied, the internal arithmetic operation and output timing counter are reset, and then reset again and timing synchronized to the external input on the next LRCI rising edge. After system reset, the outputs are muted until the 9th rising of LRCI when output muting is released.

When the timing is reset, the PWM outputs may generate an output noise. An external muting circuit may be required to prevent this output noise.

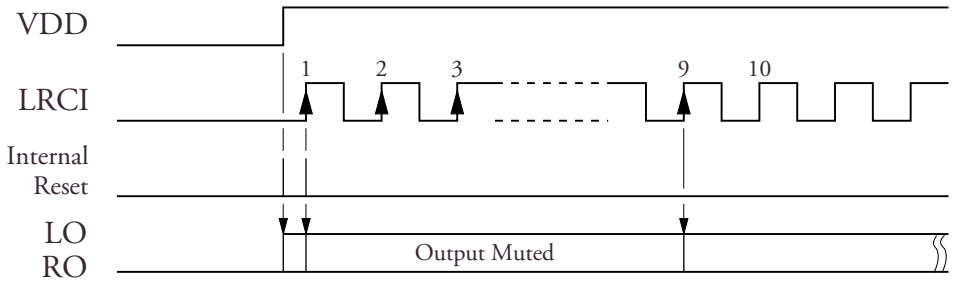


Figure 1. System reset timing

Audio Data Input

Input data format (DATA)

The input data has a format that varies with device within the series, as shown below.

Table 2. Input format

Device	Input length	Format
SM5882/SM5883[1]	16 bits	MSB first, bit serial, rear-packed, 2s complement
SM5885[2]	24 bits	

1. The 2-wire type supports bit clocks of 48fs (384fs) or 64fs (256fs/512fs) only.
2. The 3-wire type supports bit clocks of up to 64fs.

Input timing

3-wire input (DATA, LRCI, BCKI)

Serial data bits on DATA are read into the SIPO register (serial-to-parallel converter register) on the rising edge of the bit clock BCKI, and then converted to parallel data.

The arithmetic operation and output timing are independent of the input timing. Accordingly, after a reset, as long as the clock frequency ratio between LRCI and the system clock CLK is maintained, phase differences between LRCI, BCKI and the system clock CLK do not affect the functional operation. Also, any jitter present on the data input clock does not appear as output pulse jitter.

2-wire input (DATA, LRCI)

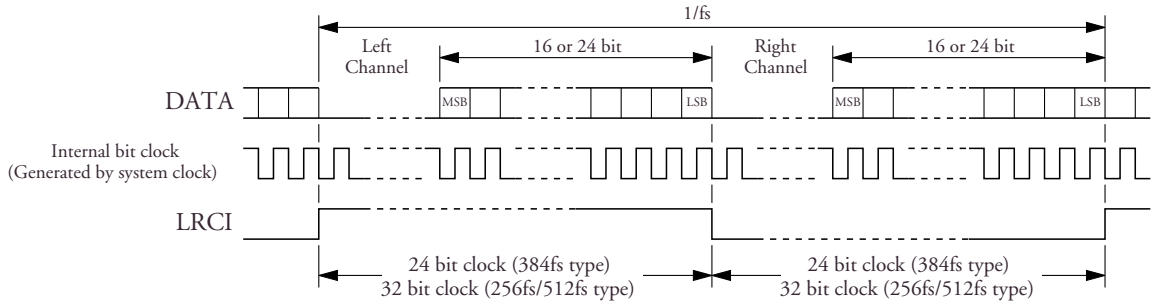
Serial data bits on DATA are read into the SIPO register (serial-to-parallel converter register) on the rising edge of an internally generated bit clock, and then converted to parallel data.

Deemphasis Filter (DEEM: 2-wire input)

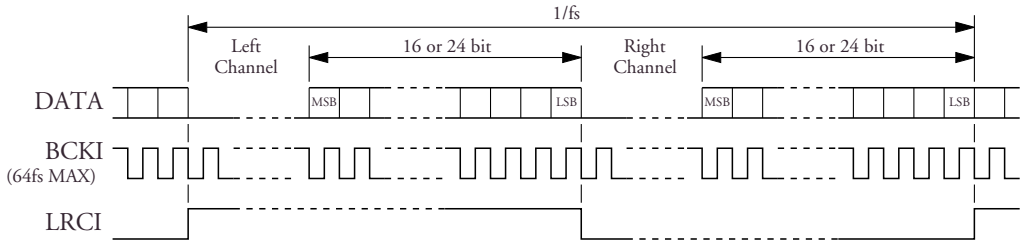
The 2-wire type with built-in digital deemphasis filter is designed to operate at 44.1 kHz. Deemphasis is ON when DEEM is HIGH, and OFF when DEEM is LOW.

TIMING DIAGRAMS

2-wire Input Type with Deemphasis Filter Built-in

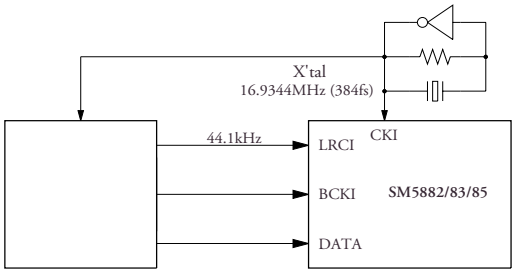


3-wire Input Type

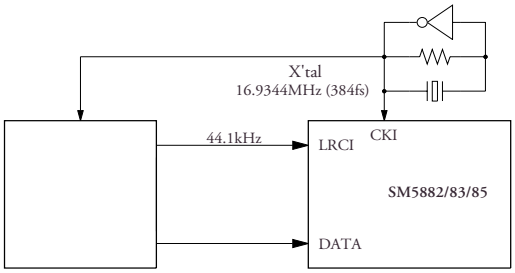


TYPICAL APPLICATIONS

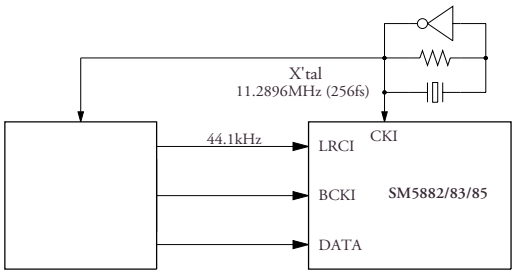
Input Interface Examples (fs = 44.1kHz)



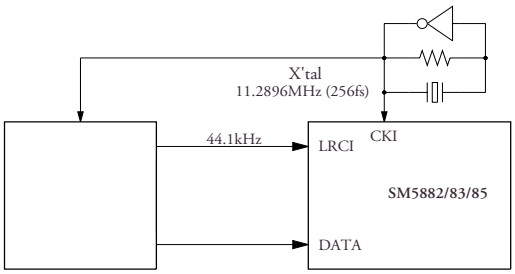
3-wire input type
System clock 384fs



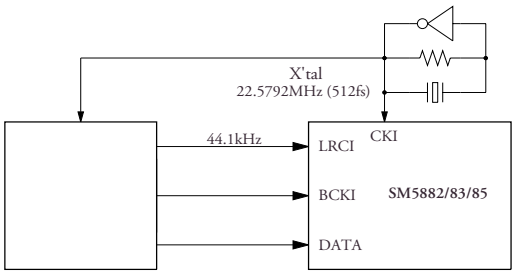
2-wire input type
System clock 384fs



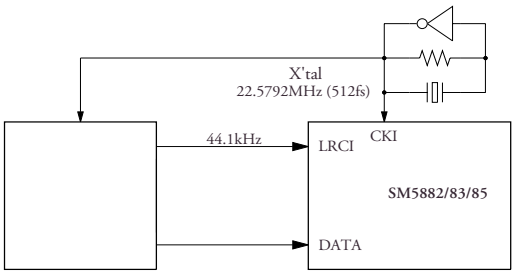
3-wire input type
System clock 256fs



2-wire input type
System clock 256fs



3-wire input type
System clock 512fs



2-wire input type
System clock 512fs

Note that the output analog characteristics and other specifications are not guaranteed for a particular format or application circuit.

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