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To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Renesas Technology Corp.

4280 Group

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SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER for INFRARED REMOTE CONTROL TRANSMITTERS

DESCRIPTION

The 4280 Group is a 4-bit single-chip microcomputer designed with CMOS technology for remote control transmitters. The 4280 Group has 7 carrier waves and enables fabrication of 8 × 7 key matrix.

FEATURES

- Number of basic instructions 62
- Minimum instruction execution time .... 8.0 µs
  (at f(X_{IN}) = 4.0 MHz, system clock = f(X_{IN})/8, V_{DD}=3.0 V)
- Supply voltage .... 1.8 V to 3.6 V
- Subroutine nesting .... 4 levels
- Timer
  Timer 1 .... 8-bit timer
  with a reload register and carrier wave output auto-control function
- Carrier wave output function (port CARR)
  f(X_{IN}), f(X_{IN})/4, f(X_{IN})/8, f(X_{IN})/12
  f(X_{IN})/64, f(X_{IN})/96, "H" output fixed
- Logic operation function (XOR, OR, AND)
- RAM back-up function
- Key-on wakeup function (ports D_7, E_0–E_2, G_0–G_3) 8
- I/O port (ports D, E, G, CARR) 16
- Oscillation circuit .... Ceramic resonance
- Watchdog timer
- Power-on reset circuit
- Voltage drop detection circuit .... Typical:1.50 V

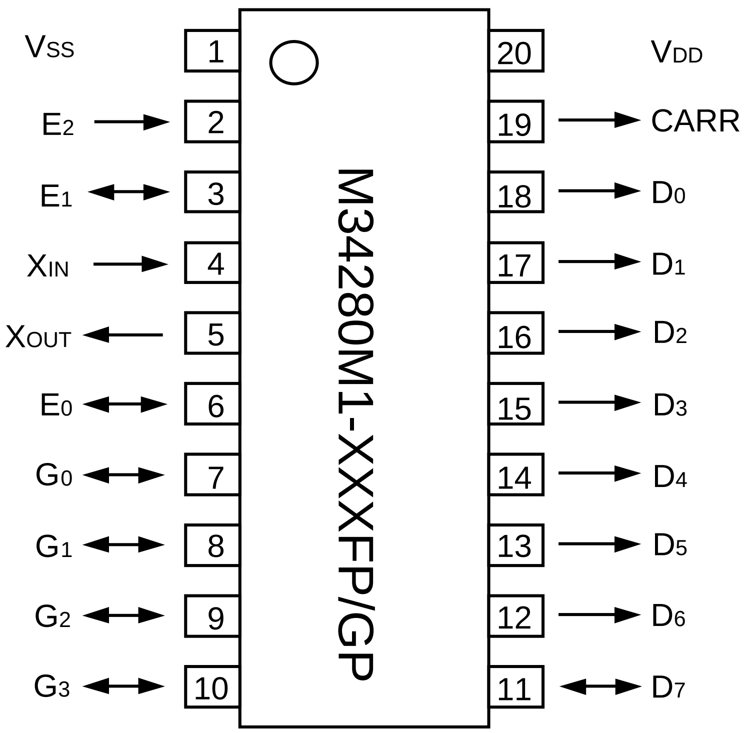
APPLICATION

Various remote control transmitters

Product	ROM (PROM) size (× 9 bits)	RAM size (× 4 bits)	Package	ROM type
M34280M1-XXXFP	1024 words	32 words	20P2N-A	Mask ROM
M34280M1-XXXGP	1024 words	32 words	20P2E/F-A	Mask ROM
M34280E1FP	1024 words	32 words	20P2N-A	One Time PROM
M34280E1GP	1024 words	32 words	20P2E/F-A	One Time PROM

PIN CONFIGURATION (TOP VIEW)

M34280M1-XXXFP/GP



Outline 20P2N-A
20P2E/F-A

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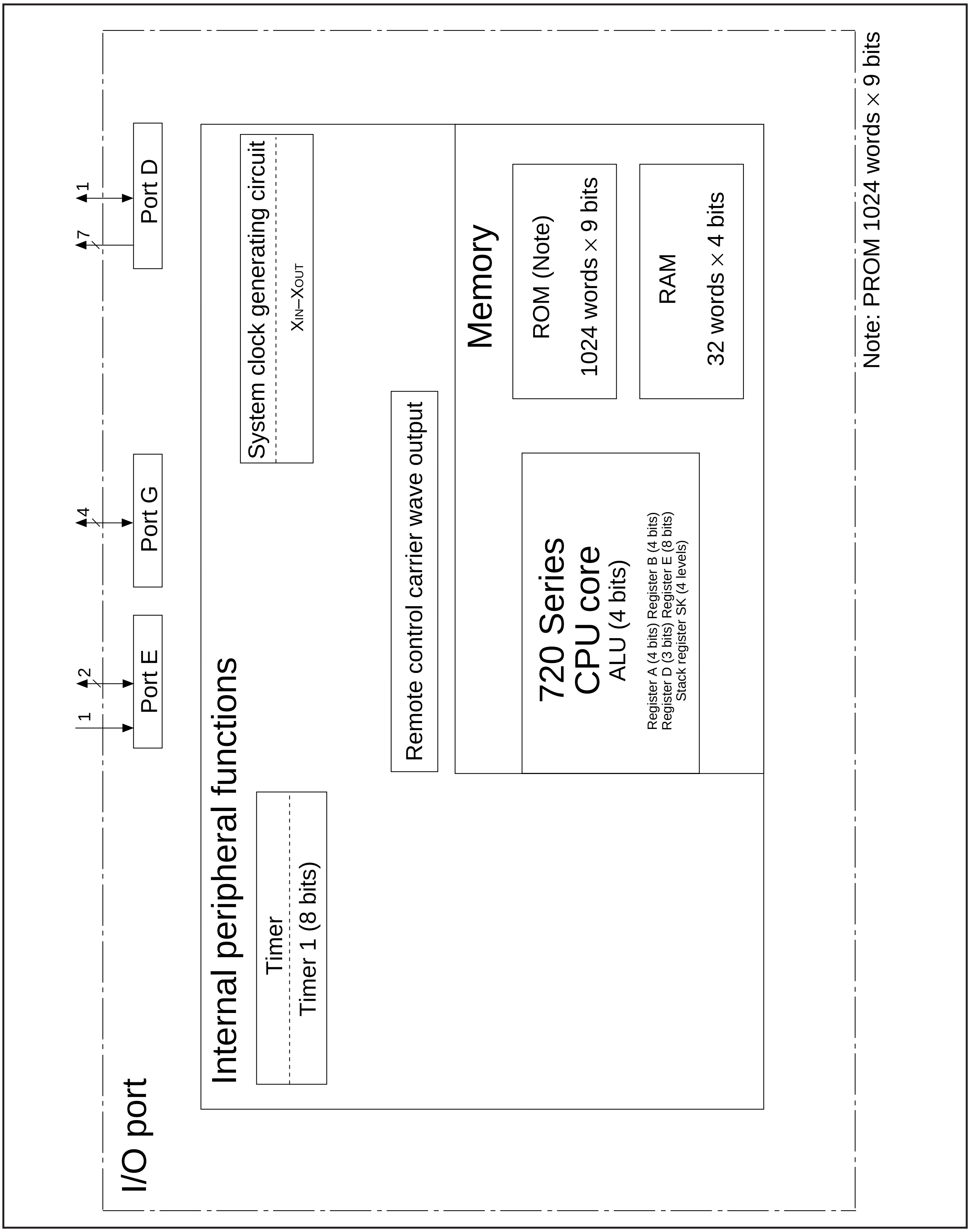
BLOCK DIAGRAM



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PERFORMANCE OVERVIEW

Parameter			Function
Number of basic instructions			62
Minimum instruction execution time			8.0 µs (at 4.0 MHz system clock frequency) (f(X_{IN}) = 4.0 MHz, system clock = f(X_{IN})/8, V_{DD} = 3 V)
Memory sizes	ROM	M34280M1/E1	1024 words × 9 bits
	RAM		32 words × 4 bits
Input/Output ports	D_0–D_6	Output	Seven independent output ports
	D_7	I/O	1-bit I/O port with the pull-down function
	E_0–E_2	Input	3-bit input port with the pull-down function
	E_0, E_1	Output	2-bit output port (E_0, E_1)
	G_0–G_3	I/O	4-bit I/O port with the pull-down function
	CARR	Output	1-bit output port; CMOS output
Timer 1			8-bit timer with a reload register
Subroutine nesting			4 levels (However, only 3 levels can be used when the TABP p instruction is executed)
Device structure			CMOS silicon gate
Package			20-pin plastic molded SOP (20P2N-A)/SSOP (20P2E/F-A)
Operating temperature range			–20 °C to 85 °C
Supply voltage			1.8 V to 3.6 V
Power dissipation (typical value)	Active mode		400 µA (f(X_{IN}) = 4.0 MHz, system clock = f(X_{IN})/8, V_{DD} = 3 V)
	RAM back-up mode		0.1 µA (at room temperature, V_{DD} = 3 V)

PIN DESCRIPTION

Pin	Name	Input/Output	Function
V_{DD}	Power supply	—	Connected to a plus power supply.
V_{SS}	Ground	—	Connected to a 0 V power supply.
X_{IN}	System clock input	Input	I/O pins of the system clock generating circuit. Connect a ceramic resonator between pins X_{IN} and X_{OUT}. The feedback resistor is built-in between pins X_{IN} and X_{OUT}.
X_{OUT}	System clock output	Output	
D_0–D_6	Output port D	Output	Each pin of port D has an independent 1-bit wide output function. The output structure is P-channel open-drain.
D_7	I/O port D	I/O	1-bit I/O port. For input use, turn on the built-in pull-down transistor and set the latch of the specified bit to “0.” In addition, key-on wakeup function using “H” level sense becomes valid. The output structure is P-channel open-drain.
E_0–E_2	I/O port E	Output	2-bit (E_0, E_1) output port. The output structure is P-channel open-drain.
		Input	3-bit input port. For input use (E_0, E_1), turn on the built-in pull-down transistor and set the latch of the specified bit to “0.” In addition, key-on wakeup function using “H” level sense becomes valid. Port E_2 has an input-only port and has a key-on wakeup function using “H” level sense and pull-down transistor.
G_0–G_3	I/O port G	I/O	4-bit I/O port. For input use, set the latch of the specified bit to “0.” The output structure is P-channel open-drain. Port G has a key-on wakeup function using “H” level sense and pull-down transistor.
CARR	Carrier wave output for remote control	Output	Carrier wave output pin for remote control. The output structure is CMOS circuit.

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CONNECTIONS OF UNUSED PINS

Pin	Connection
D_0–D_7	Open or connect to V_{DD} pin (Note 1).
E_0, E_1	Set the output latch to “1” and open, or connect to V_{DD} pin (Note 2).
E_2	Open or connect to V_{SS} pin.
G_0–G_3	Set the output latch to “0” and open, or connect to V_{SS} pin.

Notes 1: Port D_7: Set the bit 2 ($PU0_2$) of the pull-down control register PU0 to “0” by software and turn the pull-down transistor OFF.
2: Set the corresponding bits ($PU0_0$, $PU0_1$) of the pull-down control register PU0 to “0” by software and turn the pull-down transistor OFF.

(Note in order to set the output latch to “0” to make pins open)
- After system is released from reset, a port is in a high-impedance state until the output latch of the port is set to “0” by software. Accordingly, the voltage level of pins is undefined and the excess of the supply current may occur.
- To set the output latch periodically is recommended because the value of output latch may change by noise or a program run away (caused by noise).

(Note when connecting to V_{SS} and V_{DD})
- Connect the unused pins to V_{SS} or V_{DD} at the shortest distance and use the thick wire against noise.

PORT FUNCTION

Port	Pin	Input/ Output	Output structure	Control bits	Control instructions	Control registers	Remark
Port D	D_0–D_6	Output (7)	P-channel open-drain	1 bit	SD RD CLD		
	D_7	I/O (1)			SD RD CLD SZD	PU0	Pull-down function and key-on wakeup function (programmable)
Port E	E_0 E_1	I/O (2)	P-channel open-drain	Output: 2 bits Input: 3 bits	OEA IAE	PU0	Pull-down function and key-on wakeup function (programmable)
	E_2	Input (1)			IAE		
Port G	G_0–G_3	I/O (4)	P-channel open-drain	4 bits	OGA IAG		Pull-down function and key-on wakeup function
Port CARR	CARR	Output (1)	CMOS	1 bit	OCRA	C	

DEFINITION OF CLOCK AND CYCLE

- System clock (STCK)
  The system clock is the source clock for controlling this product. It can be selected as shown below whether to use the CCK instruction.

CCK instruction	System clock	Instruction clock
When not using	$f(X_{IN})/8$	$f(X_{IN})/32$
When using	$f(X_{IN})$	$f(X_{IN})/4$

- Instruction clock (INSTCK)
  The instruction clock is a signal derived by dividing the system clock by 4, and is the basic clock for controlling CPU. The one instruction clock cycle is equivalent to one machine cycle.

- Machine cycle
  The machine cycle is the cycle required to execute the instruction.

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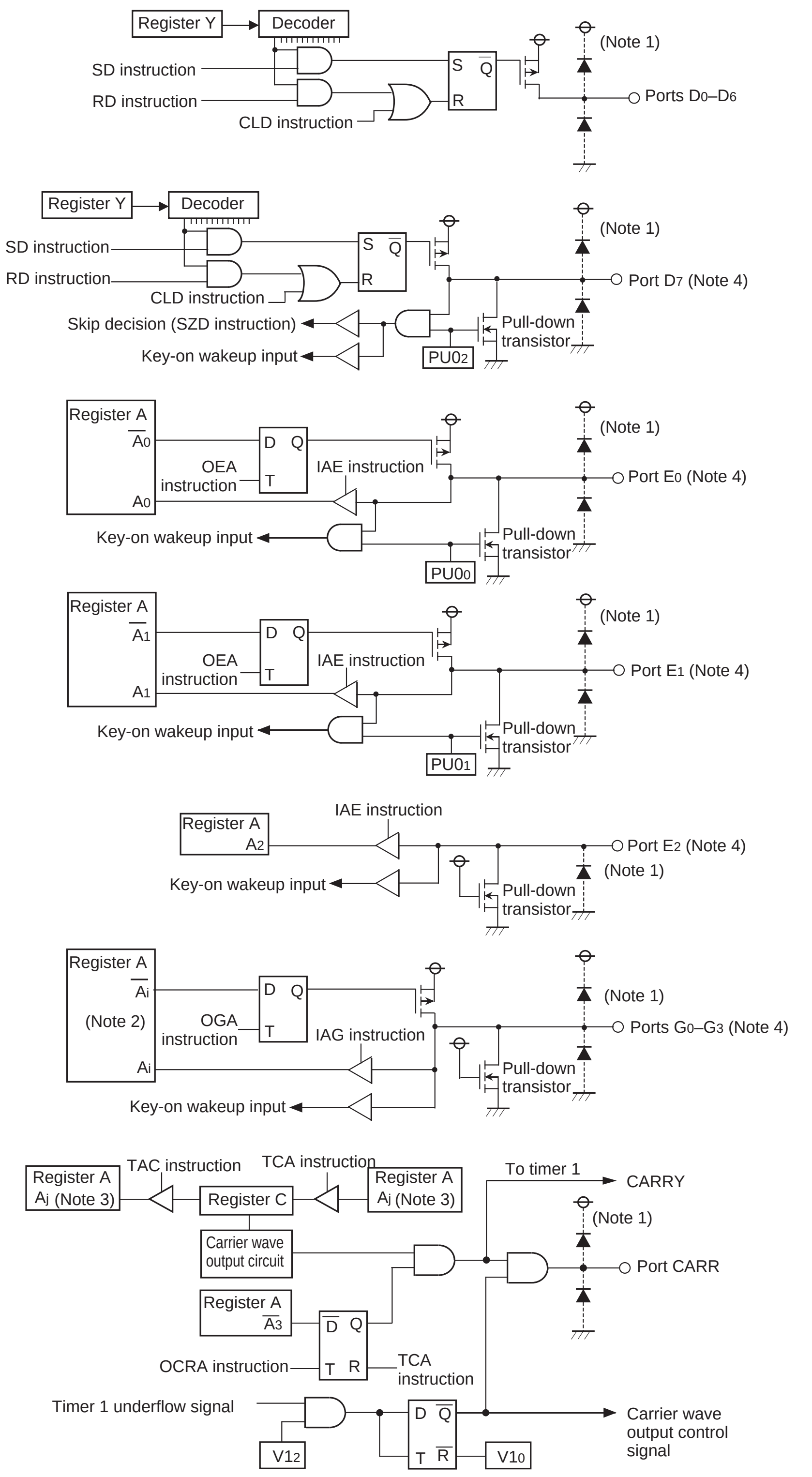
PORT BLOCK DIAGRAMS



Notes 1: ----▶|---- This symbol represents a parasitic diode.
2: i represents bits 0 to 3.
3: j represents bits 0 to 2.
4: Applied voltage must be less than V_{DD}.

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FUNCTION BLOCK OPERATIONS
CPU

(1) Arithmetic logic unit (ALU)

The arithmetic logic unit ALU performs 4-bit arithmetic such as 4-bit data addition, comparison, and bit manipulation.

(2) Register A and carry flag

Register A is a 4-bit register used for arithmetic, transfer, exchange, and I/O operation.

Carry flag CY is a 1-bit flag that is set to “1” when there is a carry with the AMC instruction (Figure 1).

It is unchanged with both A n instruction and AM instruction.

The value of A_0 is stored in carry flag CY with the RAR instruction (Figure 2).

Carry flag CY can be set to “1” with the SC instruction and cleared to “0” with the RC instruction.

(3) Registers B and E

Register B is a 4-bit register used for temporary storage of 4-bit data, and for 8-bit data transfer together with register A.

Register E is an 8-bit register. It can be used for 8-bit data transfer with register B used as the high-order 4 bits and register A as the low-order 4 bits (Figure 3).

(4) Register D

Register D is a 3-bit register.

It is used to store a 7-bit ROM address together with register A and is used as a pointer within the specified page when the TABP p, BLA p, or BMLA p instruction is executed (Figure 4).

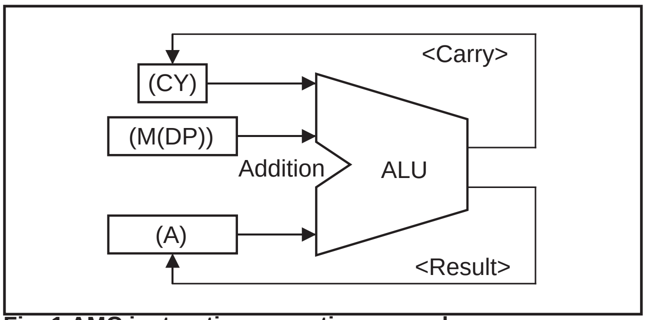

Fig. 1 AMC instruction execution example

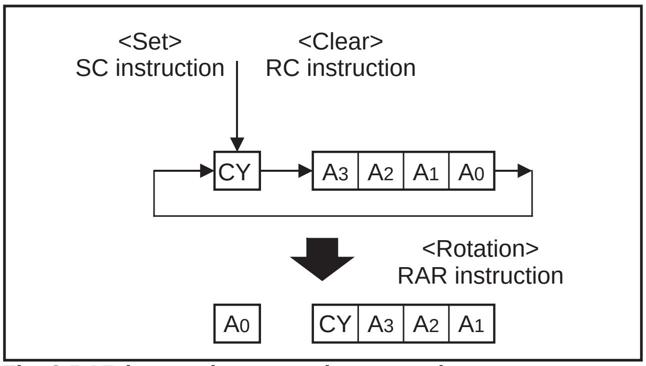

Fig. 2 RAR instruction execution example

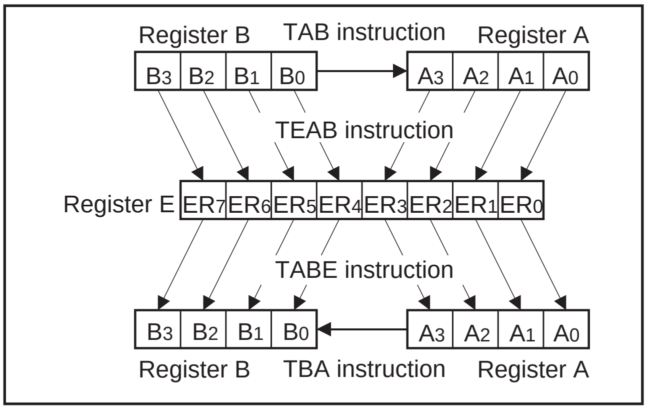

Fig. 3 Registers A, B and register E

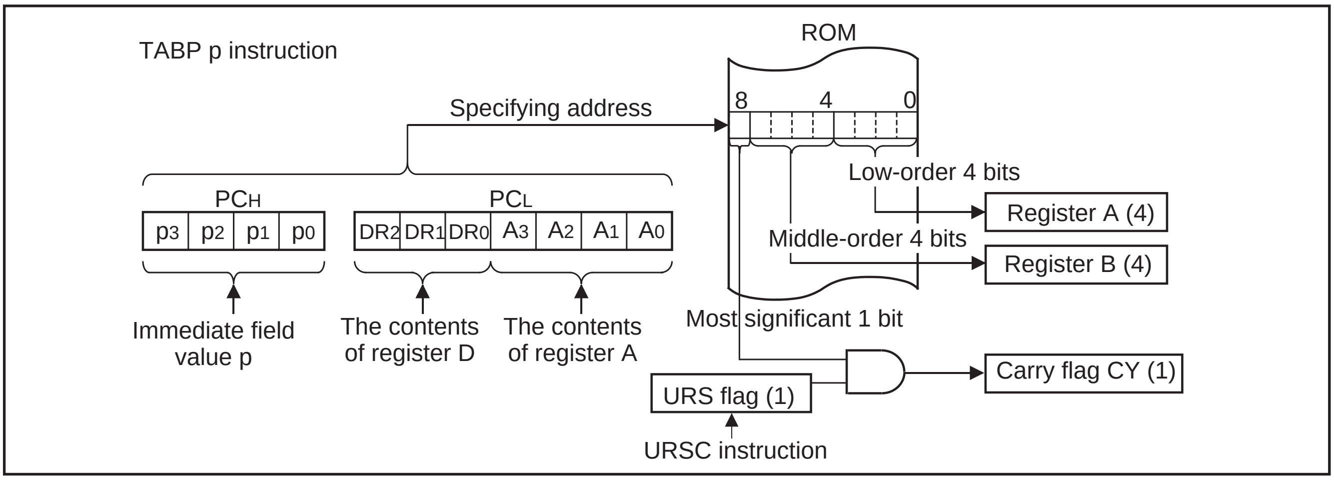

Fig. 4 TABP p instruction execution example

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(5) Most significant ROM code reference enable flag (URS)

URS flag controls whether to refer to the contents of the most significant 1 bit (bit 8) of ROM code when executing the TABP p instruction. If URS flag is "0," the contents of the most significant 1 bit of ROM code is not referred even when executing the TABP p instruction. However, if URS flag is "1," the contents of the most significant 1 bit of ROM code is set to flag CY when executing the TABP p instruction (Figure 4).

URS flag is "0" after system is released from reset and returned from RAM back-up mode. It can be set to "1" with the URSC instruction, but cannot be cleared to "0."

(6) Stack registers (SKs) and stack pointer (SP)

Stack registers (SKs) are used to temporarily store the contents of program counter (PC) just before branching until returning to the original routine when;

• performing a subroutine call, or
• executing the table reference instruction (TABP p).

Stack registers (SKs) are four identical registers, so that subroutines can be nested up to 4 levels. However, one of stack registers is used when executing a table reference instruction. Accordingly, be careful not to over the stack. The contents of registers SKs are destroyed when 4 levels are exceeded.

The register SK nesting level is pointed automatically by 2-bit stack pointer (SP).

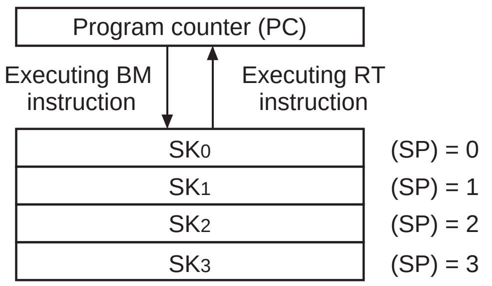
Figure 5 shows the stack registers (SKs) structure.

Figure 6 shows the example of operation at subroutine call.

(7) Skip flag

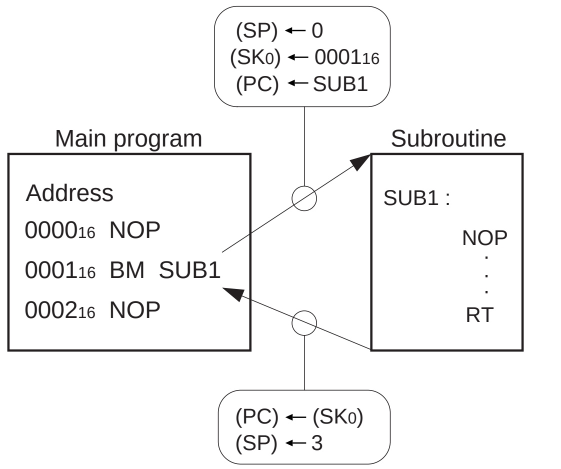
Skip flag controls skip decision for the conditional skip instructions and continuous described skip instructions.

Note : The 4280 Group just invalidates the next instruction when a skip is performed. The contents of program counter is not increased by 2. Accordingly, the number of cycles does not change even if skip is not performed. However, the cycle count becomes "1" if the TABP p, RT, or RTS instruction is skipped.



Stack pointer (SP) points "3" at reset or returning from RAM back-up mode. It points "0" by executing the first BM instruction, and the contents of program counter is stored in SK_0. When the BM instruction is executed after four stack registers are used ((SP) = 3), (SP) = 0 and the contents of SK_0 is destroyed.

Fig. 5 Stack registers (SKs) structure



Note: Returning to the BM instruction execution address with the RT instruction, and the BM instruction is equivalent to the NOP instruction.

Fig. 6 Example of operation at subroutine call

(8) Program counter (PC)

Program counter (PC) is used to specify a ROM address (page and address). It determines a sequence in which instructions stored in ROM are read. It is a binary counter that increments the number of instruction bytes each time an instruction is executed. However, the value changes to a specified address when branch instructions, subroutine call instructions, return instructions, or the table reference instruction (TABP p) is executed.

Program counter consists of PC_H (most significant bit to bit 7) which specifies to a ROM page and PC_L (bits 6 to 0) which specifies an address within a page. After it reaches the last address (address 127) of a page, it specifies address 0 of the next page (Figure 7).

Make sure that the PC_H does not exceed after the last page of the built-in ROM.

(9) Data pointer (DP)

Data pointer (DP) is used to specify a RAM address and consists of registers X and Y. Register X specifies a file and register Y specifies a RAM digit (Figure 8).

Register Y is also used to specify the port D bit position.

When using port D, set the port D bit position to register Y certainly and execute the SD, RD, or SZD instruction (Figure 9).

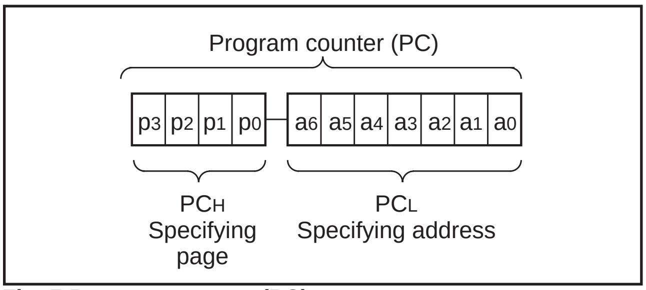


Fig. 7 Program counter (PC) structure

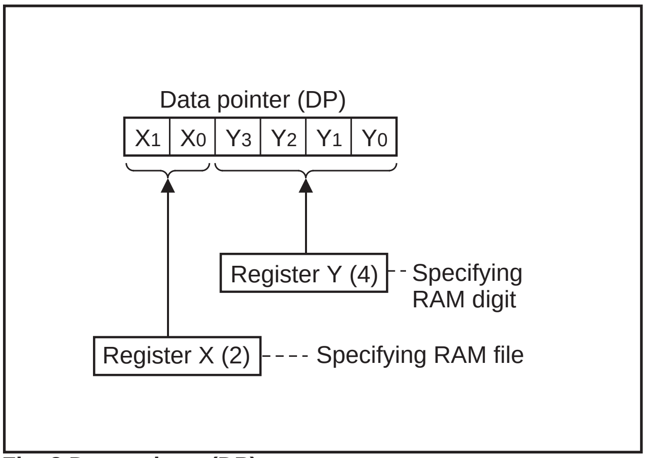


Fig. 8 Data pointer (DP) structure

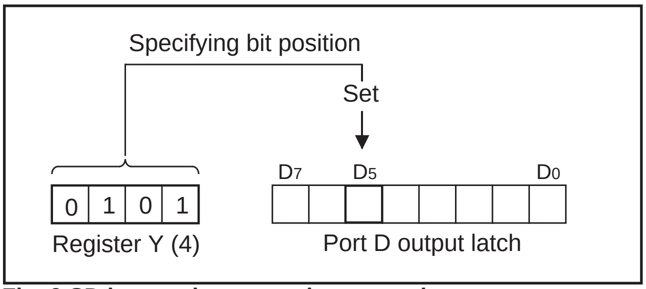


Fig. 9 SD instruction execution example

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PROGRAM MEMORY (ROM)

The program memory is a mask ROM. 1 word of ROM is composed of 9 bits. ROM is separated every 128 words by the unit of page (addresses 0 to 127).

Table 1 ROM size and pages

Product	ROM size (X 9 bits)	Pages
M34280M1	1024 words	8 (0 to 7)
M34280E1		

Page 2 (addresses 0100_{16} to $017F_{16}$) is the special page for subroutine calls. Subroutines written in this page can be called from any page with the 1-word instruction (BM). Subroutines extending from page 2 to another page can also be called with the BM instruction when it starts on page 2.
ROM pattern of all addresses can be used as data areas with the TABP p instruction.

DATA MEMORY (RAM)

1 word of RAM is composed of 4 bits, but 1-bit manipulation (with the SB j, RB j, and SZB j instructions) is enabled for the entire memory area. A RAM address is specified by a data pointer. The data pointer consists of registers X and Y. Set a value to the data pointer certainly when executing an instruction to access RAM.
Table 2 shows the RAM size. Figure 12 shows the RAM map.

Table 2 RAM size

Product	RAM size
M34280M1	32 words X 4 bits (128 bits)
M34280E1	

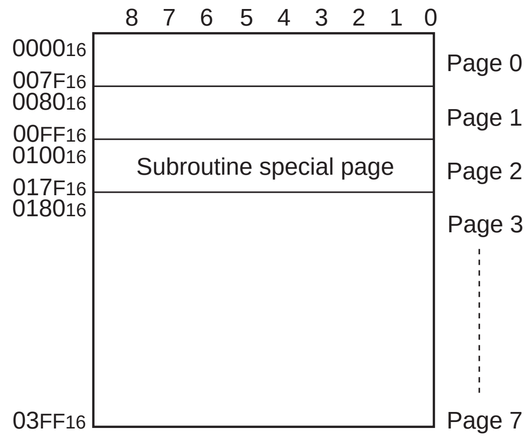

Fig. 10 ROM map of M34280M1

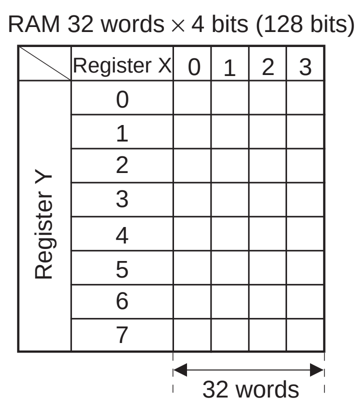

Fig. 11 RAM map

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TIMERS

The 4280 Group has the programmable timer.

- Programmable timer
  The programmable timer has a reload register and enables the frequency dividing ratio to be set. It is decremented from a setting value n. When it underflows (count to n + 1), a timer 1 underflow flag is set to “1,” new data is loaded from the reload register, and count continues (auto-reload function).

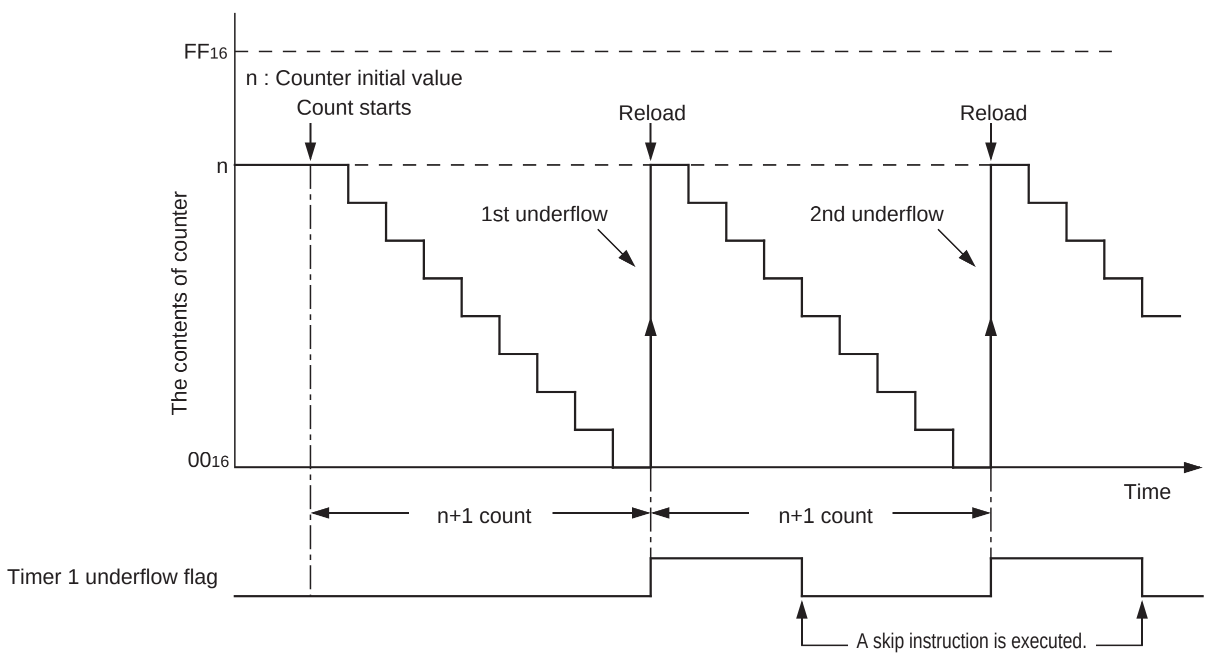

Fig. 12 Auto-reload function

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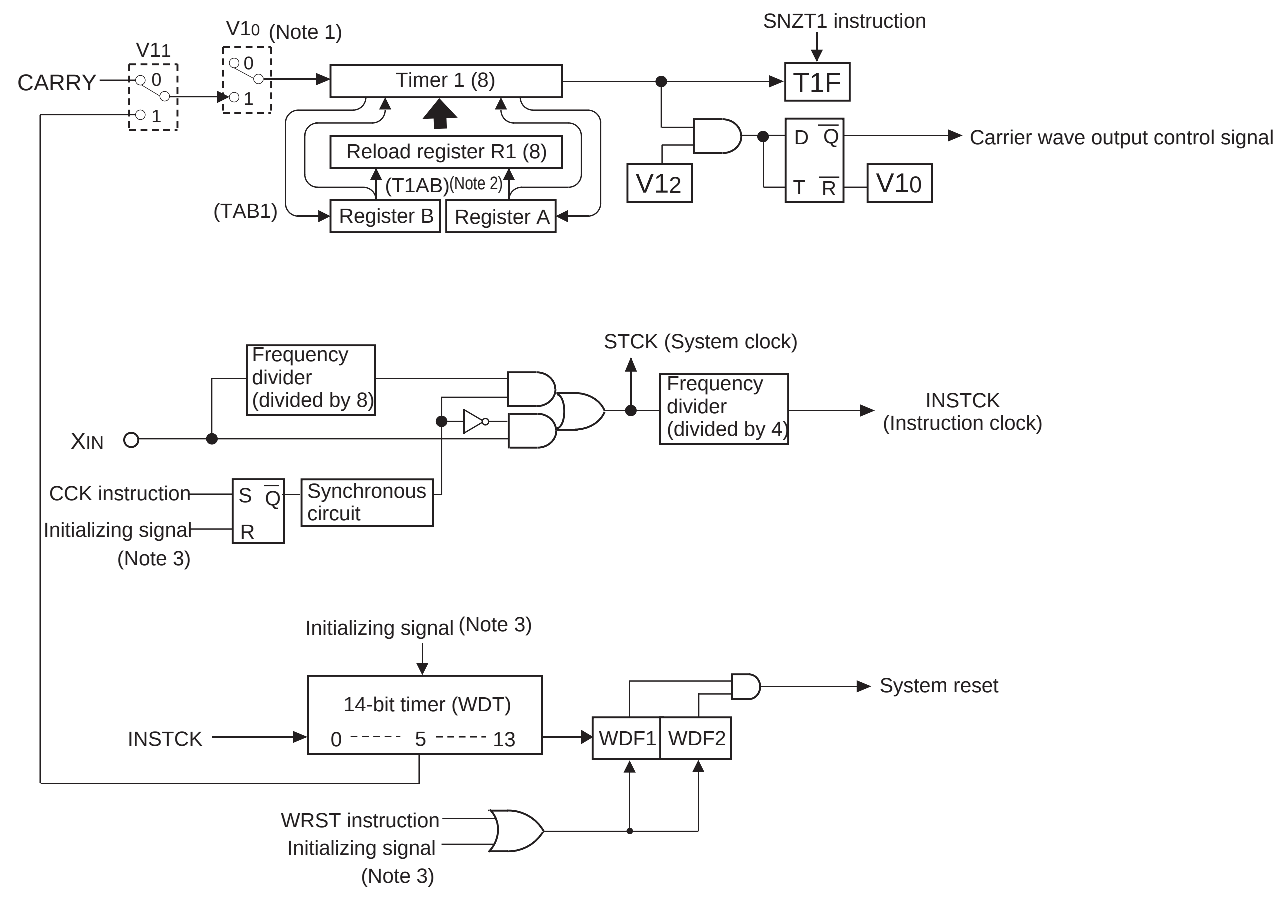
The 4280 Group timer consists of the following circuit.

- Timer 1 : 8-bit programmable timer

This timer can be controlled with the timer control register V1.
Timer 1 function is described below.

Table 3 Function related timer

Circuit	Structure	Count source	Frequency dividing ratio	Use of output signal	Control register
Timer 1	8-bit programmable binary down counter	• Carrier generating circuit output (CARRY) • Bit 5 of watchdog timer	1 to 256	• Carrier wave output control	V1



Notes 1: Counting is stopped by clearing to “0.”
2: When the T1AB instruction is executed after V10 is set to “1,” writing is performed only to reload register R1.
3: The initializing signal is output at reset or RAM back-up mode.

: Data is automatically set from a reload register when timer 1 underflows (auto-reload function).

Fig. 13 Timers structure

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Table 4 Control registers related to timer

Timer control register V1		at reset : 000_2		at RAM back-up : 000_2	W
$V1_2$	Carrier wave output auto-control bit	0	Auto-control output by timer 1 is invalid		
		1	Auto-control output by timer 1 is valid		
$V1_1$	Timer 1 count source selection bit	0	Carrier output (CARRY)		
		1	Bit 5 of watchdog timer (WDT)		
$V1_0$	Timer 1 control bit	0	Stop (Timer 1 state retained)		
		1	Operating		

Note: "W" represents write enabled.

(1) Control register related to timer

- Timer control register V1
  Register V1 controls the timer 1 count source and auto-control function of carrier wave output from port CARR by timer 1. Set the contents of this register through register A with the TV1A instruction.

(2) Precautions

Note the following for the use of timers.

- Count source
  Stop timer 1 counting to change its count source.
- Watchdog timer
  Be sure that the timing to execute the WRST instruction in order to operate WDT efficiently.
- Writing to reload register R1
  When writing data to reload register R1 while timer 1 is operating, avoid a timing when timer 1 underflows.

(3) Timer 1

Timer 1 is an 8-bit binary down counter with the timer 1 reload register (R1).
When timer is stopped, data can be set simultaneously in timer 1 and the reload register (R1) with the T1AB instruction.
When timer is operating, data can be set to only reload register R1 with the T1AB instruction.
When setting the next count data to reload register R1 at operating, set data before timer 1 underflows.
Timer 1 starts counting after the following process;
① set data in timer 1,
② select the count source with the bit 1 of register V1, and
③ set the bit 0 of register V1 to "1."
Once count is started, when timer 1 underflows (the next count pulse is input after the contents of timer 1 becomes "0"), the timer 1 underflow flag (T1F) is set to "1," new data is loaded from reload register R1, and count continues (auto-reload function).
When a value set in reload register R1 is n, timer 1 divides the count source signal by n + 1 (n = 0 to 255).
Data can be read from timer 1 to registers A and B. When reading the data, stop the counter and then execute the TAB1 instruction.

(4) Timer 1 underflow flag (T1F)

Timer 1 underflow flag is set to "1" when the timer 1 underflows.
The state of this flag can be examined with the skip instruction (SNZT1).
T1F flag is cleared to "0" when the next instruction is skipped with a skip instruction.

WATCHDOG TIMER

Watchdog timer provides a method to reset and restart the system when a program runs wild. Watchdog timer consists of 14-bit timer (WDT) and watchdog timer flags (WDF1, WDF2).
Watchdog timer downcounts the instruction clock (INSTCK) as the count source. When the timer WDT count value becomes 0000_{16} and underflow occurs, the WDF1 flag is set to "1." Then, when the WRST instruction is not executed before the timer WDT counts 16383, WDF2 flag is set to "1" and internal reset signal is generated and system reset is performed.
When using the watchdog timer, execute the WRST instruction at period of 16383 machine cycle or less to keep the microcomputer operation normal.
Timer WDT is also used for generation of oscillation stabilization time. When system is returned from reset and from RAM back-up mode by key-input, software starts after the stabilization oscillation time until timer WDT downcounts to $3E00_{16}$ elapses.

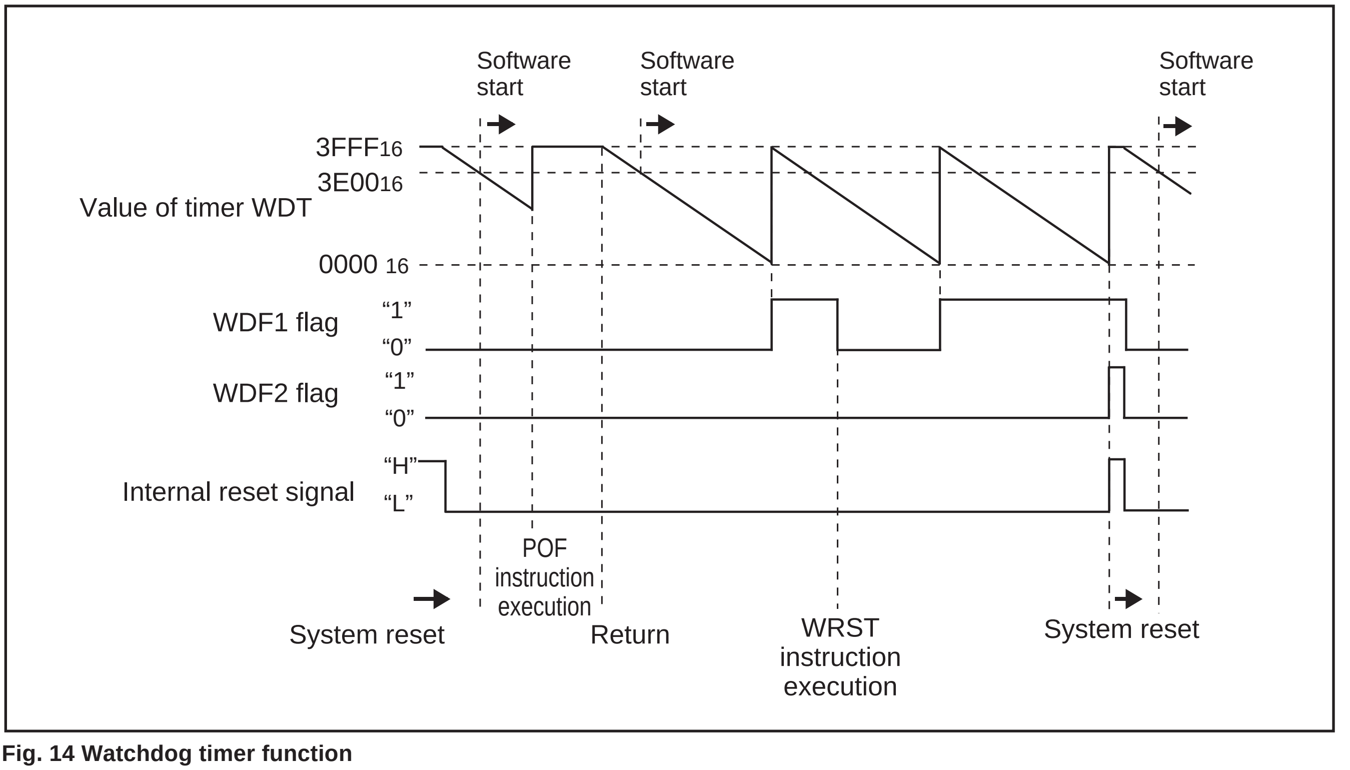

Fig. 14 Watchdog timer function

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CARRIER GENERATING CIRCUIT

The 4280 Group can output the various carrier waveforms by the carrier wave selection register C.

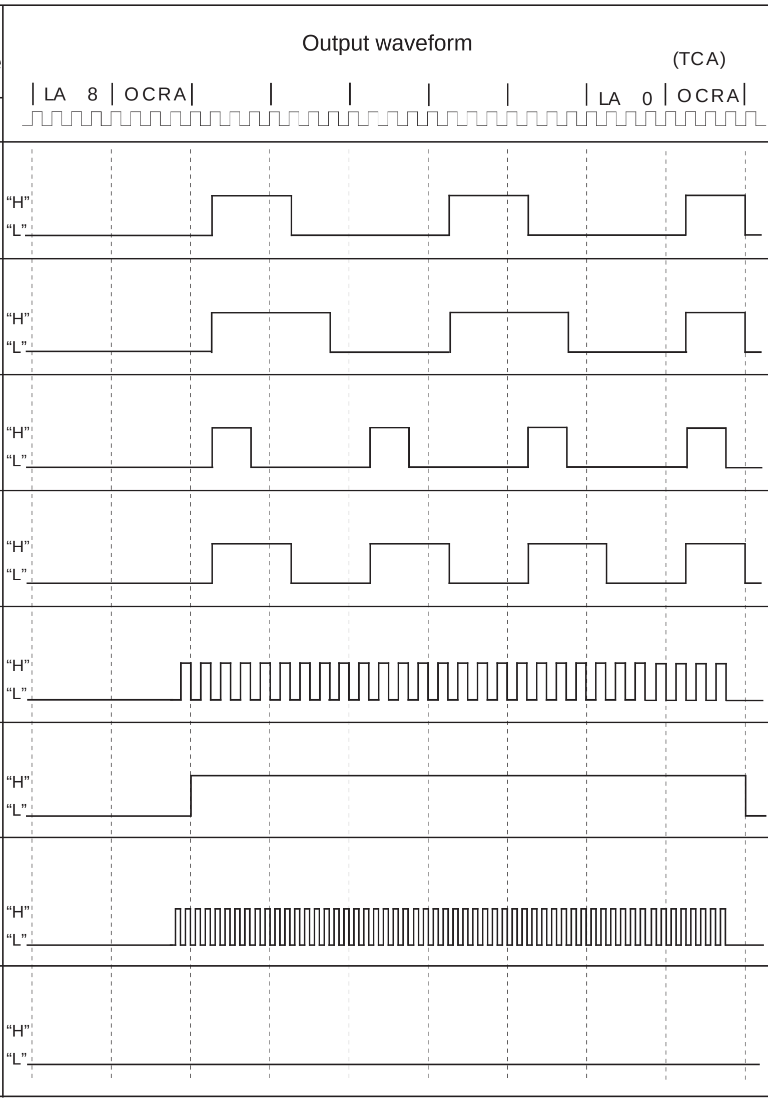
Set the contents of this register through register A with the TCA instruction. The TAC instruction can be used to transfer the contents of register C to register A. When the TCA instruction is executed, the output latch of port CARR is cleared to “0.”

The carrier waveform selected by setting register C can be output from port CARR by setting port CARR output latch to “1.” When the CARR output latch is cleared to “0,” carrier wave output is stopped and port CARR output is fixed to “L” level. The CARR output latch can be set through bit 3 (A_3) of register A with the OCRA instruction.

The relationship between the setting value of register C and selected waveform is described below.

Also, timer 1 can auto-control the carrier wave output from port CARR by setting the timer control register V1.

Carrier wave selection register C (at reset: 111_2, at RAM back-up: 111_2)



C_2	C_1	C_0	Output waveform	Carrier wave Frequency	Duty
0	0	0		System clock/12	1/3
0	0	1		System clock/12	1/2
0	1	0		System clock/8	1/4
0	1	1		System clock/8	1/2
1	0	0		System clock	1/2
1	0	1		No carrier wave	
1	1	0		f(XIN)/4 (Note)	1/2
1	1	1		“L” level fixed	

Note: This carrier wave can be used only when system clock f(XIN)/8 is selected.
The carrier wave output is fixed to “L” level when system clock f(XIN) is selected.

Fig. 15 Carrier wave selection register

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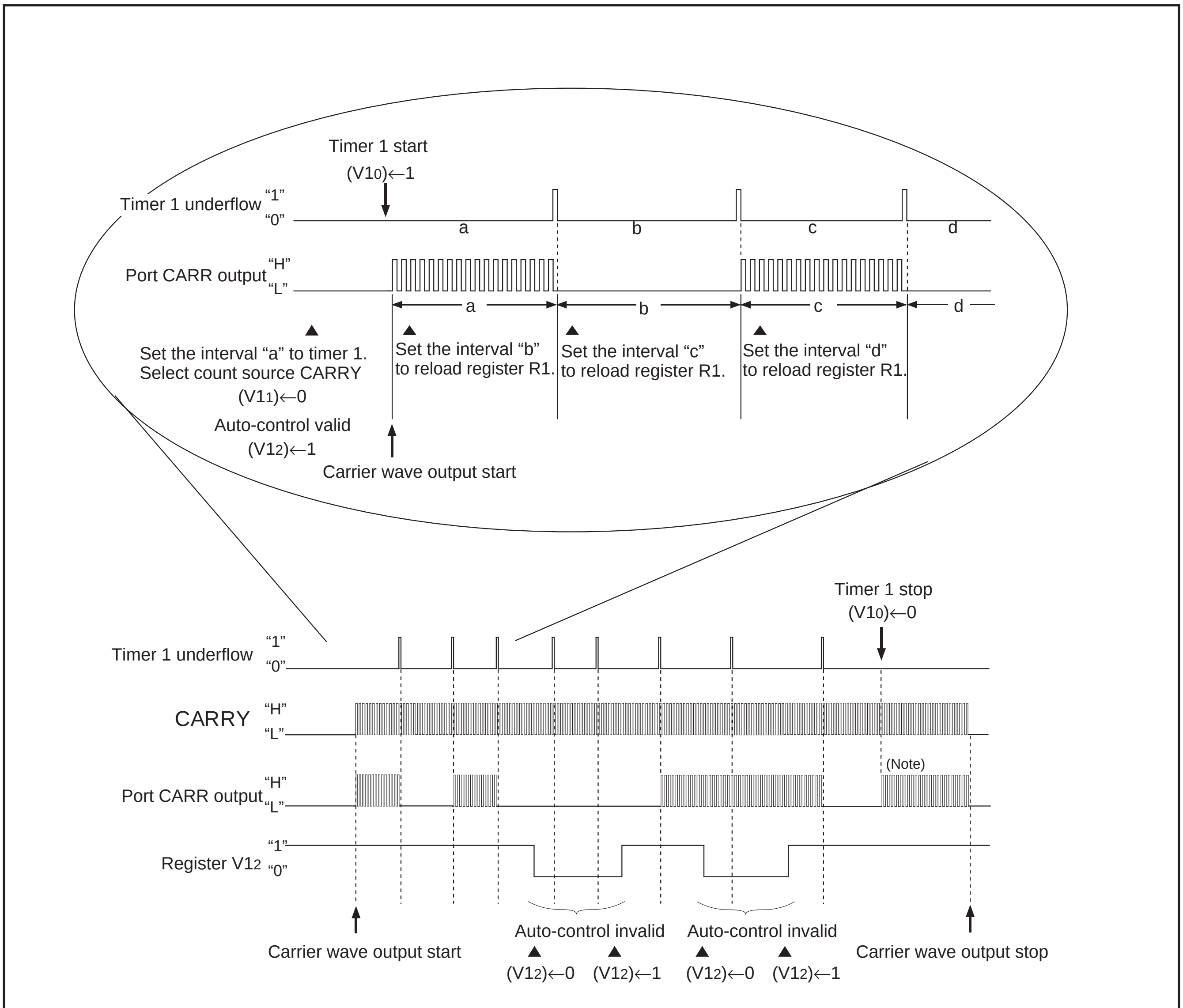

Fig. 16 Port CARR output auto-control by timer 1

LOGIC OPERATION FUNCTION

The 4280 Group has the 4-bit logic operation function. The logic operation between the contents of register A and the low-order 4 bits of register E is performed and its result is stored in register A.

Each logic operation can be selected by setting logic operation selection register LO.

Set the contents of this register through register A with the TLOA instruction. The logic operation selected by register LO is executed with the LGOP instruction.

Table 5 shows the logic operation selection register LO.

Table 5 Logic operation selection register LO

Logic operation selection register LO		at reset : 00_2		at RAM back-up : 00_2	W
		LO_1	LO_0	Logic operation function	
LO_1	Logic operation selection bits	0	0	Exclusive logic OR operation (XOR)	
		0	1	OR operation (OR)	
LO_0		1	0	AND operation (AND)	
		1	1	Not available	

Note: "W" represents write enabled.

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RESET FUNCTION

The 4280 Group has the power-on reset circuit, though it does not have $\overline{\text{RESET}}$ pin. System reset is performed automatically at power-on, and software starts program from address 0 in page 0.

In order to make the built-in power-on reset circuit operate efficiently, set the voltage rising time until V_{DD}= 0 to 2.2 V is obtained at power-on 1ms or less.

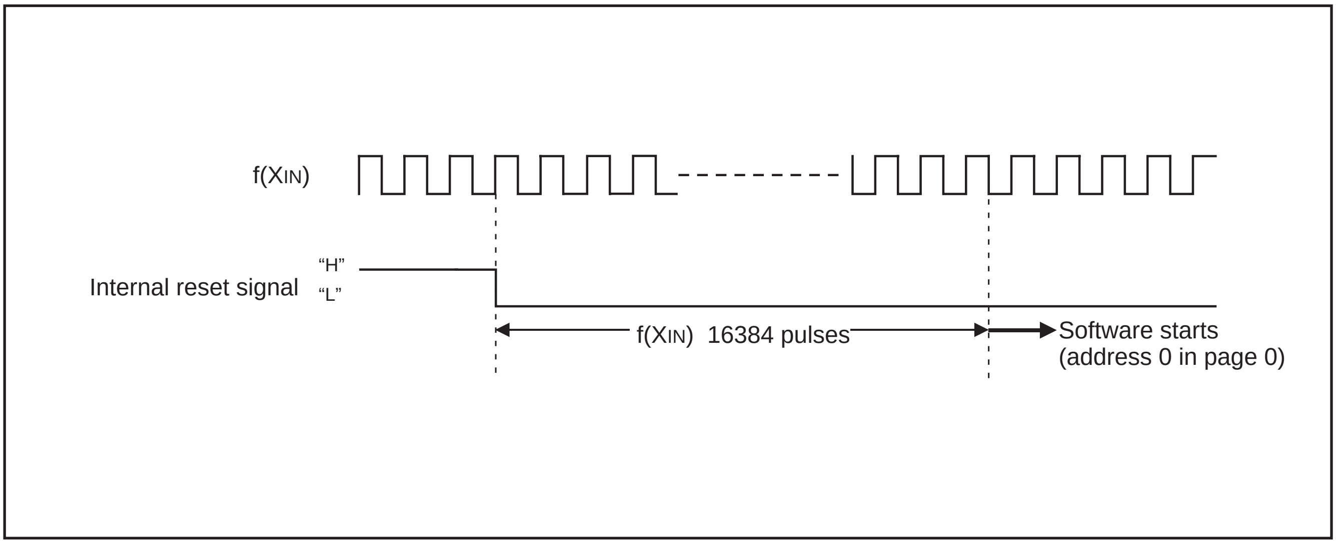

Fig. 17 Reset release timing

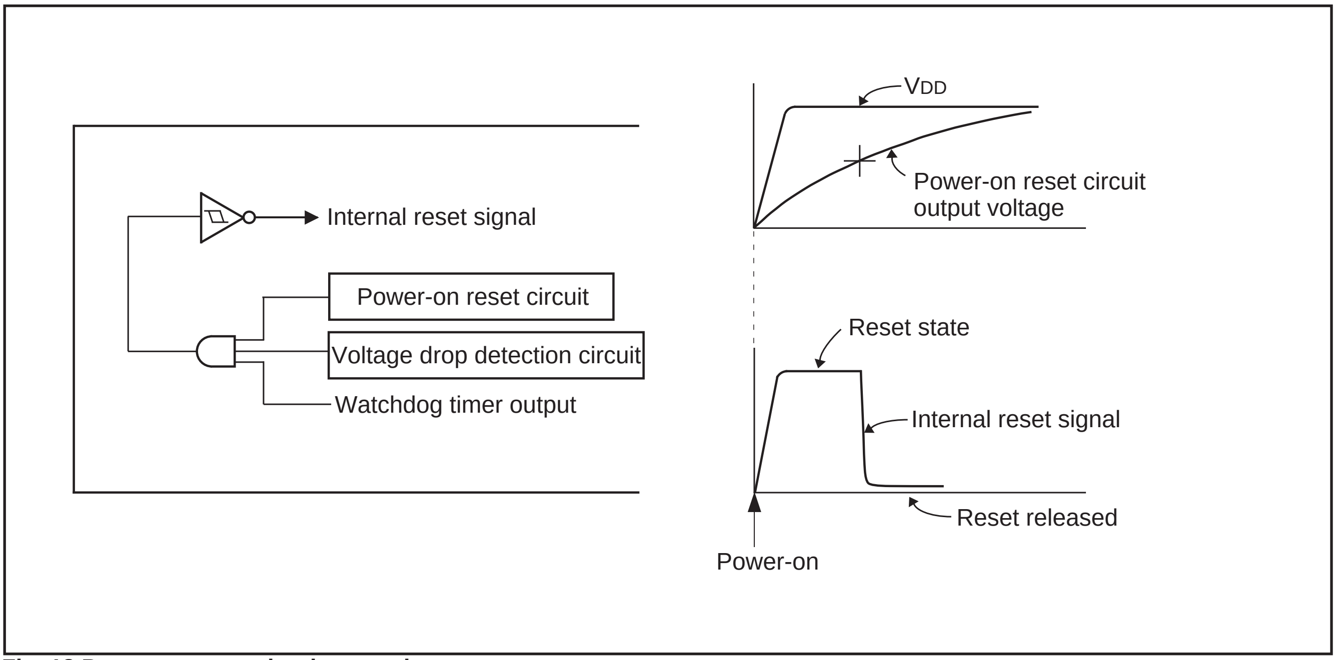

Fig. 18 Power-on reset circuit example

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(1) Internal state at reset

Table 6 shows port state at reset, and Figure 19 shows internal state at reset (they are retained after system is released from reset).

The contents of timers, registers, flags and RAM except shown in Figure 19 are undefined, so set the initial value to them.

- Program counter (PC) 0 0 0 0 0 0 0 0 0 0
  Address 0 in page 0 is set to program counter.
- Power down flag (P) 0
- Timer 1 underflow flag (T1F) 0
- Timer control register V1 .... 0 0 0
- Carrier wave selection register C 1 1 1
- Pull-down control register PU0 .... 0 0 0
- Logic operation selection register LO 0 0
- Most significant ROM code reference enable flag (URS) 0
- Carry flag (CY) 0
- Register A 1 1 1 1
- Register B 1 1 1 1
- Stack pointer (SP) 1 1

Fig. 19 Internal state at reset

Table 6 Port state at reset

Name	State at reset	State after system is released from reset
D_0–D_6	"H" output	High impedance state
D_7	"H" output	Input circuit OFF (Pull-down transistor OFF)
G_0–G_3, E_2	Input port (Pull-down transistor ON)	Input port (Pull-down transistor ON)
E_0, E_1	Input circuit OFF (Pull-down transistor OFF)	Input port (Pull-down transistor OFF)

Note: The contents of all output latch is initialized to "0."

VOLTAGE DROP DETECTION CIRCUIT

The built-in drop detection circuit is designed to detect a drop in voltage at operating and to reset the microcomputer if the supply voltage drops below the specified value (Typ. 1.50 V) or less.

The voltage drop detection circuit is stopped and power dissipation is reduced at the RAM back-up mode, when the functions except the RAM and pull-down control register (PU0) are initialized.

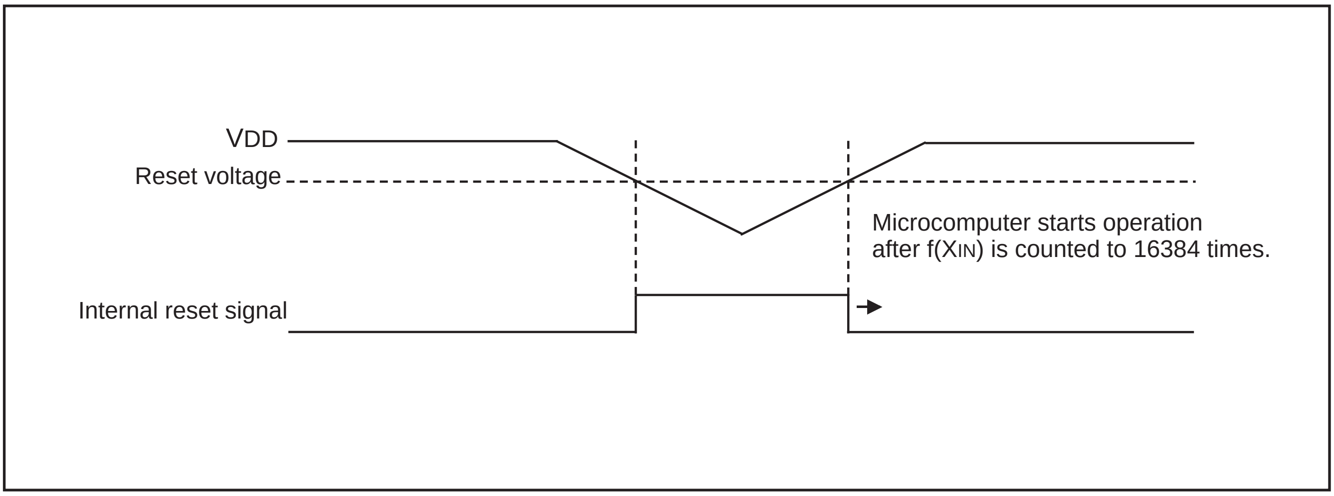

Fig. 20 Voltage drop detection circuit operation waveform

RAM BACK-UP MODE

The 4280 Group has the RAM back-up mode.
When the POF instruction is executed, system enters the RAM back-up state.
As oscillation stops retaining RAM, the function of reset circuit and states at RAM back-up mode, power dissipation can be reduced without losing the contents of RAM. Table 7 shows the function and states retained at RAM back-up. Figure 21 shows the state transition.

(1) Identification of the start condition

Warm start (return from the RAM back-up state) or cold start (return from the normal reset state) can be identified by examining the state of the power down flag (P) with the SNZP instruction.

(2) Warm start condition

When the external wakeup signal is input after the system enters the RAM back-up state by executing the POF instruction, the CPU starts executing the software from address 0 in page 0. In this case, the P flag is “1.”

(3) Cold start condition

The CPU starts executing the software from address 0 in page 0 when any of the following conditions is satisfied .
• reset by power-on reset circuit is performed
• reset by watchdog timer is performed
• reset by voltage drop detection circuit is performed
In this case, the P flag is “0.”

Table 7 Functions and states retained at RAM back-up

Function		RAM back-up
Program counter (PC), registers A, B, carry flag (CY), stack pointer (SP) (Note 2)		X
Contents of RAM		O
Ports D_0–D_6 (Note 3)		X (“H” output)
Port D_7	$(PU0_2)=0$ (Note 3)	X (“H” output)
	$(PU0_2)=1$	X (input)
Port E_0	$(PU0_0)=0$ (Note 4)	X (input cut-off)
	$(PU0_0)=1$	X (input)
Port E_1	$(PU0_1)=0$ (Note 4)	X (input cut-off)
	$(PU0_1)=1$	X (input)
Port G		X (input)
Timer control register V1		X
Pull-down control register PU0		O
Logic operation selection register LO		X
Timer 1 function		X
Timer 1 underflow flag (T1F)		X
Watchdog timer (WDT)		X
Watchdog timer flag 1 (WDF1)		X
Watchdog timer flag 2 (WDF2)		X
Most significant ROM code reference enable flag (URS)		X

Notes 1: “O” represents that the function can be retained, and “X” represents that the function is initialized.
Registers and flags other than the above are undefined at RAM back-up, and set an initial value after returning.
2:The stack pointer (SP) points the level of the stack register and is initialized to “11_2” at RAM back-up.
3: The contents of port output latch is initialized to “0.” However, port continues to output “H” level.
4: The state of this bit is equal to the state at reset.

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(4) Return signal

An external wakeup signal is used to return from the RAM back-up mode. Table 8 shows the return condition for each return source.

Table 8 Return source and return condition

Return source	Return condition	Remarks
Ports D_7, E_0, E_1	Return by an external "H" level input.	Only key-on wakeup function of the port whose pull-down transistor is turned ON is valid.
Ports G, E_2	Return by an external "H" level input.	Key-on wakeup function is always valid.

(5) Pull-down control register PU0

- Pull-down control register PU0
  Register PU0 controls the ON/OFF of pull-down transistor, input, key-on wakeup function of ports E_0, E_1 and D_7.

Set the contents of this register through register A with the TPU0A instruction.

Table 9 Pull-down control register

Pull-down control register PU0		at reset : 000_2	at RAM back-up : state retained	W
$PU0_2$	Port D_7 pull-down control bit	0	Pull-down transistor OFF, input circuit OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, input circuit ON, key-on wakeup valid	
$PU0_1$	Port E_1 pull-down control bit	0	Pull-down transistor OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, key-on wakeup valid	
$PU0_0$	Port E_0 pull-down control bit	0	Pull-down transistor OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, key-on wakeup valid	

Note: "W" represents write enabled.

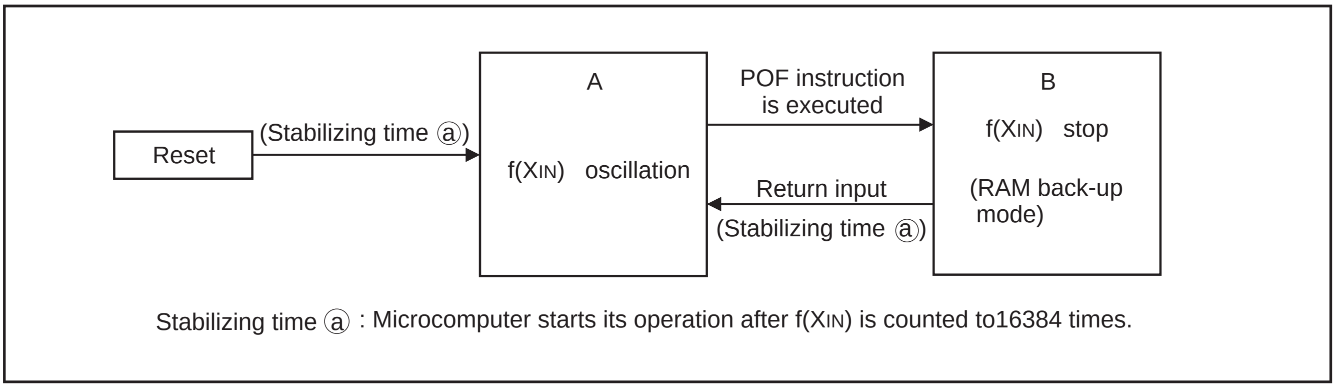

Fig. 21 State transition

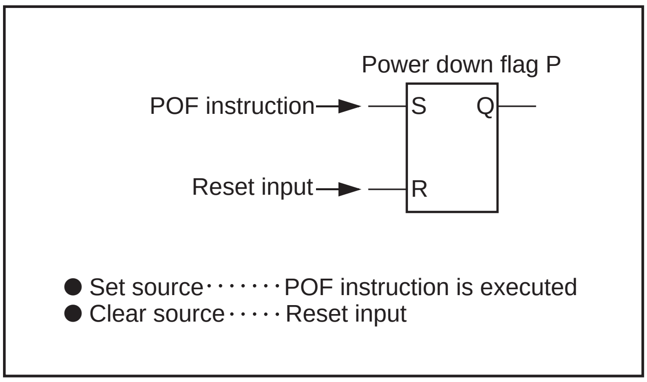

Fig. 22 Set source and clear source of the P flag

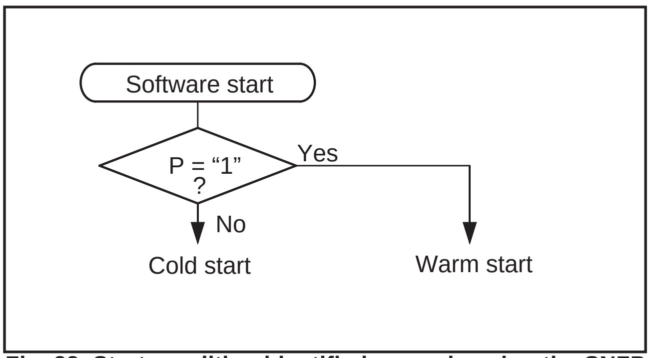

Fig. 23 Start condition identified example using the SNZP instruction

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CLOCK CONTROL

The clock control circuit consists of the following circuits.

- System clock generating circuit
- Control circuit to stop the clock oscillation
- Control circuit to return from the RAM back-up state

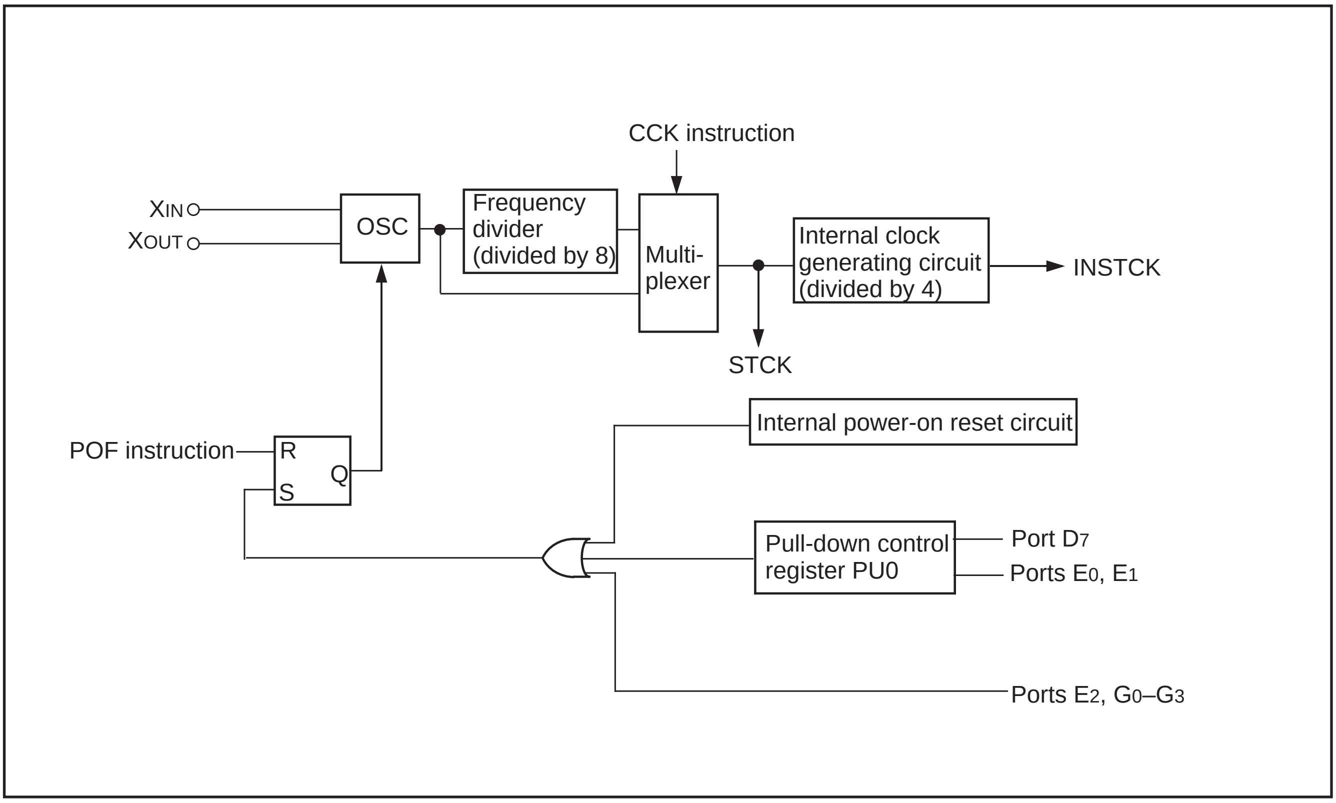

Fig. 24 Clock control circuit structure

Clock signal f(XIN) is obtained by externally connecting a ceramic resonator. Connect this external circuit to pins XIN and XOUT at the shortest distance as shown Figure 26.
A feedback resistor is built-in between XIN pin and XOUT pin.

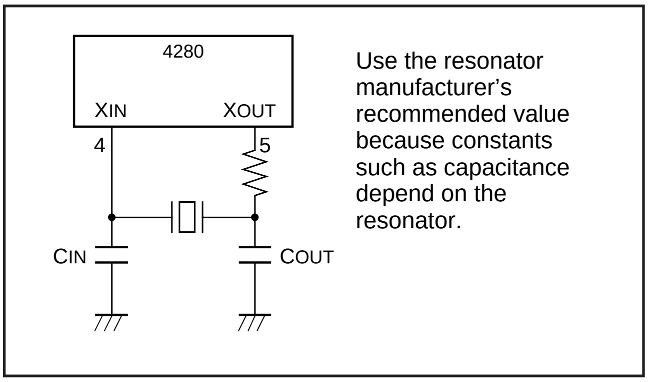

Fig. 25 Ceramic resonator external circuit

ROM ORDERING METHOD

Please submit the information described below when ordering Mask ROM.

(1) Mask ROM Order Confirmation Form................................1
(2) Data to be written into mask ROM......................... EPROM
(three sets containing the identical data)
(3) Mark Specification Form 1

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LIST OF PRECAUTIONS

① Noise and latch-up prevention

Connect a capacitor on the following condition to prevent noise and latch-up;

- connect a bypass capacitor (approx. 0.01 μF) between pins V_{DD} and V_{SS} at the shortest distance,
- equalize its wiring in width and length, and
- use the thickest wire.

In the One Time PROM version, port E_2 is also used as V_{PP} pin. Connect this pin to V_{SS} through the resistor about 5 kΩ which is assigned to E_2/V_{PP} pin as close as possible at the shortest distance.

② Notes on unused pins

(Note in order to set the output latch to “0” to make pins open)

- After system is released from reset, a port is in a high-impedance state until the output latch of the port is set to “0” by software.
  Accordingly, the voltage level of pins is undefined and the excess of the supply current may occur.
- To set the output latch periodically is recommended because the value of output latch may change by noise or a program run away (caused by noise).

(Note when connecting to V_{SS} and V_{DD})

- Connect the unused pins to V_{SS} and V_{DD} at the shortest distance and use the thick wire against noise.

③ Timer

- Count source
  Stop timer 1 counting to change its count source.
- Watchdog timer
  Be sure that the timing to execute the WRST instruction in order to operate WDT efficiently.
- Writing to reload register R1
  When writing data to reload register R1 while timer 1 is operating, avoid a timing when timer 1 underflows.

④ Program counter

Make sure that the program counter does not specify after the last page of the built-in ROM.

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SYMBOL

The symbols shown below are used in the following list of instruction function and the machine instructions.

Symbol	Contents	Symbol	Contents
A	Register A (4 bits)	D	Port D (8 bits)
B	Register B (4 bits)	E	Port E (3 bits)
DR	Register D (3 bits)	G	Port G (4 bits)
ER	Register E (8 bits)	CARR	Port CARR (1 bit)
C	Carrier wave selection register C (3 bits)		
V1	Timer control register V1 (3 bits)	x	Hexadecimal variable
PU0	Pull-down control register PU0 (3 bits)	y	Hexadecimal variable
LO	Logic operation selection register LO (2 bits)	p	Hexadecimal variable
		n	Hexadecimal constant which represents the
X	Register X (2 bits)		immediate value
Y	Register Y (4 bits)	j	Hexadecimal constant which represents the
DP	Data pointer (6 bits)		immediate value
	(It consists of registers X and Y)	$A_3A_2A_1A_0$	Binary notation of hexadecimal variable A
PC	Program counter (10 bits)		(same for others)
PC_H	High-order 3 bits of program counter		
PC_L	Low-order 7 bits of program counter	←	Direction of data movement
SK	Stack register (10 bits × 4)	↔	Data exchange between a register and memory
SP	Stack pointer (2 bits)	?	Decision of state shown before "?"
CY	Carry flag	( )	Contents of registers and memories
R1	Timer 1 reload register	—	Negate, Flag unchanged after executing
T1	Timer 1		instruction
T1F	Timer 1 underflow flag	M(DP)	RAM address pointed by the data pointer
WDT	Watchdog timer	a	Label indicating address a_6 a_5 a_4 a_3 a_2 a_1 a_0
WDF1	Watchdog timer flag 1	p, a	Label indicating address a_6 a_5 a_4 a_3 a_2 a_1 a_0
WDF2	Watchdog timer flag 2		in page p_3 p_2 p_1 p_0
URS	Most significant ROM code reference enable flag	C	Hex. number C + Hex. number x (also same for
P	Power down flag	+	others)
STCK	System clock	x	
INSTCK	Instruction clock		

Note : The 4280 Group just invalidates the next instruction when a skip is performed. The contents of program counter is not increased by 2. Accordingly, the number of cycles does not change even if skip is not performed. However, the cycle count becomes "1" if the TABP p, RT, or RTS instruction is skipped.

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LIST OF INSTRUCTION FUNCTION

Grouping	Mnemonic	Function
Register to register transfer	TAB	(A) ← (B)
	TBA	(B) ← (A)
	TAY	(A) ← (Y)
	TYA	(Y) ← (A)
	TEAB	(ER_7–ER_4) ← (B) (ER_3–ER_0) ← (A)
	TABE	(B) ← (ER_7–ER_4) (A) ← (ER_3–ER_0)
	TDA	(DR_2–DR_0) ← (A_2–A_0)
RAM addresses	LXY x, y	(X) ← x, x = 0 to 3 (Y) ← y, y = 0 to 15
	INY	(Y) ← (Y) + 1
	DEY	(Y) ← (Y) – 1
RAM to register transfer	TAM j	(A) ← (M(DP)) (X) ← (X) EXOR(j) j = 0 to 3
	XAM j	(A) ←→ (M(DP)) (X) ← (X) EXOR(j) j = 0 to 3
	XAMD j	(A) ←→ (M(DP)) (X) ← (X) EXOR(j) j = 0 to 3 (Y) ← (Y) – 1
	XAMI j	(A) ←→ (M(DP)) (X) ← (X) EXOR(j) j = 0 to 3 (Y) ← (Y) + 1

Grouping	Mnemonic	Function
Arithmetic operation	LA n	(A) ← n n = 0 to 15
	TABP p	(SP) ← (SP) + 1 (SK(SP)) ← (PC) (PC_H) ← p p=0 to 7 (PC_L) ← (DR_2–DR_0, A_3–A_0) When URS=0 (B) ← $(ROM(PC))_{7\ to\ 4}$ (A) ← $(ROM(PC))_{3\ to\ 0}$ When URS=1 (CY) ← $(ROM(PC))_8$ (B) ← $(ROM(PC))_{7\ to\ 4}$ (A) ← $(ROM(PC))_{3\ to\ 0}$ (PC) ← (SK(SP)) (SP) ← (SP) – 1
	AM	(A) ← (A) + (M(DP))
	AMC	(A) ← (A) + (M(DP)) + (CY) (CY) ← Carry
	A n	(A) ← (A) + n n = 0 to 15
	SC	(CY) ← 1
	RC	(CY) ← 0
	SZC	(CY) = 0 ?
	CMA	(A) ← ($\overline{A}$)
	RAR	→ CY → $A_3A_2A_1A_0$ → (rotate)
	LGOP	Logic operation instruction XOR, OR, AND
Bit operation	SB j	(Mj(DP)) ← 1 j = 0 to 3
	RB j	(Mj(DP)) ← 0 j = 0 to 3
	SZB j	(Mj(DP)) = 0 ? j = 0 to 3

Grouping	Mnemonic	Function
Comparison operation	SEAM	(A) = (M(DP)) ?
	SEA n	(A) = n ? n = 0 to 15
Branch operation	B a	(PC_L) ← a_6–a_0
	BL p, a	(PC_H) ← p (PC_L) ← a_6–a_0
	BA a	(PC_L) ← (a_6–a_4, A_3–A_0)
	BLA p, a	(PC_H) ← p (PC_L) ← (a_6–a_4, A_3–A_0)
Subroutine operation	BM a	(SP) ← (SP) + 1 (SK(SP)) ← (PC) (PC_H) ← 2 (PC_L) ← a_6–a_0
	BML p, a	(SP) ← (SP) + 1 (SK(SP)) ← (PC) (PC_H) ← p p= 0 to 7 (PC_L) ← a_6–a_0
	BMLA p, a	(SP) ← (SP) + 1 (SK(SP)) ← (PC) (PC_H) ← p p= 0 to 7 (PC_L) ← (a_6–a_4, A_3–A_0)
Return operation	RT	(PC) ← (SK(SP)) (SP) ← (SP) – 1
	RTS	(PC) ← (SK(SP)) (SP) ← (SP) – 1

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LIST OF INSTRUCTION FUNCTION (CONTINUED)

Grouping	Mnemonic	Function	Grouping	Mnemonic	Function
Timer operation	TV1A	$(V1_2–V1_0) \leftarrow (A_2–A_0)$	Other operation	NOP	$(PC) \leftarrow (PC) + 1$
	TAB1	$(B) \leftarrow (T1_7–T1_4)$ $(A) \leftarrow (T1_3–T1_0)$		POF	RAM back-up
				SNZP	(P) = 1 ?
	T1AB	at timer 1 stop ($V1_0$=0): $(R1_7–R1_4) \leftarrow (B)$ $(T1_7–T1_4) \leftarrow (B)$ $(R1_3–R1_0) \leftarrow (A)$ $(T1_3–T1_0) \leftarrow (A)$ at timer 1 operating: ($V1_0$=1) $(R1_7–R1_4) \leftarrow (B)$ $(R1_3–R1_0) \leftarrow (A)$		CCK	STCK changes to $f(X_{IN})$
				TLOA	$(LO_1, LO_0) \leftarrow (A_1, A_0)$
				URSC	$(URS) \leftarrow 1$
				TPU0A	$(PU0_2–PU0_0) \leftarrow (A_2–A_0)$
				WRST	$(WDF1) \leftarrow 0$
	SNZ1	(T1F) = 1 ? After skipping the next instruction $(T1F) \leftarrow 0$			
Carrier wave control operation	TCA	$(C_2–C_0) \leftarrow (A_2–A_0)$ $(CARR) \leftarrow 0$			
	TAC	$(A_2–A_0) \leftarrow (C_2–C_0)$			
	OCRA	$(CARR) \leftarrow (A_3)$			
Input/Output operation	CLD	$(D) \leftarrow 1$			
	RD	$(D(Y)) \leftarrow 0$ (Y) = 0 to 7			
	SD	$(D(Y)) \leftarrow 1$ (Y) = 0 to 7			
	SZD	(D(Y)) = 0 ? (Y) = 7			
	OEA	$(E_1, E_0) \leftarrow (A_1, A_0)$			
	IAE	$(A_2–A_0) \leftarrow (E_2–E_0)$			
	OGA	$(G) \leftarrow (A)$			
	IAG	$(A) \leftarrow (G)$			

INSTRUCTION CODE TABLE

D8–D4		00000	00001	00010	00011	00100	00101	00110	00111	01000	01001	01010	01011	01100	01101	01110	01111	10000 10111	11000 11111
D3–D0	Hex. notation	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10–17	18–1F
0000	0	NOP	BLA	SZB 0	BL	TAC	BMLA	XAM 0	BML	OGA	TABP 0	A 0	LA 0	LXY 0,0	LXY 1,0	LXY 2,0	LXY 3,0	BM	B
0001	1	BA	CLD	SZB 1	BL	LGOP	—	XAM 1	BML	—	TABP 1	A 1	LA 1	LXY 0,1	LXY 1,1	LXY 2,1	LXY 3,1	BM	B
0010	2	—	—	SZB 2	BL	SNZT1	—	XAM 2	BML	URSC	TABP 2	A 2	LA 2	LXY 0,2	LXY 1,2	LXY 2,2	LXY 3,2	BM	B
0011	3	SNZP	INY	SZB 3	BL	—	—	XAM 3	BML	—	TABP 3	A 3	LA 3	LXY 0,3	LXY 1,3	LXY 2,3	LXY 3,3	BM	B
0100	4	—	RD	SZD	BL	RT	—	TAM 0	BML	OEA	TABP 4	A 4	LA 4	LXY 0,4	LXY 1,4	LXY 2,4	LXY 3,4	BM	B
0101	5	—	SD	SEAn	BL	RTS	—	TAM 1	BML	—	TABP 5	A 5	LA 5	LXY 0,5	LXY 1,5	LXY 2,5	LXY 3,5	BM	B
0110	6	RC	—	SEAM	BL	—	IAE	TAM 2	BML	OCRA	TABP 6	A 6	LA 6	LXY 0,6	LXY 1,6	LXY 2,6	LXY 3,6	BM	B
0111	7	SC	DEY	—	BL	T1AB	TAB1	TAM 3	BML	—	TABP 7	A 7	LA 7	LXY 0,7	LXY 1,7	LXY 2,7	LXY 3,7	BM	B
1000	8	—	—	IAG	—	—	TLOA	XAMI 0	—	—	—	A 8	LA 8	LXY 0,8	LXY 1,8	LXY 2,8	LXY 3,8	BM	B
1001	9	—	—	TDA	—	—	CCK	XAMI 1	—	—	—	A 9	LA 9	LXY 0,9	LXY 1,9	LXY 2,9	LXY 3,9	BM	B
1010	A	AM	TEAB	TABE	—	—	TCA	XAMI 2	—	—	—	A 10	LA 10	LXY 0,10	LXY 1,10	LXY 2,10	LXY 3,10	BM	B
1011	B	AMC	—	—	—	—	TV1A	XAMI 3	—	—	—	A 11	LA 11	LXY 011	LXY 1,11	LXY 2,11	LXY 3,11	BM	B
1100	C	TYA	CMA	—	—	RB 0	SB 0	XAMD 0	—	—	—	A 12	LA 12	LXY 0,12	LXY 1,12	LXY 2,12	LXY 3,12	BM	B
1101	D	POF	RAR	—	—	RB 1	SB 1	XAMD 1	—	—	—	A 13	LA 13	LXY 0,13	LXY 1,13	LXY 2,13	LXY 3,13	BM	B
1110	E	TBA	TAB	—	—	RB 2	SB 2	XAMD 2	—	—	—	A 14	LA 14	LXY 0,14	LXY 1,14	LXY 2,14	LXY 3,14	BM	B
1111	F	WRST	TAY	SZC	—	RB 3	SB 3	XAMD 3	—	TPU0A	—	A 15	LA 15	LXY 0,15	LXY 1,15	LXY 2,15	LXY 3,15	BM	B

The above table shows the relationship between machine language codes and machine language instructions. D_3–D_0 show the low-order 4 bits of the machine language code, and D_8–D_4 show the high-order 5 bits of the machine language code. The hexadecimal representation of the code is also provided. There are one-word instructions and two-word instructions, but only the first word of each instruction is shown. Do not use the code marked "–."

The codes for the second word of a two-word instruction are described below.

	The second word
BL	1 1aaa aaaa
BML	1 0aaa aaaa
BA	1 1aaa aaaa
BLA	1 1aaa 0ppp
BMLA	1 0aaa 0ppp
SEA	0 1011 nnnn
SZD	0 0010 1011

(A) ← (Y)	–	–	Transfers the contents of register Y to register A.
(Y) ← (A)	–	–	Transfers the contents of register A to register Y.
(ER_7–ER_4) ← (B) (ER_3–ER_0) ← (A)	–	–	Transfers the contents of registers A and B to register E.
(B) ← (ER_7–ER_4) (A) ← (ER_3–ER_0)	–	–	Transfers the contents of register E to registers A and B.
(DR_2–DR_0) ← (A_2–A_0)	–	–	Transfers the contents of register A to register D.
(X) ← x, x = 0 to 3 (Y) ← y, y = 0 to 15	Continuous description	–	Loads the value x in the immediate field to register X, and the value y in the immediate field to register Y. When the LXY instructions are continuously coded and executed, only the first LXY instruction is executed and other LXY instructions coded continuously are skipped.
(Y) ← (Y) + 1	(Y) = 0	–	Adds 1 to the contents of register Y. As a result of addition, when the contents of register Y is 0, the next instruction is skipped.
(Y) ← (Y) – 1	(Y) = 15	–	Subtracts 1 from the contents of register Y. As a result of subtraction, when the contents of register Y is 15, the next instruction is skipped.
(A) ← (M(DP)) (X) ← (X) EXOR(j) j = 0 to 3	–	–	After transferring the contents of M(DP) to register A, an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X.
(A) ←→ (M(DP)) (X) ← (X) EXOR(j) j = 0 to 3	–	–	After exchanging the contents of M(DP) with the contents of register A, an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X.
(A) ←→ (M(DP)) (X) ← (X) EXOR(j) j = 0 to 3 (Y) ← (Y) – 1	(Y) = 15	–	After exchanging the contents of M(DP) with the contents of register A, an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X. Subtracts 1 from the contents of register Y. As a result of subtraction, when the contents of register Y is 15, the next instruction is skipped.
(A) ←→ (M(DP)) (X) ← (X) EXOR(j) j = 0 to 3 (Y) ← (Y) + 1	(Y) = 0	–	After exchanging the contents of M(DP) with the contents of register A, an exclusive OR operation is performed between register X and the value j in the immediate field, and stores the result in register X. Adds 1 to the contents of register Y. As a result of addition, when the contents of register Y is 0, the next instruction is skipped.

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(SK(SP)) ← (PC) (SP) ← (SP) + 1 (PC_H) ← p, p=0 to 7 (PC_L) ← (DR_2–DR_0, A_3–A_0) When URS=0, (B) ← $(ROM(PC))_{7\ to\ 4}$ (A) ← $(ROM(PC))_{3\ to\ 0}$ When URS=1, (CY) ← $(ROM(PC))_8$ (B) ← $(ROM(PC))_{7\ to\ 4}$ (A) ← $(ROM(PC))_{3\ to\ 0}$ (SP) ← (SP) – 1 (PC) ← (SK(SP))	–	– / 0/1	Transfers bits 7 to 4 to register B and bits 3 to 0 to register A when URS flag is cleared to "0." These bits 7 to 0 are the ROM pattern in address (DR_2 DR_1 DR_0 A_3 A_2 A_1 A_0) specified by registers A and D in page p. When this instruction is executed, 1 stage of stack register is used. Transfers bit 8 of ROM pattern is transferred to flag CY when URS flag is set to "1" (after the URSC instruction is executed). One of stack is used when the TABP p instruction is executed.
(A) ← (A) + (M(DP))	–	–	Adds the contents of M(DP) to register A. Stores the result in register A. The contents of carry flag CY remains unchanged.
(A) ← (A) + (M(DP))+ (CY) (CY) ← Carry	–	0/1	Adds the contents of M(DP) and carry flag CY to register A. Stores the result in register A and carry flag CY.
(A) ← (A) + n n = 0 to 15	Overflow = 0	–	Adds the value n in the immediate field to register A. The contents of carry flag CY remains unchanged. Skips the next instruction when there is no overflow as the result of operation.
(CY) ← 1	–	1	Sets (1) to carry flag CY.
(CY) ← 0	–	0	Clears (0) to carry flag CY.
(CY) = 0 ?	(CY) = 0	–	Skips the next instruction when the contents of carry flag CY is "0."
(A) ← ($\overline{A}$)	–	–	Stores the one's complement for register A's contents in register A.
→ CY → $A_3A_2A_1A_0$ ┘	–	0/1	Rotates 1 bit of the contents of register A including the contents of carry flag CY to the right.
Logic operation instruction XOR, OR, AND	–	–	Execute the logic operation selected by logic operation selection register LO between the contents of register A and register E, and stores the result in register A.

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j = 0 to 3
(Mj(DP)) = 0 ? j = 0 to 3
(A) = (M(DP)) ? (A) = n ? n = 0 to 15
$(PC_L) \leftarrow a_6$–a_0 $(PC_H) \leftarrow p$ $(PC_L) \leftarrow a_6$–a_0 (Note) $(PC_L) \leftarrow (a_6$–a_4, A_3–$A_0)$ $(PC_H) \leftarrow p$ $(PC_L) \leftarrow (a_6$–a_4, A_3–$A_0)$ (Note)

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(Mj(DP)) = 0 j = 0 to 3	–	Skips the next instruction when the contents of bit j (bit specified by the value j in the immediate field) of M(DP) is "0."
(A) = (M(DP))	–	Skips the next instruction when the contents of register A is equal to the contents of M(DP).
(A) = n n = 0 to 15	–	Skips the next instruction when the contents of register A is equal to the value n in the immediate field.
–	–	Branch within a page : Branches to address a in the identical page.
–	–	Branch out of a page : Branches to address a in page p.
–	–	Branch within a page : Branches to address (a_6 a_5 a_4 A_3 A_2 A_1 A_0) determined by replacing the low-order 4 bits of the address a in the identical page with register A.
–	–	Branch out of a page : Branches to address (a_6 a_5 a_4 A_3 A_2 A_1 A_0) determined by replacing the low-order 4 bits of the address a in page p with register A.

(SK(SP)) ← (PC) (SP) ← (SP) + 1 (PC_H) ← p (PC_L) ← a_6–a_0 (Note)	–	–	Call the subroutine : Calls the subroutine at address a in page p.
(SK(SP)) ← (PC) (SP) ← (SP) + 1 (PC_H) ← p (PC_L) ← (a_6–a_4, A_3–A_0) (Note)	–	–	Call the subroutine : Calls the subroutine at address (a_6 a_5 a_4 A_3 A_2 A_1 A_0) determined by replacing the low-order 4 bits of address a in page p with register A.
(PC) ← (SK(SP)) (SP) ← (SP) – 1	–	–	Returns from subroutine to the routine called the subroutine.
(PC) ← (SK(SP)) (SP) ← (SP) – 1	Skip at uncondition	–	Returns from subroutine to the routine called the subroutine, and skips the next instruction at uncondition.
(B) ← ($T1_7$–$T1_4$) (A) ← ($T1_3$–$T1_0$)	–	–	Transfers the contents of timer 1 to registers A and B.
at timer 1 stop ($V1_0$=0) ($R1_7$–$R1_4$) ← (B), ($R1_3$–$R1_0$) ← (A) ($T1_7$–$T1_4$) ← (B), ($T1_3$–$T1_0$) ← (A) at timer 1 operating ($V1_0$=1) ($R1_7$–$R1_4$) ← (B), ($R1_3$–$R1_0$) ← (A)	–	–	Transfers the contents of registers A and B to timer 1.
($V1_2$–$V1_0$) ← (A_2–A_0)	–	–	Transfers the contents of register A to registers V1.
(T1F) = 1 ? After skipping the next instruction (T1F) ← 0	(T1F) = 1	–	Skips the next instruction when the contents of T1F flag is “1.” After skipping, clears (0) to T1F flag.
(A_2–A_0) ← (C_2–C_0)	–	–	Transfers the contents of register A to register C.
(C_2–C_0) ← (A_2–A_0), (CARR) ← 0	–	–	Transfers the contents of register C to register A. In this case, port CARR output latch is cleared to “0.”
(CARR) ← (A_3)	–	–	Transfers the contents of bit 3 (A_3) of register A to port CARR output latch.

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$(D(Y)) \leftarrow 1$ $(Y) = 0$ to 7	–	–	Sets (1) to a bit of port D specified by register Y.
$(D(Y)) = 0$? $(Y) = 7$	$(D(Y)) = 0$ $(Y) = 7$	–	Skips the next instruction when a bit of port D specified by register Y is “0.”
$(E_1, E_0) \leftarrow (A_1, A_0)$	–	–	Outputs the contents of register A to port E.
$(A_2–A_0) \leftarrow (E_2–E_0)$	–	–	Transfers the contents of port E to register A.
$(G) \leftarrow (A)$	–	–	Outputs the contents of register A to port G.
$(A) \leftarrow (G)$	–	–	Transfers the contents of port G to register A.
$(PC) \leftarrow (PC) + 1$	–	–	No operation
RAM back-up	–	–	Puts the system in RAM back-up state.
$(P) = 1$?	$(P) = 1$	–	Skips the next instruction when P flag is “1.” After skipping, P flag remains unchanged.
STCK changes to $f(X_{IN})$	–	–	System clock (STCK) changes to $f(X_{IN})$ from $f(X_{IN})/8$. Execute this CCK instruction at address 0 in page 0.
$(LO_1, LO_0) \leftarrow (A_1, A_0)$	–	–	Transfers the contents of register A to the logic operation selection register LO.
$(URS) \leftarrow 1$	–	–	Sets the most significant ROM code reference enable flag (URS) to “1.”
$(PU0_2–PU0_0) \leftarrow (A_2–A_0)$	–	–	Transfers the contents of register A to register PU0.
$(WDF1) \leftarrow 0$	–	–	Initializes the watchdog timer flag (WDF1).

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CONTROL REGISTERS

Timer control register V1		at reset : 000_2	at RAM back-up : 000_2	W
$V1_2$	Carrier wave output auto-control bit	0	Auto-control output by timer 1 is invalid	
		1	Auto-control output by timer 1 is valid	
$V1_1$	Timer 1 count source selection bit	0	Carrier output (CARRY)	
		1	Bit 5 of watchdog timer (WDT)	
$V1_0$	Timer 1 control bit	0	Stop (Timer 1 state retained)	
		1	Operating	

Pull-down control register PU0		at reset : 000_2	at RAM back-up : state retained	W
$PU0_2$	Port D_7 pull-down control bit	0	Pull-down transistor OFF, input circuit OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, input circuit ON, key-on wakeup valid	
$PU0_1$	Port E_1 pull-down control bit	0	Pull-down transistor OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, key-on wakeup valid	
$PU0_0$	Port E_0 pull-down control bit	0	Pull-down transistor OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, key-on wakeup valid	

Carrier wave selection register C		at reset : 111_2			at RAM back-up : 111_2	R/W
		C_2	C_1	C_0	Carrier wave	
					Frequency	Duty
C_2	Carrier wave selection bits	0	0	0	System clock/12	1/3
		0	0	1	System clock/12	1/2
C_1		0	1	0	System clock/8	1/4
		0	1	1	System clock/8	1/2
		1	0	0	System clock	1/2
C_0		1	0	1	No carrier wave	
		1	1	0	$f(X_{IN})/4$ (Note 2)	1/2
		1	1	1	"L" level fixed	

Logic operation selection register LO		at reset : 00_2		at RAM back-up : 00_2	W
		LO_1	LO_0	Logic operation function	
LO_1	Logic operation selection bits	0	0	Exclusive logic OR operation (XOR)	
		0	1	OR operation (OR)	
LO_0		1	0	AND operation (AND)	
		1	1	Not available	

Notes 1: "R" represents read enabled, and "W" represents write enabled.
2: $f(X_{IN})$ is valid only when $f(X_{IN})/8$ is selected as the system clock.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage		–0.3 to 5	V
V_I	Input voltage		–0.3 to V_{DD}+0.3	V
V_O	Output voltage		–0.3 to V_{DD}+0.3	V
P_d	Power dissipation	Ta = 25 °C	300	mW
T_{opr}	Operating temperature range		–20 to 85	°C
T_{stg}	Storage temperature range		–40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = –20 °C to 85 °C, V_{DD} = 1.8 V to 3.6 V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage		1.8		3.6	V
V_{RAM}	RAM back-up voltage (at RAM back-up mode)		1.4		3.6	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" level input voltage Ports D_7, E, G	V_{DD} = 3 V	0.7V_{DD}		V_{DD}	V
V_{IH}	"H" level input voltage X_{IN}	V_{DD} = 3 V	0.8V_{DD}		V_{DD}	V
V_{IL}	"L" level input voltage Ports D_7, E, G	V_{DD} = 3 V	0		0.2V_{DD}	V
V_{IL}	"L" level input voltage X_{IN}	V_{DD} = 3 V	0		0.2V_{DD}	V
I_{OH}(peak)	"H" level peak output current Ports D, E_1, G	V_{DD} = 3 V			–4	mA
I_{OH}(peak)	"H" level peak output current Port E_0	V_{DD} = 3 V			–24	mA
I_{OH}(peak)	"H" level peak output current CARR	V_{DD} = 3 V			–20	mA
I_{OL}(peak)	"L" level peak output current CARR	V_{DD} = 3 V			4	mA
I_{OH}(avg)	"H" level average output current Ports D, E_1, G	V_{DD} = 3 V			–2	mA
I_{OH}(avg)	"H" level average output current Port E_0	V_{DD} = 3 V			–12	mA
I_{OH}(avg)	"H" level average output current CARR	V_{DD} = 3 V			–10	mA
I_{OL}(avg)	"L" level average output current CARR	V_{DD} = 3 V			2	mA
f(X_{IN})	System clock frequency — when STCK = f(X_{IN})/8 selected	Ceramic resonance			4	MHz
	System clock frequency — when STCK = f(X_{IN}) selected	Ceramic resonance			500	kHz
V_{DET}	Voltage drop detection circuit detection voltage		1.10		1.80	V
		Ta=25 °C	1.40	1.50	1.56	
T_{DET}	Voltage drop detection circuit low voltage determination time	Supply voltage is -10V/s and drops under detected voltage.		0.16	1.2	ms
T_{PON}	Power-on reset circuit valid power source rising time	V_{DD} = 0 to 2.2 V			1	ms

Note: The average output current ratings are the average current value during 100 ms.

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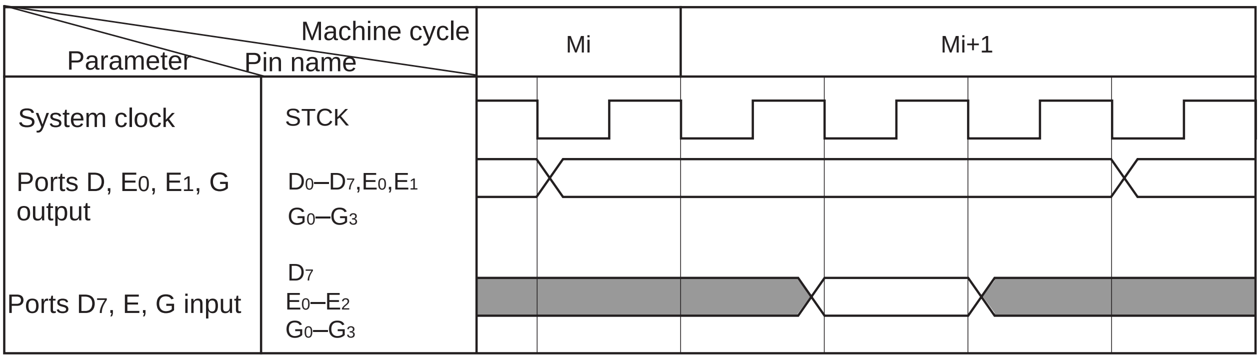
ELECTRICAL CHARACTERISTICS

(Ta = –20 °C to 85 °C, V_{DD} = 3 V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OL}	"L" level output voltage Port CARR	I_{OL} = 2 mA			0.9	V
V_{OH}	"H" level output voltage Ports D, E_1, G	I_{OH} = –2 mA	2.1			V
V_{OH}	"H" level output voltage Port E_0	I_{OH} = –12 mA	1.5			V
V_{OH}	"H" level output voltage CARR	I_{OH} = –10 mA	1.0			V
I_{IL}	"L" level input current Ports D_7, E, G	V_I = V_{SS}			–1	µA
I_{IH}	"H" level input current Ports E_0, E_1	V_I = V_{DD} Pull-down transistor in off-state			1	µA
I_{OZ}	Output current at off-state Ports D, E_0, E_1	V_O = V_{SS}			–1	µA
I_{DD}	Supply current (when operating)	f(X_{IN}) = 4.0 MHz		400	800	µA
		f(X_{IN}) = 500 kHz		350	700	µA
	Supply current (at RAM back-up)			1	3	µA
		Ta = 25 °C		0.1	0.5	µA
R_{PH}	Pull-down resistor value Ports D_7, E, G	V_{DD} = 3 V, V_I = 3 V	75	150	300	kΩ
R_{OSC}	Feedback resistor value between X_{IN}–X_{OUT}		700		3200	kΩ

BASIC TIMING DIAGRAM



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BUILT-IN PROM VERSION

In addition to the mask ROM versions, the 4280 Group has the One Time PROM versions whose PROMs can only be written to and not be erased.
The built-in PROM version has functions similar to those of the mask ROM versions, but it has PROM mode that enables writing to built-in PROM.

Table 10 shows the product of built-in PROM version. Figure 26 and 27 show the pin configurations of built-in PROM versions.
The One Time PROM version has pin-compatibility with the mask ROM version.

Table 10 Product of built-in PROM version

Product	PROM size (× 9 bits)	RAM size (× 4 bits)	Package	ROM type
M34280E1FP	1024 words	32 words	20P2N-A	One Time PROM [shipped in blank]
M34280E1GP	1024 words	32 words	20P2E/F-A	One Time PROM [shipped in blank]

PIN CONFIGURATION (TOP VIEW)

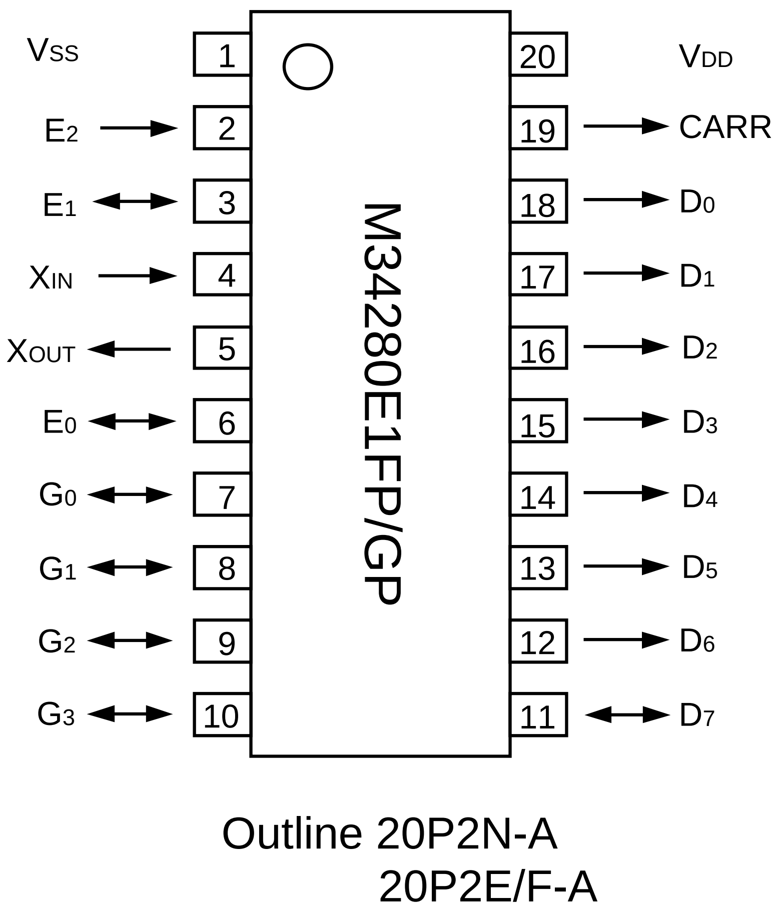


Fig. 26 Pin configuration of built-in PROM version

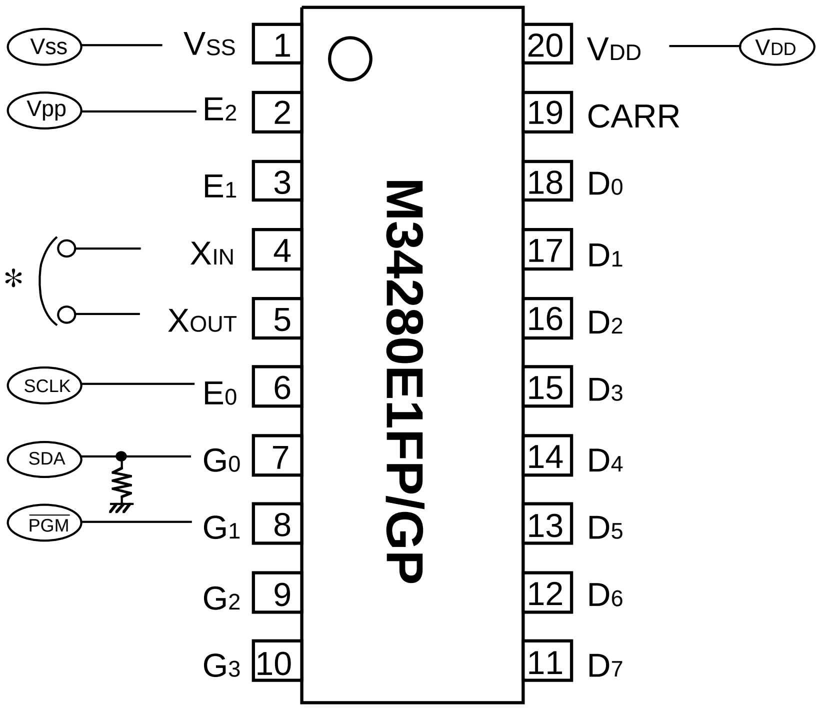
(1) PROM mode (serial input/output)

The M34280E1FP/GP has a PROM mode in addition to a normal operation mode. It has a function to serially input/output the command codes, addresses, and data required for operation (e.g., read and program) on the built-in PROM using only a few pins. This mode can be selected by setting pins SDA (serial data input/output), SCLK (serial clock input), $\overline{PGM}$ and V_{PP} to "H" after connecting wires as shown in Figure 1 and powering on the V_{DD} pin, and then applying 12.5V to the V_{PP} pin.

In the PROM mode, three types of software commands (read, program, and program verify) can be used. Clock-synchronous serial I/O is used, beginning from the LSB (LSB first).

Refer to the Mitsubishi Data Book "DEVELOPMENT SUPPORT TOOLS FOR MICROCOMPUTERS" about the serial programmer for the Mitsubishi single-chip microcomputers.

PIN CONFIGURATION (TOP VIEW)



Outline 20P2N-A
20P2E/F-A

* : connected to the ceramic resonance circuit

Note: The state of disconnected pins are the same as that at reset.

Fig. 27 Pin configuration of built-in PROM version (continued)

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(2) Functional outline

In the PROM mode, data is transferred with the clock-synchronous serial input/output. The input data is read through the SDA pin into the internal circuit synchronously with the rising edge of the serial clock pulse. The output data is output from the SDA pin synchronously with the falling edge of the serial clock pulse. Data is transferred in units of 8 bits.

In the first transfer, the command code is input. Then, address input or data input/output is performed according to the contents of the command code. Table 11 shows the software command used in the PROM mode. The following explains each software command.

Table 11 Software command

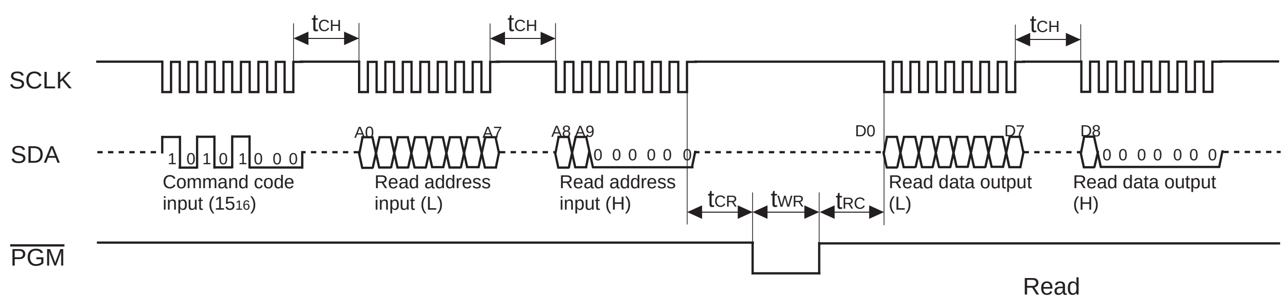
Number of transfer / Command	First command code input	Second	Third	Fourth
Read	15_{16}	Read address L (input)	Read address H (input)	Read data L (output)
Program	25_{16}	Program address L (input)	Program address H (input)	Program data L (input)
Program verify	35_{16}	Program address L (input)	Program address H (input)	Program data L (input)

Number of transfer / Command	Fifth	Sixth	Seventh
Read	Read data H (output)	————	————
Program	Program data H (input)	————	————
Program verify	Program data H (input)	Verify data L (output)	Verify data H (output)

(3) Read

Input the command code 15_{16} in the first transfer. Proceed and input the low-order 8 bits and the high-order 8 bits of the address and pull the $\overline{PGM}$ pin to "L." When this is done, the contents of input address is read and stored into the internal data latch.

When the $\overline{PGM}$ pin is released back to "H" and serial clock is input to the SCLK pin, the low-order 8 bits and high-order 8 bits of read data which have been stored into the data latch, are serially output from the SDA pin.



Note: When outputting the read data, the SDA pin is switched for output at the first falling of the serial clock. The SDA pin is placed in the high-impedance state during the $t_{h(C-E)}$ period after the last rising edge of the serial clock (at the 16th bit).

Fig. 28 Timing at reading

(4) Program

Input command code 25_{16} in the first transfer. Proceed and input the low-order 8 bits and high-order 8 bits of the address and the low-order 8 bits and high-order 8 bits of program data, and pull the $\overline{PGM}$ pin to "L." When this is done, the program data is programmed to the specified address.

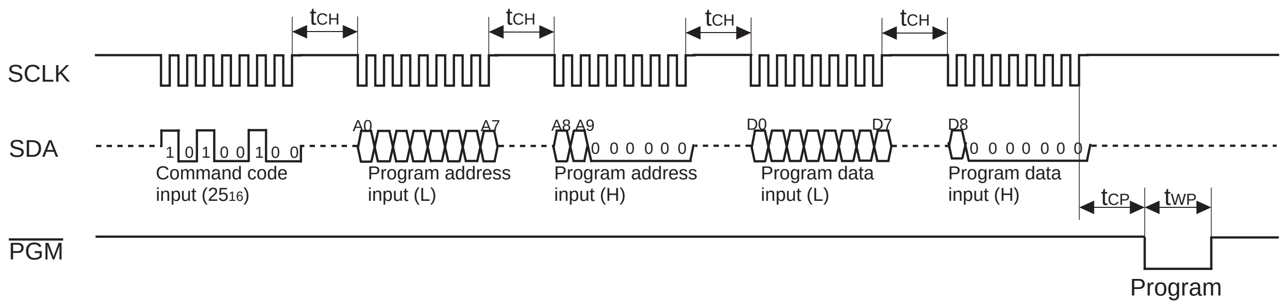
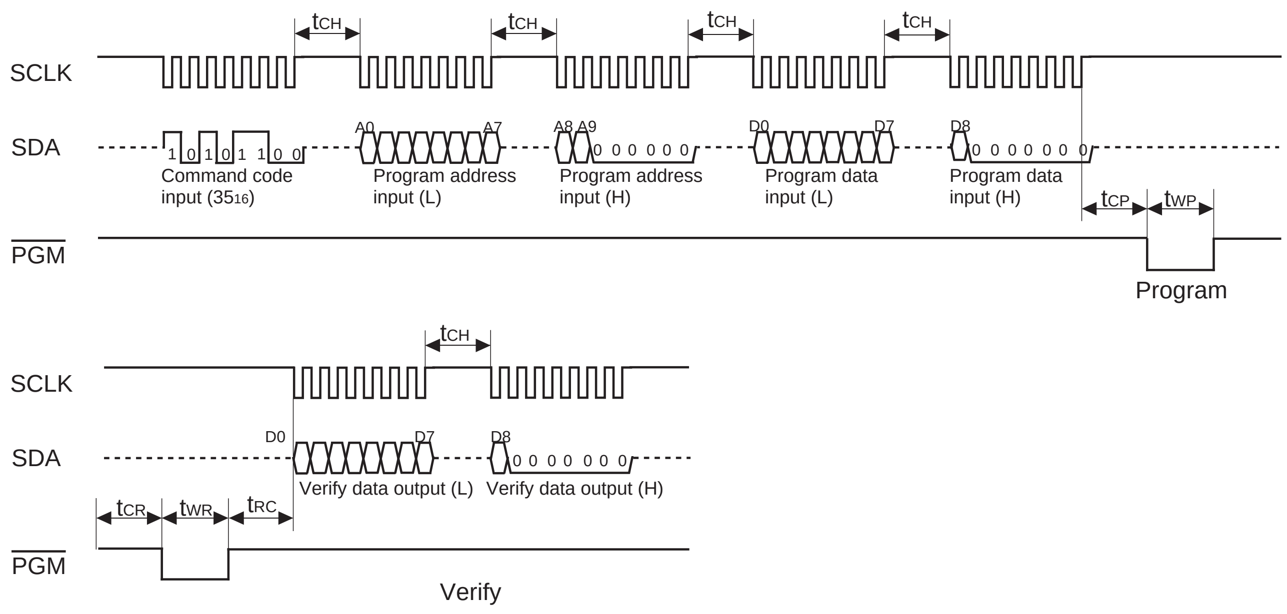


Fig. 29 Timing at programming

(5) Program verify

Input command code 35_{16} in the first transfer. Proceed and input the low-order 8 bits and high-order 8 bits of the address and the low-order 8 bits and high-order 8 bits of program data, and pull the $\overline{PGM}$ pin to "L." When this is done, the program data is programmed to the specified address. Then, when the $\overline{PGM}$ pin is pulled to "L" again after it is released back to "H," the address programmed with the program command is read and verified and stored into the internal data latch. When the $\overline{PGM}$ pin is released back to "H" and serial clock is input to the SCLK pin, the verify data that has been stored into the data latch is serially output from the SDA pin.



Note: When outputting the verify data, the SDA pin is switched for output at the first falling of the serial clock. The SDA pin is placed in the high-impedance state during the $t_{h(C-E)}$ period after the last rising edge of the serial clock (at the 16th bit).

Fig. 30 Timing at program verifying

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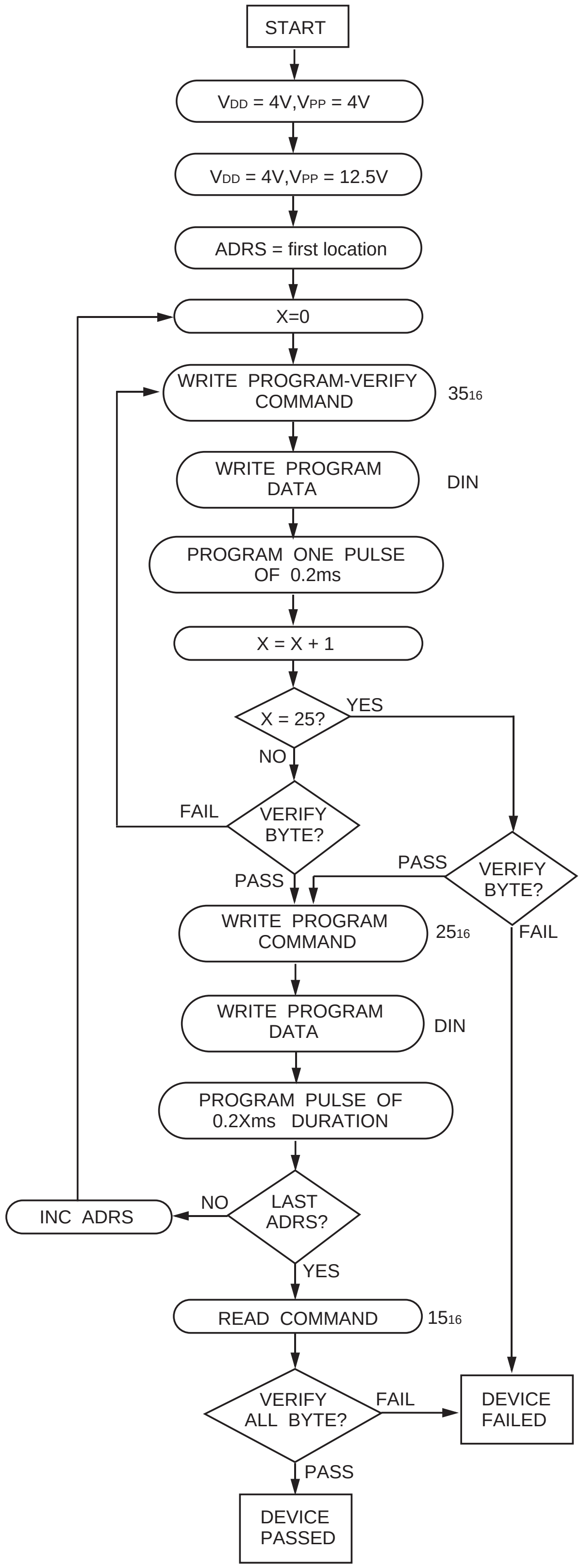
PROGRAM ALGORITHM FLOW CHART

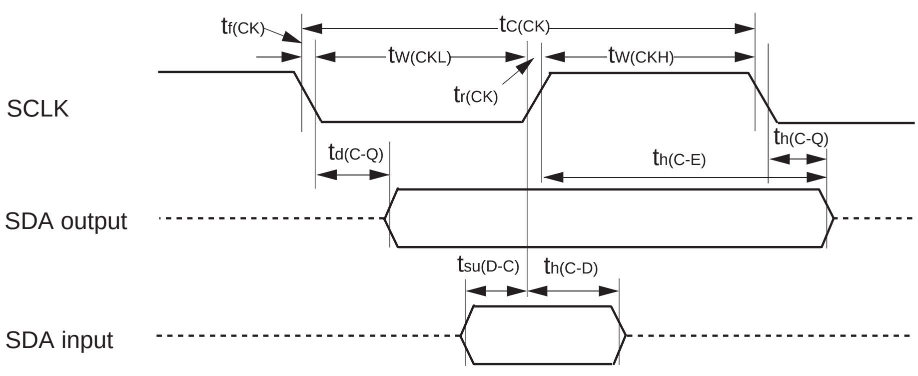


TIMING REQUIREMENT CONDITION AND SWITCHING CHARACTERISTICS

($Ta = 25$ °C, $V_{DD} = 4.0$ V, $V_{PP} = 12.5$ V)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{CH}	Serial transfer width time	2.0		µs
t_{CR}	Read wait time after transfer	2.0		µs
t_{WR}	Read pulse width	500		ns
t_{RC}	Transfer wait time after read	2.0		µs
t_{CP}	Program wait time after transfer	2.0		µs
t_{WP}	Program pulse width	0.19	0.21	ms
t_{OWP}	Added program pulse width	0.19	5.25	ms
$t_{C(CK)}$	SCLK input cycle time	1.0		µs
$t_{W(CKH)}$	SCLK “H” pulse width	450		ns
$t_{W(CKL)}$	SCLK “L” pulse width	450		ns
$t_{r(CK)}$	SCLK rising time	40		ns
$t_{f(CK)}$	SCLK falling time	40		ns
$t_{d(C-Q)}$	SDA output delay time	0	180	ns
$t_{h(C-Q)}$	SDA output hold time	0		ns
$t_{h(C-E)}$	SDA output hold time (only for 16th bit)	100		ns
$t_{su(D-C)}$	SDA input set-up time	60		ns
$t_{h(C-D)}$	SDA input hold time	180		ns

TIMING DIAGRAM



Measurement condition
Output timing voltage: $V_{OL} = 0.8$ V, $V_{OH} = 2.0$ V
Input timing voltage: $V_{IL} = 0.2\ V_{DD}$, $V_{IH} = 0.8\ V_{DD}$

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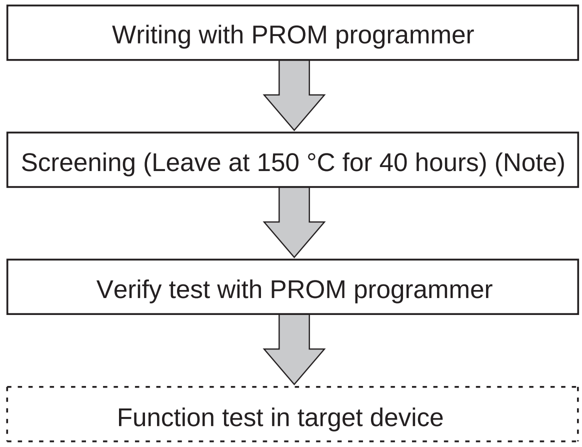
(6) Notes on handling

① A high-voltage is used for writing. Take care that overvoltage is not applied. Take care especially at turning on the power.

② For the M34280E1FP/GP, Mitsubishi Electric corp. does not perform PROM writing test and screening in the assembly process and following processes. In order to improve reliability after writing, performing writing and test according to the flow shown in Figure 31 before using is recommended.



Note: Since the screening temperature is higher than storage temperature, never expose the microcomputer to 150 °C exceeding 100 hours.

Fig. 31 Flow of writing and test of the product shipped in blank

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GZZ-SH54-86B <91A0>

Mask ROM number	

720 SERIES MASK ROM ORDER CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M34280M1-XXXFP/GP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Please fill in all items marked ✻ .

✻ Customer	Company name	TEL ( )
	Date issued	Date:

Issuance signature	Responsible officer	Supervisor

✻ 1. Confirmation

Specify the name of the product being ordered (check in the approximate box).
Three sets of EPROMs are required for each pattern if this order is performed by EPROMs.
One floppy disk is required for each pattern if this order is performed by floppy disk.

Microcomputer name: ☐ M34280M1-XXXFP ☐ M34280M1-XXXGP

☐ Ordering by the EPROMs

Specify the type of EPROMs submitted (check in the approximate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM area ☐☐☐☐ (hexadecimal notation)

EPROM Type:

☐ 27C64	☐ 27C128	☐ 27C256	☐ 27C512
0000_{16}	0000_{16}	0000_{16}	0000_{16}
Low-order 8-bit data (1.00K)	Low-order 8-bit data (1.00K)	Low-order 8-bit data (1.00K)	Low-order 8-bit data (1.00K)
$03FF_{16}$	$03FF_{16}$	$03FF_{16}$	$03FF_{16}$
(shaded)	(shaded)	(shaded)	(shaded)
1000_{16}	1000_{16}	1000_{16}	1000_{16}
Most significant bit data (1.00K)	Most significant bit data (1.00K)	Most significant bit data (1.00K)	Most significant bit data (1.00K)
$13FF_{16}$	$13FF_{16}$	$13FF_{16}$	$13FF_{16}$
(shaded)	(shaded)	(shaded)	(shaded)
$1FFF_{16}$	$3FFF_{16}$	$7FFF_{16}$	$FFFF_{16}$

Set "FF_{16}" in the shaded area.

GZZ-SH54-86B <91A0>

Mask ROM number	

720 SERIES MASK ROM ORDER CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M34280M1-XXXFP/GP
MITSUBISHI ELECTRIC

☐ Ordering by floppy disk

We will produce masks based on the mask files generated by the mask file generating utility. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this mask file. Thus, extreme care must be taken to verify the mask file in the submitted floppy disk.

The submitted floppy disk must be-3.5 inch 2HD type and DOS/V format. And the number of the mask files must be 1 in one floppy disk.

File code									(hexadecimal notation)
Mask file name									.MSK (equal or less than eight characters)

✻ 2. Mark Specification

Mark specification must be submitted using the correct form for the type of package being ordered. Fill out the approximate Mark Specification Form (20P2N-A for M34280M1-XXXFP, 20P2E/F-A for M34280M1-XXXGP) and attach to the Mask ROM Order Confirmation Form.

✻ 3. Comments

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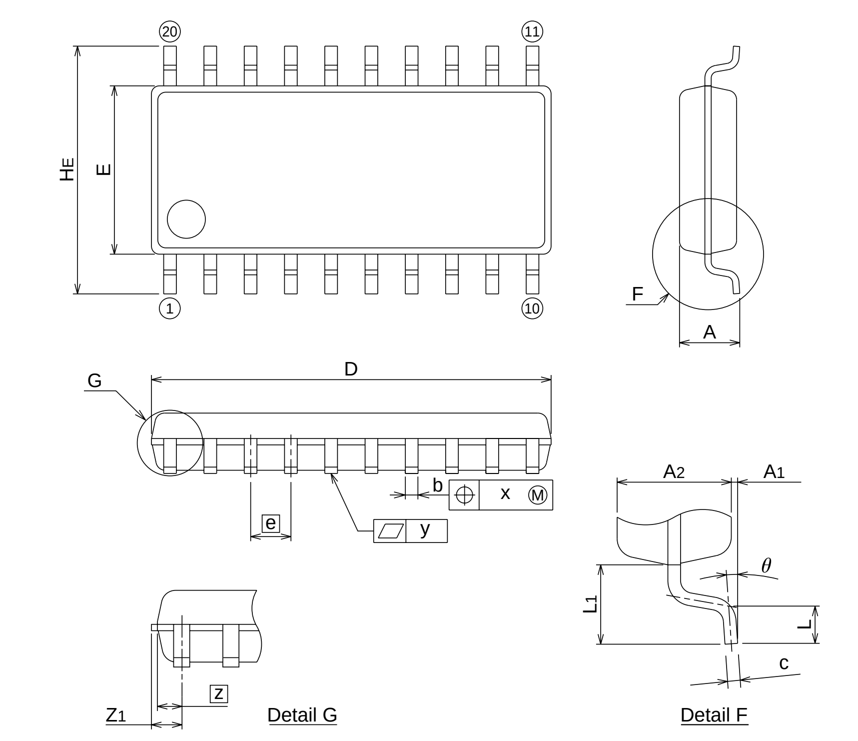
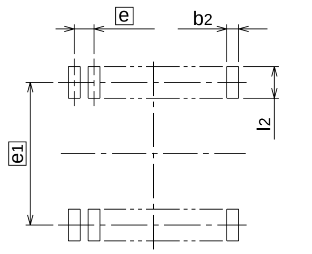
PACKAGE OUTLINE

20P2N-A

Plastic 20pin 300mil SOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOP20-P-300-1.27	–	0.26	Cu Alloy





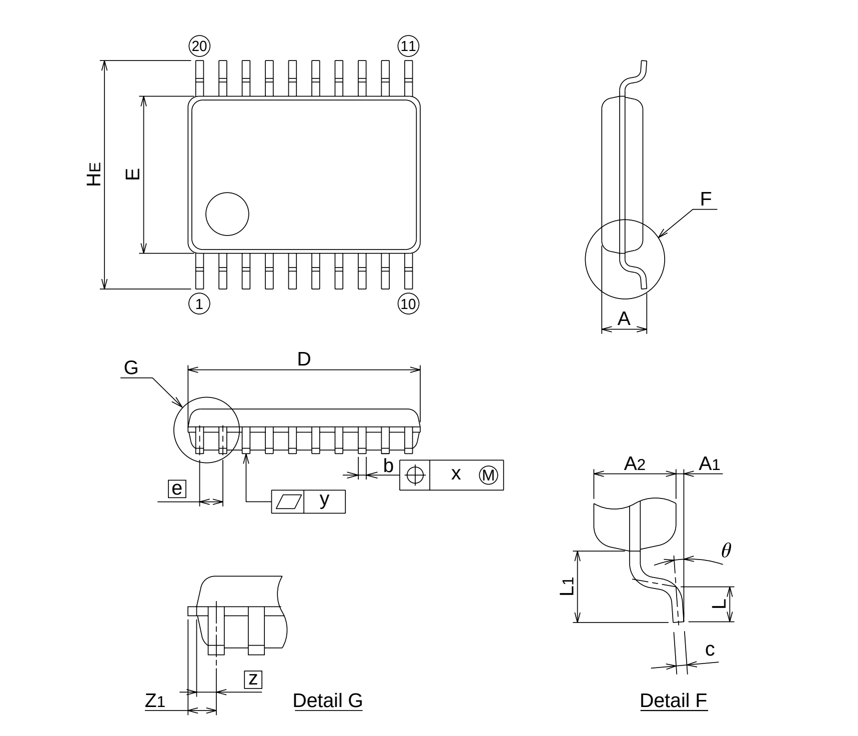
Recommended Mount Pad

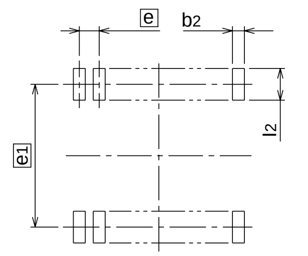
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.1
A_1	0	0.1	0.2
A_2	–	1.8	–
b	0.35	0.4	0.5
c	0.18	0.2	0.25
D	12.5	12.6	12.7
E	5.2	5.3	5.4
e	–	1.27	–
H_E	7.5	7.8	8.1
L	0.4	0.6	0.8
L_1	–	1.25	–
z	–	0.585	–
Z_1	–	–	0.735
x	–	–	0.25
y	–	–	0.1
θ	0°	–	8°
b_2	–	0.76	–
e_1	–	7.62	–
I_2	1.27	–	–

20P2E/F-A

Plastic 20pin 225mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP20-P-225-0.65	–	0.08	Alloy 42/Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.45
A_1	0	0.1	0.2
A_2	–	1.15	–
b	0.17	0.22	0.32
c	0.13	0.15	0.2
D	6.4	6.5	6.6
E	4.3	4.4	4.5
e	–	0.65	–
H_E	6.2	6.4	6.6
L	0.3	0.5	0.7
L_1	–	1.0	–
z	–	0.325	–
Z_1	–	–	0.475
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.35	–
e_1	–	5.8	–
I_2	1.0	–	–

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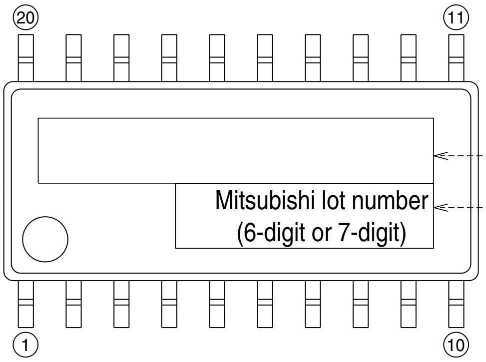
20P2N-A (20-PIN SOP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

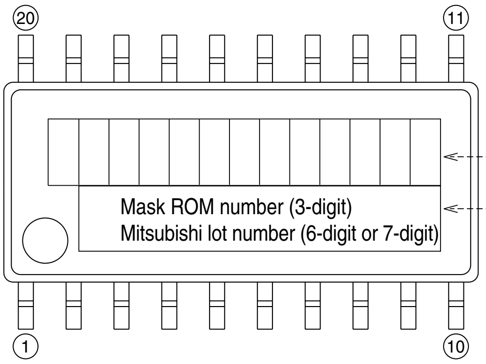
A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi IC Catalog Name



Customer's Parts Number

Note: The fonts and size of characters are standard Mitsubishi type.

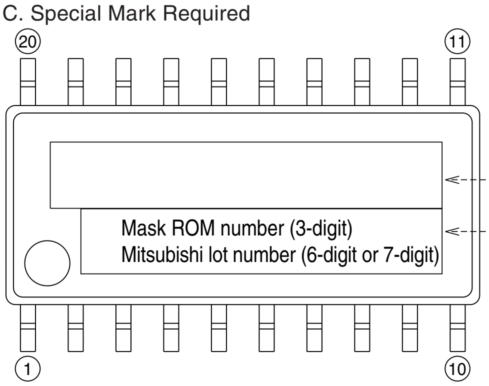
Mitsubishi IC catalog name and Mitsubishi lot number

Notes 1 : The mark field should be written right aligned.

2 : The fonts and size of characters are standard Mitsubishi type.

3 : Customer's Parts Number can be up to 13 characters: Only 0 to 9, A to Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

C. Special Mark Required



Note 1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible.
Mitsubishi lot number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the Special Mark, check the box below.
Please submit a clean original of the logo.
For the new special character fonts, a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

Special Mark (Customer's Trade Mark)

Mitsubishi IC catalog name

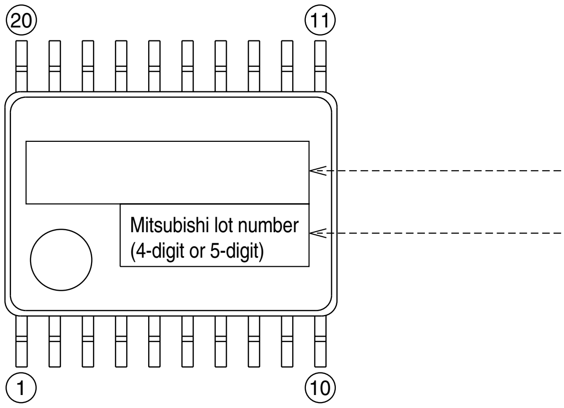
查询"4280"供应商

20P2E/F-A (20-PIN SSOP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

Please choose one of the marking types below (A, B), and enter the Mitsubishi IC catalog name and the special mark (if needed).

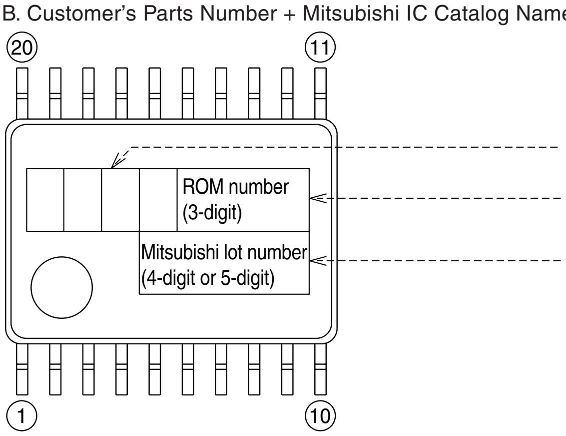
A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi IC Catalog Name



Customer's Parts Number
Note: The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name and Mitsubishi lot number

Mitsubishi IC catalog name and Mitsubishi lot number

Notes 1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's Parts Number can be up to 4 characters: Only 0 to 9, A to Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

RENESAS
Renesas Technology Corp.

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Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

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REVISION DESCRIPTION LIST	4280 GROUP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	980420
2.0	• 20P2E/F-A package added • Figure XA-2: A resistor is added	990611