



4066

CMOS IC

QUAD BILATERAL SWITCH

DESCRIPTION

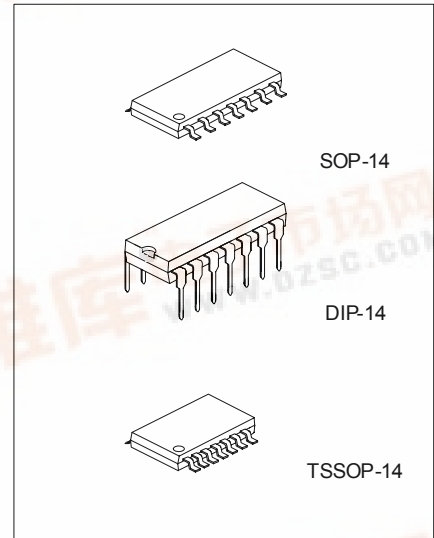
The UTC **4066** is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals.

FEATURES

- * Wide supply voltage range: 3V ~ 15V.
- * High noise immunity : 0.45V_{DD} (typ.)
- * Wide range of digital and ± 7.5V_{PEAK} analog switching
- * "ON" resistance for 15V operation : 80Ω
- * Matched "ON" resistance : R_{ON}=5Ω (typ.) over 15V signal input
- * "ON" resistance flat over peak-to-peak signal range
- * High "ON" / "OFF" : 65 dB (typ.) output voltage ratio @ f_{IS}=10kHz, R_L=10kΩ
- * High degree linearity: 0.1% distortion (typ.) @ f_{IS}=1kHz, V_{IS}=5Vp-p. V_{DD}-V_{SS}=10V, R_L=10kΩ
- * Extremely low "OFF" : 0.1nA (typ.) switch leakage @V_{DD}-V_{SS}=10V, Ta=25
- * Extremely high control input impedance : 10¹²Ω (typ.)
- * Low crosstalk : -50dB (typ.) between switches @ f_{IS}=0.9MHz, R_L=1kΩ
- * Frequency response, switch "ON" : 40MHz (typ.)

ORDERING INFORMATION

Ordering Number		Package	Packing
Normal	Lead Free Plating		
4066-D14-T	4066L-D14-T	DIP-14	Tube
4066-S14-R	4066L-S14-R	SOP-14	Tape Reel
4066-S14-T	4066L-S14-T	SOP-14	Tube
4066-P14-R	4066L-P14-R	TSSOP-14	Tape Reel
4066-P14-T	4066L-P14-T	TSSOP-14	Tube

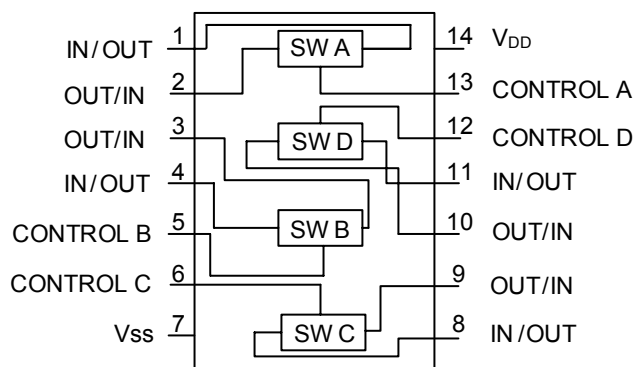


*Pb-free plating product number: 4066L

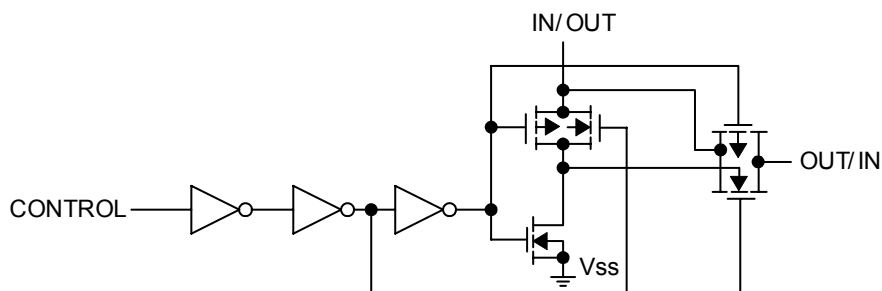
<p>4066L-D14-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Plating</p>	<p>(1) R: Tape Reel, T: Tube (2) D14: DIP-14, S14: SOP-14, P14: TSSOP-14 (3) L: Lead Free Plating Blank: Pb/Sn</p>
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■ PIN CONFIGURATION



■ SCHEMATIC DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (V_{SS}=0V, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V _{DD}	-0.5 ~ +18	V
Input Voltage		V _{IN}	-0.5 ~ V _{CC} +0.5	V
Power Dissipation	DIP-14	P _D	700	mW
	SOP-14		500	mW
	TSSOP-14		500	mW
Junction Temperature		T _J	+125	°C
Storage Temperature		T _{STG}	-40 ~ +150	°C

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V _{DD}	3 ~ 15	V
Input Voltage		V _{IN}	0 ~ V _{DD}	V
Operating Temperature Range		T _{OPR}	-40 ~ +85	°C

■ DC ELECTRICAL CHARACTERISTICS (V_{SS}=0V, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	-40°C		+25°C			+85°C		UNITS	
			MIN	MAX	MIN	TYP	MAX	MIN	MAX		
Quiescent Device Current	I _{DD}	V _{DD} =5V		1.0		0.01	1.0		7.5	μA	
		V _{DD} =10V		2.0		0.01	2.0		15	μA	
		V _{DD} =15V		4.0		0.01	4.0		30	μA	
SIGNAL INPUTS AND OUTPUTS											
Input or Output Leakage Switch "OFF"	I _{IS}	V _C =0		±50		±0.1	±50		±200	nA	
"ON" Resistance	R _{ON}	R _L =10kΩ ~ (V _{DD} -V _{SS} /2)									
		V _C =V _{DD} , V _{SS} ~ V _{DD}									
		V _{DD} =5V		850		270	1050		1200	Ω	
		V _{DD} =10V		330		120	400		520	Ω	
"ON" Resistance Between Any 2 of 4 Switches	R _{ON}	R _L =10kΩ ~ (V _{DD} -V _{SS} /2)									
		V _C =V _{DD} , V _{IS} =V _{SS} ~ V _{DD}									
		V _{DD} =10V				10				Ω	
V _{DD} =15V						5				Ω	
	CONTROL INPUTS										
	Low Level Input Voltage	V _{ILC}	V _{IS} = V _{SS} and V _{DD} V _{OS} =V _{DD} and V _{SS} I _{IS} = ±10μA V _{DD} =5V V _{DD} =10V V _{DD} =15V		1.5 3.0 4.0		2.25 4.5 6.75	1.5 3.0 4.0		1.5 3.0 4.0	V
HIGH Level Input Voltage	V _{IHC}	V _{DD} =5V	3.5		3.5	2.75		3.5		V	
		V _{DD} =10V (Note 4)	7.0		7.0	5.5		7.0		V	
		V _{DD} =15V	11.0		11.0	8.25		11.0		V	
Input Current	I _{IN}	V _{DD} -V _{SS} =15V V _{DD} V _{IS} V _{SS} V _{DD} V _C V _{SS}		±0.3		±10 ⁻⁵	±0.3		±1.0	μA	

■ AC ELECTRICAL CHARACTERISTICS (AC Parameters are guaranteed by DC correlated testing)

(Ta=25 , tr=tf=20 ns and Vss=0V unless otherwise)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time Signal Input to Signal Output	T _{PHL} , T _{PLH}	V _c =V _{DD} , C _L =50pF, (Figure1) R _L =200k	V _{DD} =5V	25	55	ns
			V _{DD} =10V	15	35	ns
			V _{DD} =15V	10	25	ns
Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	t _{PZH} , t _{PLZ}	R _L =1.0kΩ, C _L =50pF (Figure 2, Figure3)	V _{DD} =5V		125	ns
			V _{DD} =10V		60	ns
			V _{DD} =15V		50	ns
Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	t _{PHZ} , t _{PLZ}	R _L =1.0kΩ, C _L =50pF, (Figure 2, Figure3) V _{DD} =5V V _{DD} =10V V _{DD} =15V			125	ns
					60	ns
Sine Wave Distortion	t _{PHZ} , t _{PLZ}	V _c =V _{DD} =5V, V _{ss} = -5V R _L =10kΩ, V _{IS} =5V _{P-P} , f=1kHz, (Figure 4)	0.1		50	%
Frequency Response -Switch "ON" (Frequency at-3dB)			40			MHz
Feedthrough - Switch "OFF" (Frequency at -50 dB)		V _{DD} =5.0V, V _{CC} =V _{SS} = -5.0V, R _L =1kΩ, V _{IS} =5.0V _{P-P} , 20Log ₁₀ , V _{OS} /V _{IS} = -50dB, (Figure 4)		1.25		
Crosstalk Between Any Two Switches(Frequency at-50dB)		V _{DD} =V _C (A)=5.0V; V _{SS} =V _C (B)=5.0V, R _L =1kΩ, V _{IS} (A)=5.0V _{P-P} , 20Log ₁₀ , V _{OS} (B)/V _{IS} (A)= -50dB (Figure 5)		0.9		MHz
Crosstalk; Control Input to Signal Output		V _{DD} =10V, R _L =10kΩ, R _{IN} =1.0kΩ V _{CC} =10V Square Wave, C _L =50pF (Figure 6)		150		mV _{P-P}
Maximum Control Input		R _L =1.0kΩ, C _L =50pF, (Figure 7) V _{OS} (f) =1/2V _{OS} (1.0kHz)	V _{DD} =5.0V	6.0		MHz
			V _{DD} =10V	8.0		MHz
			V _{DD} =15V	8.5		MHz
Signal Input Capacitance	C _{IS}		8.0		pF	
Signal Output Capacitance	C _{OS}	V _{DD} =10V		8.0	pF	
Feedthrough Capacitance	C _{IOS}	V _C =0V		0.5	pF	
Control Input Capacitance	C _{IN}			5.0	7.5	pF

Note 1: These devices should not be connected to circuits with the power "ON"

Note 2: In all cases, there is approximately 5pF of probe and jig capacitance in the output; however, this capacitance is included in C_L wherever it is specified.

Note 3: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_c is the voltage at the control input.

Note 4: Conditions for V_{IHC}: (a) V_{IS}=V_{DD}, I_{OS}=standard B series I_{OH}. (b) V_{IS}=0V, I_{OL}=standard B series I_{OL}

■ SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L =effective external load of the UTC 4066 bilateral switches).This provision avoids any permanent current flow or clamp action of the V_{DD} supply when power is applied or removed from UTC 4066.

In certain applications, the external load-resistor current may include both V_{DD} and Signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1,4,8 or 11,the voltage drop across the bidirectional swith must not exceed 0.6V at $T_a \leq 25$, or 0.4V at $T_a > 25$ (calculated from R_{ON} values shown).

NO V_{DD} current will flow through R_L if the switch current flows into terminals2, 3, 9 or 10.

■ AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS

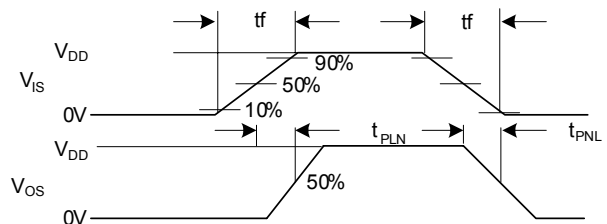
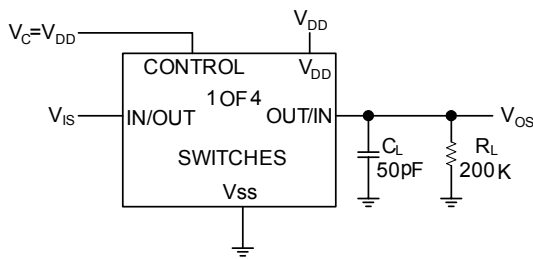


FIGURE 1. t_{PHL} , t_{PLH} Propagation Delay Time Signal Input to Signal Output

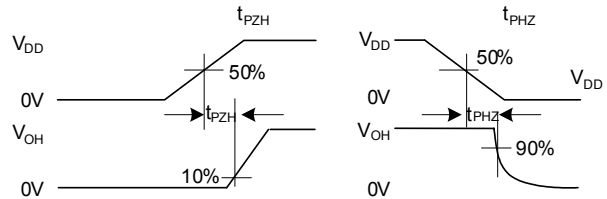
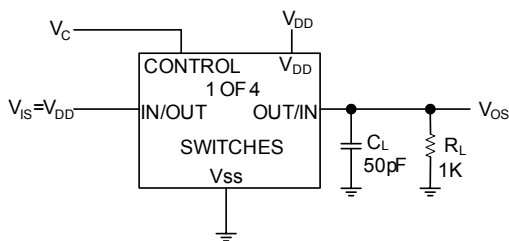


FIGURE 2. t_{PZH} , t_{PHZ} Propagation Delay Time Control to Signal Output

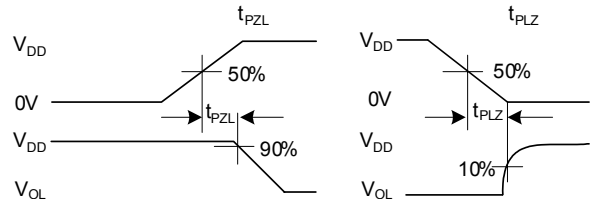
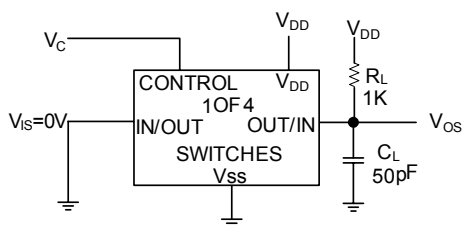
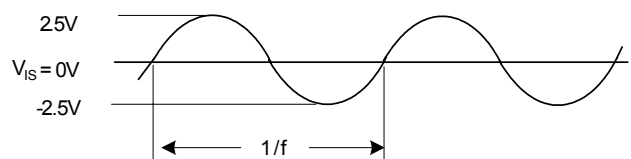
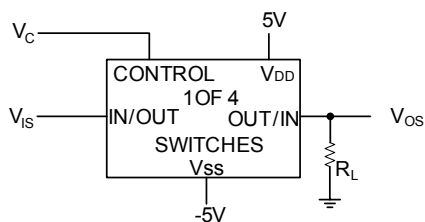


FIGURE 3. t_{PZL} , t_{PLZ} Propagation Delay Time Control to Signal Output



$V_c = V_{DD}$ for distortion and frequency response tests
 $V_c = V_{SS}$ for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

■ AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS(Cont.)

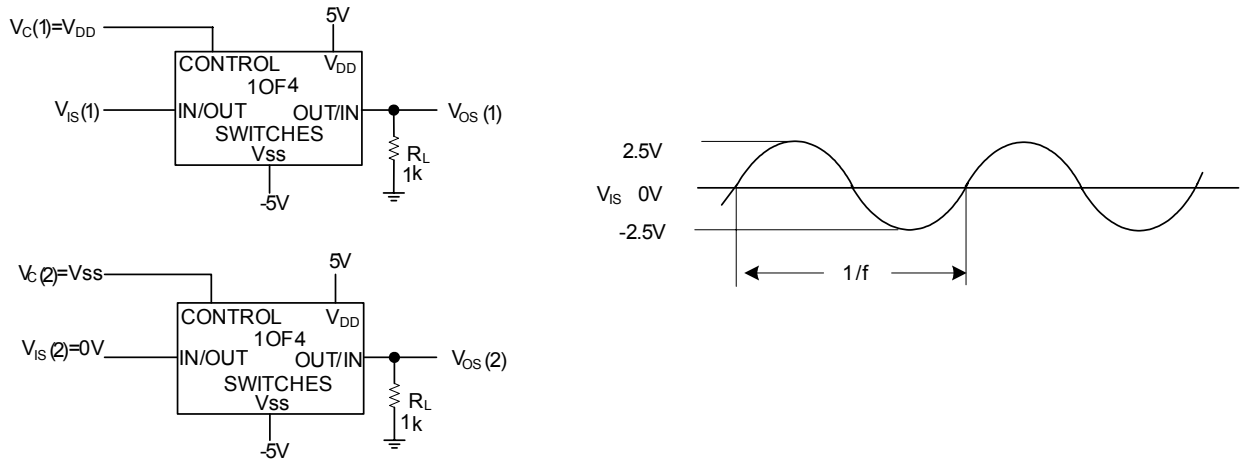


FIGURE 5. Crosstalk Between Any Two Switches

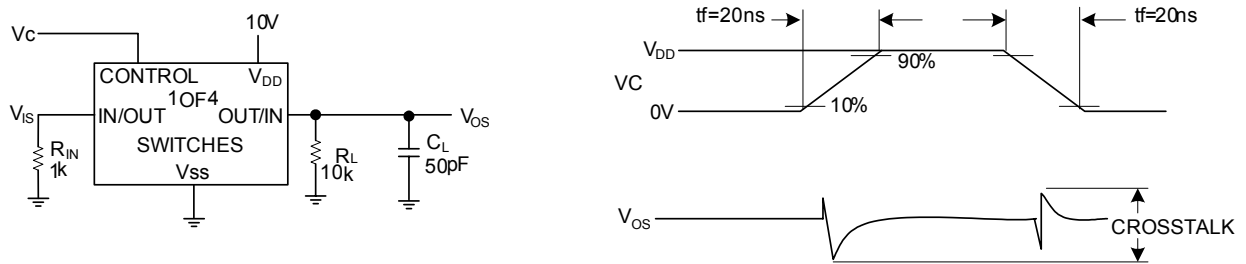


FIGURE 6. Crosstalk: Control Input to Signal Output

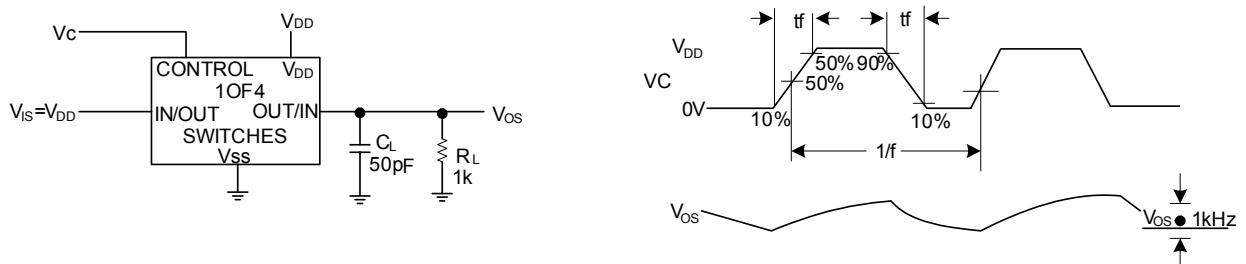
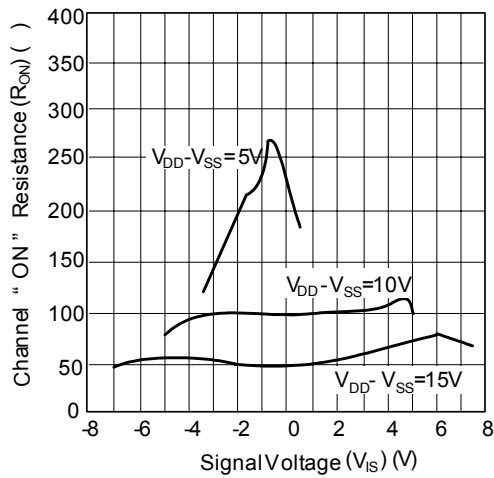


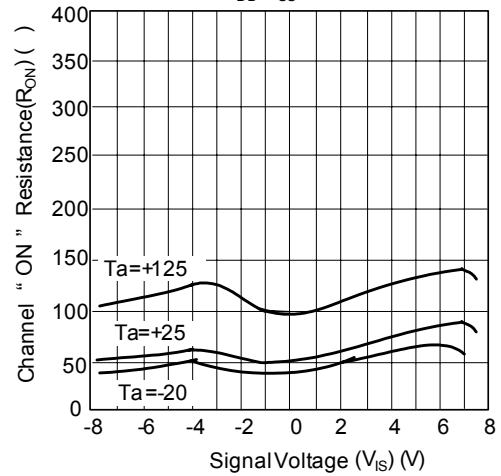
FIGURE 7. Maximum Control Input Frequency

■ TYPICAL PERFORMANCE CHARACTERISTICS

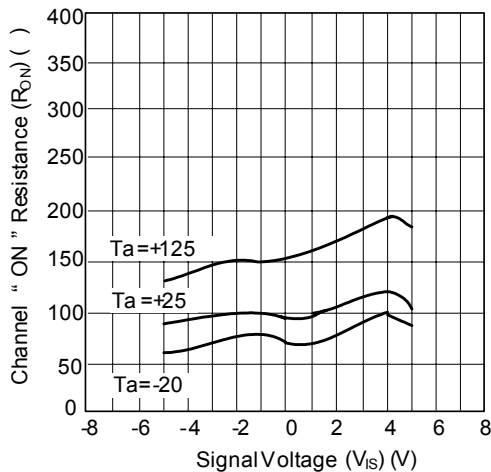
"ON" Resistance vs Signal Voltage for $T_a=25$



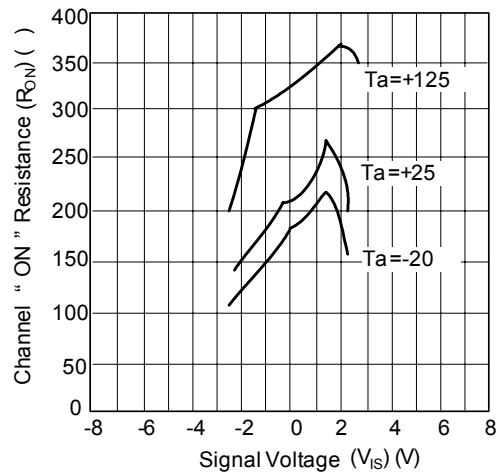
"ON" Resistance as a Function of emperature for $V_{DD}-V_{SS}=15V$



"ON" Resistance as a Function of Temperature for $V_{DD}-V_{SS}=10V$



"ON" Resistance as a Function of Temperature for $V_{DD}-V_{SS}=15V$



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