

SANYO Semiconductors DATA SHEET

LC723661,

CMOS IC

Electronic tuning radio for car audio

ETP Controllers LC723663

Overview

The LC723661, 723662 and 723663 are ETR controllers that can support up to 64KB of ROM and up to 4KB of RAM. These are an 80-pin version of the 100-pin LC723780 series.

They have a built-in serial I/O port and 6-input 8-bit A/D converter to enhance communication with the internal and external devices.

Functions

• ROM : Up to 32K steps (32767×16-bits)

The subroutine area holds 4K steps (4,096×16-bits)

RAM : Up to 8K×4-bits (In banks 00 through 7F)

> LC723661-ROM 32KB, RAM 2KB LC723662-ROM 48KB, RAM 2KB LC723663-ROM 64KB, RAM 4KB

 Stack : 32 levels

• Serial I/O : Two channels. These circuits can support both 2-wire and 3-wire 8-bit communication

> techniques, and can be switched between MSB first and LSB first operation. One of six internally generated serial transfer clock rates can be selected: 12.5kHz,

37.5kHz, 187.5kHz, 281.25kHz, 375kHz, and 450kHz

: Five interrupt inputs (pins INT0, 1, 4, and 5, and the HOLD pin) • External interrupts

These interrupts can be set to switch between rising and falling edges, although the HOLD

pin only supports falling edge detection.

: Six interrupts ; four internal timer interrupts, and two serial I/O interrupts. • Internal interrupts

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查個。ITUP 2500 P 供应商: 11 levels

Interrupts are prioritized in hardware as follows:

HOLD pin>INT0 pin>INT1 pin> INT4 pin>INT5 pin>

S-I/O0>S-I/O1>Internal TMR0>Internal TMR1>Internal TMR2>

Internal TMR3

• A/D Converter : 8-bit resolution and 6 inputs

• General-purpose ports : Input ports : 10

Output ports: 2

I/O ports: 48 (These pins can be switched between input and output in 1-bit units.)

• PLL block : Includes a sub-charge pump for high-speed locking.

Supports dead zone control.

Built-in unlock detection circuit

Twelve reference frequencies: 1kHz, 3kHz, 3.125kHz, 5kHz, 6.25kHz, 9kHz,

10kHz, 12.5kHz, 25kHz, 30kHz, 50kHz, and 100kHz

• Universal counter : This 20-bit counter can be used for either frequency or period measurement and

supports four measurement (calculation) periods: 1ms, 4ms, 8ms, and 32ms

• Timers : Two fixed timers and two programmable timers (8-bit counters)

TMR0 : Supports four periods : 10µs, 100µs, 1ms, and 5ms TMR1 : Supports four periods : 10µs, 100µs, 1ms, and 10ms

TMR2 and TMR3: Programmable 8-bit counters.

Input clocks with 10µs, 100µs, and 1ms

One 125-ms timer flip-flop provided

• Beep circuit : Provides 12 fixed beep tones :

500Hz, 1kHz, 2kHz, 2.08kHz, 2.2kHz, 2.5kHz, 3.33kHz,

3.75kHz, 4.17kHz, and 7.03kHz Programmable 8-bit beep tone generator.

Reference clocks with frequencies of 50kHz, 15kHz, and 5kHz.

• Reset : Built-in voltage detection reset circuit

External reset pin

• Cycle time : 1.33µs/833ns (All instructions are one word), X'tal : 4.5MHz/7.2MHz

(4.5MHz when initialization is to be performed. When 7.2MHz is used, select 4.5MHz

by software.)

• Halt mode : Stops the operation clock of the controller.

There are four conditions that can clear Halt mode : Interrupt requests, timer flip-flop overflows, port PA inputs, and HOLD pin inputs.

• Operating supply voltage: 4.5 to 5.5V (Microcontroller block only: 3.5 to 5.5V)

Package : QIP80EOTP version : LC72F3661

• Development tools : Emulator : RE128V

Evaluation chip : LC72EV3780 Evaluation board : EB-72EV3780

Specificateons"供应商

Absolute Maximum Ratings at Ta = 25°C $V_{SS} = 0V$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} max		-0.3 to +6.5	٧
Input voltage	V _{IN} 1	All input pins	-0.3 to V _{DD} +0.3	٧
Output voltage	V _{OUT} 1	PJ-PORT	-0.3 to +14	٧
	V _{OUT} 2	All input pins other than V _{OUT} 1	-0.3 to V _{DD} +0.3	٧
Output current	I _{OUT} 1	PJ-PORT	0 to 5	mA
	I _{OUT} 2	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PQ, PR, PS-PORT, EO1, EO2	0 to 3	mA
Allowable power dissipation	Pd max	Ta = -40 to +85 °C	400	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-45 to +125	°C

Allowable Operating Range at Ta = -40 to +85°C, $V_{DD} = 3.5$ to 5.5V

Darameter	Symbol	Pins		Ratings			
Parameter	Gymbol		min	typ	mx	uit	
Supply voltage	V _{DD} 1	PLL operation	4.5	5.0	5.5		
	V _{DD} 2	Memory retention	1.1		5.5	V	
	V _{DD} 3	CPU operation	3.5		5.5		
Input high-level voltage	V _{IH} 1	PB, PH, PI, PL, PM, PN, PO, PQ, PR, PS-PORT, HCTR, LCTR	0.7V _{DD}		V _{DD}	٧	
	V _{IH} 2	PD, PE, PF, PG, PK-PORT, LCTR (in period measurement mode), HOLD, RESET	0.8V _{DD}		V _{DD}	V	
	V _{IH} 3	SNS	2.5		V_{DD}	V	
	V _{IH} 4	PA-PORT	0.6V _{DD}		V_{DD}	V	
Input low-level voltage	V _{IL} 1	PB, PH, PI, PL, PM, PN, PO, PQ, PR, PS-PORT, HCTR, LCTR	0		0.3V _{DD}	٧	
	V _{IL} 2	PA, PD, PE, PF, PG, PK-PORT, LCTR (in period measurement mode), RESET	0		0.2V _{DD}	V	
	V _{IL} 3	SNS	0		1.1	V	
	V _{IL} 4	HOLD	0		0.4V _{DD}	V	
Input amplitude	V _{IN} 1	XIN	0.5		1.5	Vrms	
	V _{IN} 2	FMIN	0.07		1.5	Vrms	
	V _{IN} 3	FMIN, AMIN, HCTR, LCTR	0.04		1.5	Vrms	
Input voltage range	V _{IN} 6	ADI0 to ADI7	0		V_{DD}	V	
Input frequency	F _{IN} 1	XIN	4.0	4.5	8.0	MHz	
	F _{IN} 2	FMIN: V _{IN} 2, V _{DD} 1	10		150	MHz	
	F _{IN} 3	FMIN: V _{IN} 3, V _{DD} 1	10		130	MHz	
	F _{IN} 4	AMIN(H): V _{IN} 3, V _{DD} 1	2.0		40	MHz	
	F _{IN} 5	AMIN(L): V _{IN} 3, V _{DD} 1	0.5		10	MHz	
	F _{IN} 6	HCTR: V _{IN} 3, V _{DD} 1	0.4		12	MHz	
	F _{IN} 7	LCTR: V _{IN} 3, V _{DD} 1	100		500	kHz	
	F _{IN} 8	LCTR (in period measurement) : V _{IH} 2, V _{IL} 2, V _{DD} 1	1		20×10 ³	Hz	

Exercise Characteristics in the allowable operating ranges

Parameter	Symbol	Pins	Ratings			unit	
	-,		min	typ	max		
Input high-level current	I _{IH} 1	$XIN: V_I = V_{DD} = 5.0V$	2.0	5.0	15	μΑ	
	I _{IH} 2	FMIN, AMIN, HCTR, LCTR: V _I = V _{DD} = 5.0V	4.0	10	30	μΑ	
	I _{IH} 3	PA, PB, PD, PE, PF, PG, PH, PI, PK, PL, PM, PN, PO, PQ, PR, PS-PORT, SNS, HOLD, RESET, HCTR, LCTR: V _I = V _{DD} = 5.0V (with the ports PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PQ, PR, and PS-PORT set to input mode)			3	μΑ	
Input low-level current	I _{IL} 1	$XIN: V_I = V_{DD} = V_{SS}$	2.0	5.0	15	μΑ	
	I _{IL} 2	FMIN, AMIN, HCTR, LCTR: V _I = V _{DD} = V _{SS}	4.0	10	30	μΑ	
	I _{IL} 3	PA, PB, PD, PE, PF, PG, PH, PI, PK, PL, PM, PN, PO, PQ, PR, PS-PORT, SNS, HOLD, RESET, HCTR, LCTR: VI = VSS (with the ports PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PQ, PR, and PS-PORT set to input mode)			3	μА	
Hysteresis	VH	PD, PE, PF, PG, PK-PORT, RESET, LCTR (in period measurement)	0.1V _{DD}	0.2V _{DD}		٧	
Output high-level voltage	V _{OH} 1	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PQ, PR, PS-PORT: I _O = -1mA	V _{DD} -1.0			٧	
	V _{OH} 2	EO1, EO2: I _O = -500μA	V _{DD} -1.0			V	
	V _{OH} 3	XOUT: I _O = -200μA	V _{DD} -1.0			V	
Output low-level voltage	V _{OL} 1	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PQ, PR, PS-PORT: I _O = -1mA	55		1.0	٧	
	V _{OL} 2	EO1, EO2: I _O = -500μA			1.0	V	
	V _{OL} 3	XOUT : I _O = -200μA			1.5	V	
	V _{OL} 4	PJ-PORT : I _O = -5mA			2.0	V	
Output off leakage current	I _{OFF} 1	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PQ, PR, PS-PORT	-3		+3	μΑ	
	I _{OFF} 2	EO1, EO2	-100		+100	nA	
	I _{OFF} 3	PJ-PORT	-5		+5	μΑ	
A/D conversion error		ADI0 to ADI7	-1.5		+1.5	LSB	
Rejected pulse width	P _{REJ} 1	SNS			50	μs	
Power down detection voltage	V _{DET}		2.7	3.0	3.3	٧	
Power supply current	I _{DD} 1	V _{DD} 1 : F _{IN} 2 = 130MHz Ta = 25°C		5	10	mA	
	I _{DD} 2	V _{DD} 1 : F _{IN} 2 = 130MHz Ta = 25°C		5.5	11	mA	
	I _{DD} 3	V _{DD} 2 : Halt mode Ta = 25°C, X'tal : 4.5 MHz *1 (Fig. 1)		0.45		mA	
	I _{DD} 4	V _{DD} 2 : Halt mode Ta = 25°C, X'tal : 7.2MHz		0.55		mA	
	I _{DD} 5	Backup mode (OSC stopped) VDD = 5.5V, Ta = 25°C *2 (Fig. 2)			5	μΑ	
	I _{DD} 6	Backup mode (OSC stopped) VDD = 2.5V, Ta = 25°C *2 (Fig. 2)			1	μА	

^{*1:} Twenty instruction steps are executed every millisecond. The PLL, universal counter, and other functions are stopped.

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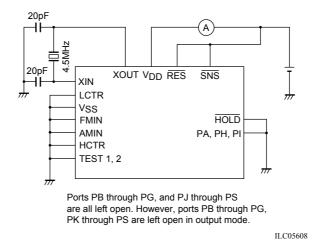


Figure 1. HALT current test condition

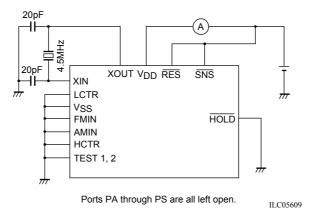
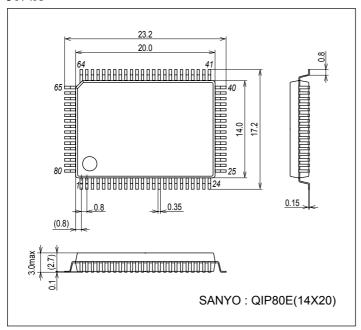


Figure 2. BACK UP current test condition

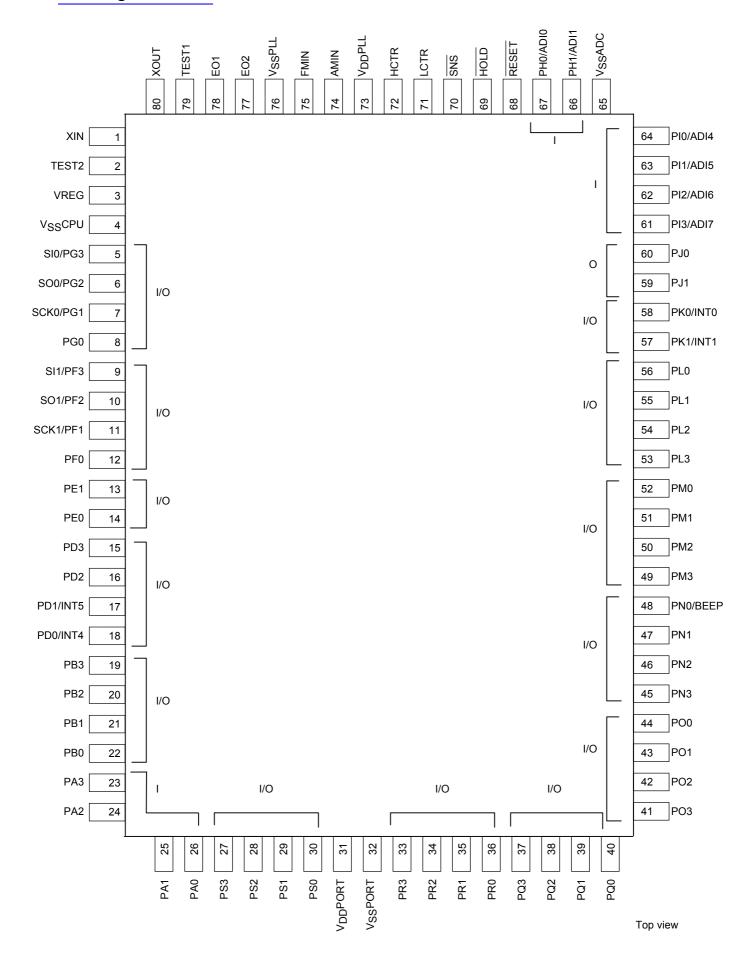
Package Dimensions

unit:mm (typ)

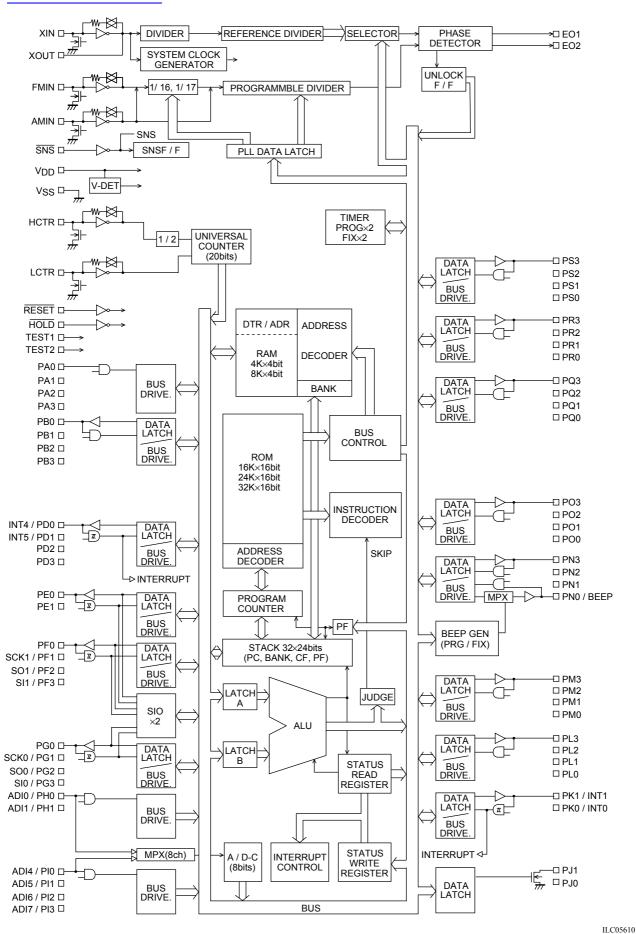
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Pin name	Pin No.	I/O	Pin explanation	Equivalent circuit
PA0	26	I	Dedicated input ports.	BACK UP
PA1	25		These ports are designed with a low threshold voltage.	<u> </u>
PA2	24		Input is disabled in Backup mode.	
PA3	23			į
				! ILC05529
				112003327
PB0	22	I/O	General-purpose I/O ports.	: BACK UP
PB1	21		The mode (input or output) is set using the IOS2 instruction.	L DACK OF
PB2	20		Input is disabled and the pins go to the high-impedance state in	
PB3	19		Backup mode.	
			These ports are set up as general-purpose input ports after a power	5
			on reset.	;
				ILC05530
DD0/INT4	40	1/0	Occasion with the state of the	
PD0/INT4 PD1/INT5	18 17	I/O	General-purpose I/O and external interrupt shared function ports. The input formats are Schmitt inputs.	
PD1/INTS	16		The external interrupt function is enabled when the external interrupt	
PD3	15		enable flag is set.	
			When used as general-purpose I/O ports:	
			The mode (input or output) is set in 1-bit units using the IOS2	
			instruction.	
			When used as external interrupt pins :	
			The external interrupt functions are enabled by setting the	
			corresponding external interrupt enable flag (INT4EN or INT5EN).	
			In this case, the pins must be set to input mode in advance.	
			Input is disabled and the pins go to the high-impedance state in	
			Backup mode.	
			These ports are set up as general-purpose input ports after a power	
			on reset.	
PE0	14	I/O	General-purpose I/O ports	
PE1	13		The input formats are Schmitt inputs.	BACK UP
			The mode (input or output) is set in 1-bit units using the IOS1	\square
			instruction	
			Input is disabled and the pins go to the high-impedance state in	
			Backup mode.	
			These ports are set up as general-purpose input ports after a power	ILC05532
DEO	40	1/0	on reset.	
PF0 PF1/SCK1	12 11	I/O	General-purpose I/O ports with shared functions as serial I/O ports. The input formats are Schmitt inputs.	
PF1/SCK1 PF2/SO1	10		The IOS1 instruction is used to switch between the general-purpose	
PF3/SI1	9		I/O port and serial I/O port functions.	
PG0	8		When used as general-purpose I/O ports:	
PG1/SCK0	7		The pins are set to the general-purpose I/O port function using the	
PG2/SO0	6		IOS1 instruction.	
PG3/SI0	5		The mode (input or output) is set in 1-bit units using the IOS1	
			instruction	
			When used serial I/O ports:	
			The pins are set to the serial I/O port function using the IOS1	
			instruction.	
			[Pin states when set to the serial I/O port function]	
			PF0, PG0 General-purpose I/O	
			PF1, PG1 SCK input or output	
			PF2, PG2 SO output	
			PF3, PG3 SI input	
			Input is disabled and the pins go to the high-impedance state in	
			Backup mode.	
			These ports are set up as general-purpose input ports after a power	
			on reset.	

Pin name	7230012 Pin No.	 	Pin explanation	Equivalent circuit
XIN	1	1	Connections for 4.5MHz/7.2MHz crystal oscillator element	
XOUT	80	0	Connections for 4.5Min2/1.2Min2 crystal oscillator element	XIN XOUT ILC05534
EO1 EO2	78 77	0	Main charge pump outputs. These pins output a high level when the frequency of the local oscillator divided by n is higher than that of the reference frequency, and they output a low level when that frequency is lower. They go to the high-impedance state when the frequencies match. These pins go to the high-impedance state in Backup mode, after a power on reset, and in the PLL stopped state.	ILC05535
V _{DD} PORT	31	-	+ pin of power supply (These pins must connected to VDD.)	
V _{DD} PLL	73		The V _{DD} PORT pin is mainly supply power for the peripheral I/O blocks. The V _{DD} PLL pin is mainly for the PLL circuits and the regulator.	
$V_{SS}CPU$	4		Power supply ground pin (These pins must be connected to ground.)	
V_{SS} PORT	32		The $V_{\mbox{SS}}\mbox{PORT}$ pin is mainly supply power for the peripheral I/O	
$V_{SS}ADC$	65		blocks.	
V _{SS} PLL	76		The V_{SS} PLL pin is mainly for the PLL circuits and the regulator. The V_{SS} CPU pin is mainly used by the CPU block. The V_{SS} ADC pin is mainly used by the ADC block.	
VREG	3	0	Internal low voltage output.	
			Connect a bypass capacitor to this pin.	
FMIN	75	ı	FM VCO (local oscillator) input. This pin is selected with CW1 in the PLL instruction. The signal input to this pin must be capacitor coupled. Input is disabled in Backup mode, after a power on reset, and in the PLL stopped state.	
AMIN	74	I	AM VCO (local oscillator) input. This pin is selected and the band set with CW1 (b1, b0) in the PLL instruction.	
			b1 b0 Band	
			1 0 2 to 40MHz (SW, AM upconversion)	. —466—
			1 1 0.5 to 10MHz (MW, LW)	'**
			The signal input to this pin must be capacitor coupled. Input is disabled in Backup mode, after a power on reset, and in the PLL stopped state.	PLL Stop instruction
HCTR	72	1	Universal counter and general-purpose input shared function input port. The IOS1 instruction is used for switching between the universal counter and general-purpose input functions. • When used for frequency measurement: The universal counter function is set up with the IOS1 instruction. The counter is controlled using UCS and UCC instructions. Since this pin functions as an AC amplifier in this mode, the input signal must be input with capacitor coupling. • When used as a general-purpose input pin: The general-purpose input function is set up with the IOS1 instruction. Data is read from the port using the INR (b0) instruction. Input is disabled in Backup mode. (The input pin will be pulled down.) The universal counter function is selected after a power on reset.	! /// ILC05536

Continued from	m preceding 1/23001 Pin No.	無效音		
			Tim explanation	Equivalent circuit
LCTR	71	I	Universal counter (frequency or period measurement) and general- purpose input shared function input port.	
			The IOS1 instruction is used for switching between the universal	
			counter and general-purpose input functions.	
			When used for frequency measurement :	
			The universal counter function is set up with the IOS1 instruction.	
			Set up LCTR frequency measurement mode with the UCS	
			instruction, and control operation with the UCC instruction.	· ——W——
			Since this pin functions as an AC amplifier in this mode, the input	"
			signal must be input with capacitor coupling.	
			When used for period measurement :	
			The universal counter function is set up with the IOS1 instruction.	
			Set up LCTR frequency measurement mode with the UCS	→ PLL Stop instruction
			instruction, and control operation with the UCC instruction.	: 777 ILC05536
			Since the bias feedback resistor is disconnected in this mode, the	
			input signal must be input with DC coupling.	
			When used as a general-purpose input pin:	
			The general-purpose input port function is set up with the IOS1	
			instruction.	
			Data is read from the port using the INR (b1) instruction.	
			Input is disabled in Backup mode. (The input pin will be pulled down.)	
			The universal counter function (HCTR frequency measurement mode)	
			is selected after a power on reset.	
SNS	70	I	Voltage sense and general-purpose input shared function port.	
			This input circuit is designed with a low input threshold voltage.	
			When used as a voltage sense input :	
			The pin is used to test for power failures on the return from Backup mode.	
			Application can test this condition using the internal SNS flip-flop.	
			The SNS flip-flop can be tested with the TST instruction.	1
			(This usage requires external components, capacitors and resistors.	□ ———
			For the sample application circuit, see the user's manual.)	ILC05539
			When used as a general-purpose input port :	11.003339
			When used as a general-purpose input port the pin state can be	
			tested with the TST instruction.	
			Unlike the other input ports, input to this pin is not disabled in Backup	
			mode and after a power on reset. As a result, through currents must	
			be taken into account when designing applications that use this pin as	
			a general-purpose input.	
HOLD	69	1	Power supply monitor (with interrupt function)	
			This is designed with a high input threshold voltage.	
			This pin is normally connected to the ACC line and used for power off	1
			detection.	<u> </u>
			When a power off state is detected, the HOLDON flag and the hold	∀
			interrupt request flag will be set.	ILC05539
			To enter Backup mode, execute a CKSTP instruction when the HOLD	
			pin is low. Set this pin high to clear Backup mode.	
RESET	68	- 1	System reset pin.	
			When the CPU is operating or in Halt mode, the system is reset when	1
			this pin is held low for at least one machine cycle. Execution starts	┆───≧ ≫───
			with the PC pointing to location 0. At this time the SNS flip-flop is set.	ILC05540
			A low level must be applied for at least 50ms when power is first	11.003340

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			T III OADIGITATION	Equivalent circuit
PH0/ADI0	67	I	General-purpose input and A/D converter input shared function ports.	
PH1/ADI1	66		The IOS1 instruction is used to switch between the general-purpose	
PI0/ADI4	64		input and the A/D converter input functions.	
PI1/ADI5	63		When used as general-purpose input ports:	
PI2/ADI6	62		The general-purpose input port function is set up with the IOS1	
PI3/ADI7	61		instruction. (In bit units)	
			When used as A/D converter input pins :	BACK UP
			The A/D converter input port function is set up with the IOS1	
			instruction. (In bit units)	To the
			The pin whose voltage is to be converted is specified with the IOS1	A/D converter input
			instruction, and the conversion is started with UCC instruction.	H 005541
			Note: Since input is disabled for ports specified for the ADI function,	ILC05541
			executing an input instruction for such a port will always return	
			a low level.	
			Input is disabled in Backup mode.	
			These ports are set up as general-purpose input ports after a power	
			on reset.	
PJ0	60	0	General-purpose output ports (high-voltage output)	
PJ1	59		Since these are open-drain output circuits, external pull-up resistors	BACK UP
			are required.	
			The internal transistors are turned off (resulting in a high-level output)	
			in Backup mode and after a power on reset.	<i> </i>
				ILC05542
PK0/INT0	58	I/O	General-purpose I/O and external interrupt shared function ports.	
PK1/INT1	57		The input formats are Schmitt inputs.	
1 10////	01		The external interrupt function is enabled when the external interrupt	
			enable flag is set.	
			When used as general-purpose I/O ports :	
			The mode (input or output) is set in 1-bit units using the IOS1	BACK UP
			instruction.	$\Box \qquad \qquad \downarrow \qquad \qquad \qquad \downarrow \qquad \qquad \qquad \downarrow \qquad \qquad \qquad \downarrow \qquad \qquad \qquad \qquad \downarrow \qquad \qquad \qquad \downarrow \qquad \qquad \qquad \qquad \downarrow \qquad \qquad \qquad \downarrow \qquad \qquad \qquad \qquad \downarrow \qquad \qquad \qquad \downarrow \qquad \qquad \qquad \qquad \qquad \downarrow \qquad $
			When used as external interrupt pins :	
			The external interrupt functions are enabled by setting the	
			· · · · · · · · · · · · · · · · · · ·	
			corresponding external interrupt enable flag (INTOEN through	ILC05543
			INT3EN). Here, the pins must be set to input mode in advance.	
			Input is disabled and the pins go to the high-impedance state in	
			Backup mode.	
			These ports are set up as general-purpose input ports after a power	
			on reset.	
PL0 to 3	56 to 53	I/O	General-purpose I/O ports	
PM0 to 3	52 to 49		The mode is switched between input and output with the IOS	
			instruction.	
			Input is disabled and the pins go to the high-impedance state in	
			Backup mode.	
			These ports are set up as general-purpose input ports after a power	
			on reset.	
PN0/BEEP	48	I/O	General-purpose I/O port and beep tone output shared function ports.	I BACKUB
PN1	47		The IOS2 instruction is used to switch between the general-purpose	BACK UP
PN2	46		I/O port and the beep tone output functions.	
PN3	45		When used as general-purpose I/O ports:	
			The general-purpose I/O port function is set up with the IOS2	
			instruction.	
			(Pins PN1 through PN3 are dedicated general-purpose output pins.)	ILC05544
			When used as the beep tone output pin:	
			The beep tone output function is set up with the IOS2 instruction.	
			The frequency is set up with the BEEP instruction.	
			When this pin is used as the beep tone output pin, executing an	
			output instruction for this pin only sets the internal latch and has no	
]		influence on the output.	
			Input is disabled and the pins go to the high-impedance state in	
			Backup mode.	
			These ports are set up as general-purpose input ports after a power	
			on reset.	
				Continued on next nego

Continued from preceding page						
早in name	7 2300 I Pin No.	六份 ⁶	Pin explanation	Equivalent circuit		
P00	44	I/O	General-purpose I/O ports			
P01	43		The mode is switched between input and output with the IOS			
P02	42		instruction.			
P03	41		Input is disabled and the pins go to the high-impedance state in			
			Backup mode.			
			These ports are set up as general-purpose input ports after a power on reset.	BACK UP		
PQ0 to 3	40 to 37	I/O	General-purpose I/O ports.			
PR0 to 3	36 to 33		The mode is switched between input and output with the IOS			
PS0 to 3	30 to 27		instruction, and data is input with the INR instruction and output with			
			the OUTR instruction.			
			The SPB, RPB, TPT, and TPF instruction cannot be used with these	ILC05544		
			ports.			
			Input is disabled and the pins go to the high-impedance state in			
			Backup mode.			
			These ports are set up as general-purpose input ports after a power			
			on reset.			
TEST1	79		LSI test pins.			
TEST2	2		These pins must be connected to GND.			

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