

MSM5416126A

131,072-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The OKI MSM5416126A is a 128K-word × 16-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM5416126A achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM5416126A has conventional two $\overline{\text{CAS}}$ type 256K × 16 DRAM compatible pinout. The MSM5416126A is available in a 40-pin plastic SOJ or 44/40-pin plastic TSOP.

FEATURES

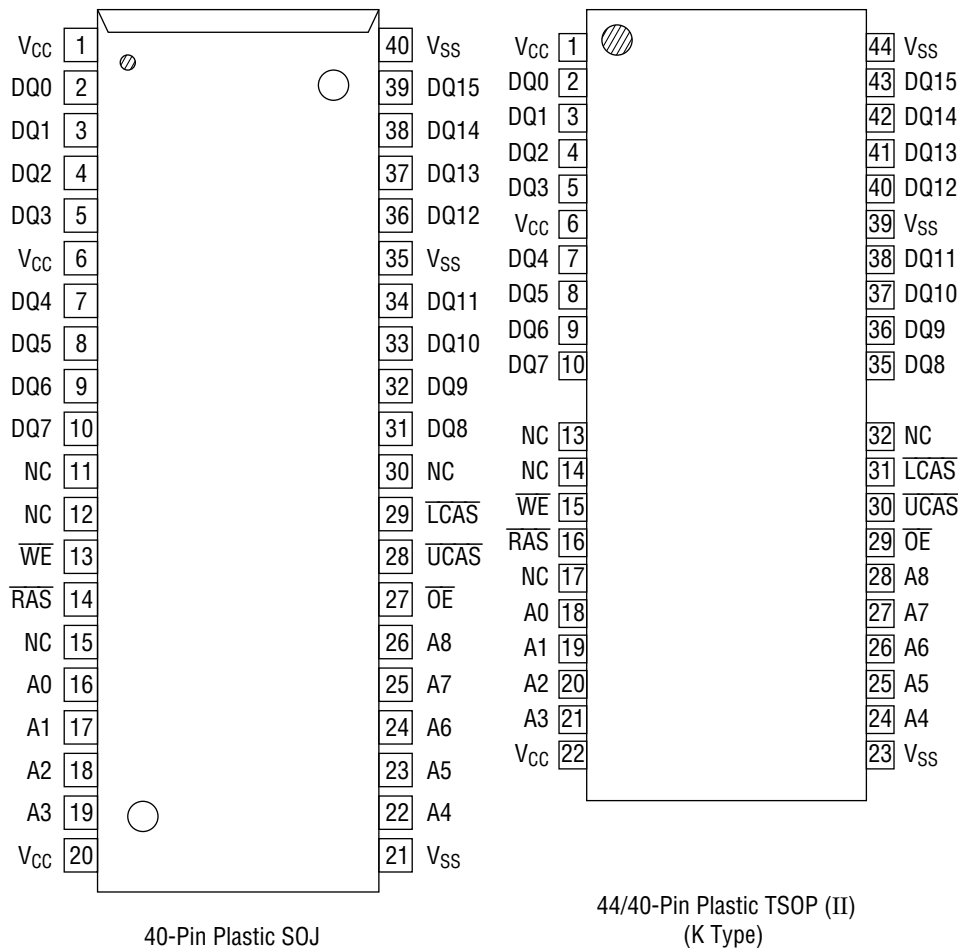
- Fast Page Mode with Extended Data Out
- Byte wide control: 2 $\overline{\text{CAS}}$ control
- 131,072-word × 16-bit organization
- Pin compatible with 2 $\overline{\text{CAS}}$ type 256K × 16 DRAM
- Single 5 V power supply, ±10% tolerance
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh, $\overline{\text{RAS}}$ only refresh capability
- Refresh: 512 cycles/8 ms
- Package options:
 - 40-pin 400 mil plastic SOJ (SOJ40-P-400-1.27) (Product : MSM5416126A-xxJS)
 - 44/40-pin 400 mil plastic TSOP (Type II) (TSOPII44/40-P-400-0.80-K) (Product: MSM5416126A-xxTS-K)xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)		Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}	t _{RC}	t _{HPC}	Operating (Max.)	Standby (Max.)
MSM5416126A-40	40 ns	22 ns	14 ns	14 ns	75 ns	20 ns	770 mW	11 mW
MSM5416126A-45	45 ns	24 ns	14 ns	14 ns	85 ns	20 ns	715 mW	
MSM5416126A-50	50 ns	26 ns	14 ns	14 ns	100 ns	22 ns	660 mW	
MSM5416126A-60	60 ns	30 ns	15 ns	15 ns	120 ns	25 ns	605 mW	

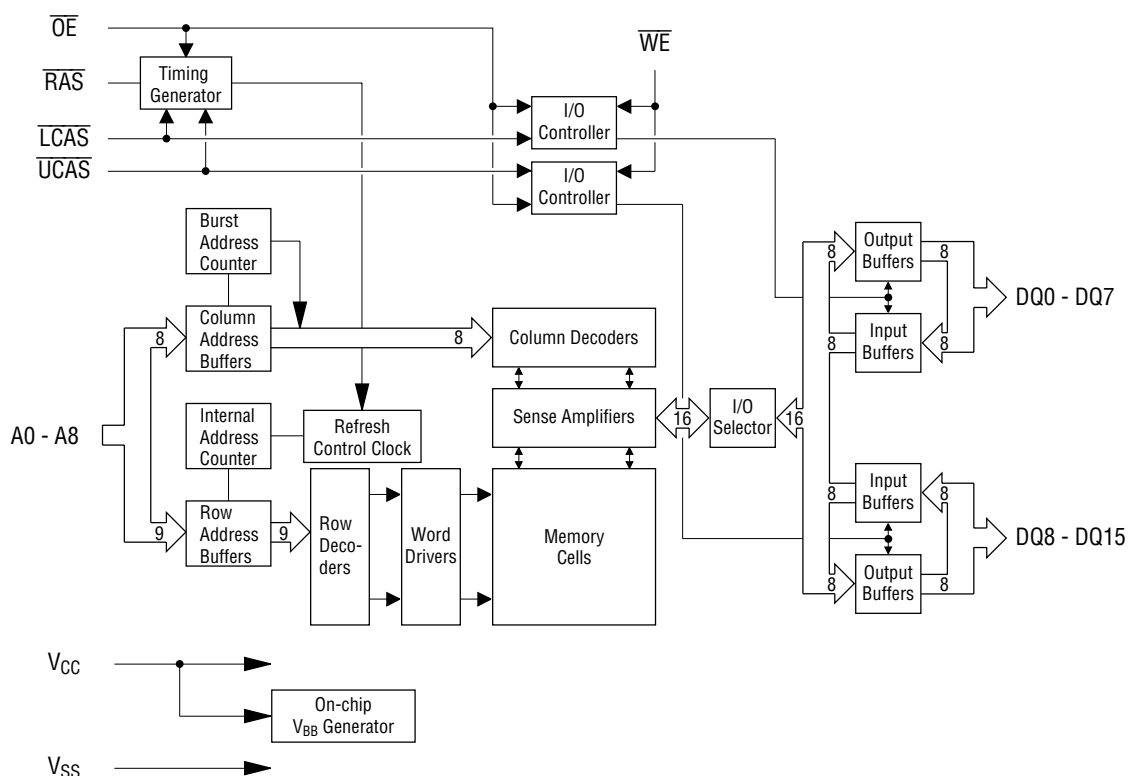
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PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0 - A8	Address Input Row Address : A0 - A8 Column Address : A0 - A7
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{LCAS}}$	Lower Byte Column Address Strobe
$\overline{\text{UCAS}}$	Upper Byte Column Address Strobe
DQ0 - DQ15	Data - Input / Data - Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
V _{CC}	Power Supply (5 V)
V _{SS}	Ground (0 V)
NC	No Connection

Note: The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	DQ0 - DQ7	DQ8 - DQ15	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D _{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D _{OUT}	Upper Byte Read
L	L	L	H	L	D _{OUT}	D _{OUT}	Word Read
L	L	H	L	H	D _{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D _{IN}	Upper Byte Write
L	L	L	L	H	D _{IN}	D _{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

* : "H" or "L"

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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	$T_a = 25^\circ\text{C}$	-1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	$T_a = 25^\circ\text{C}$	50	mA
Power Dissipation	P_D	$T_a = 25^\circ\text{C}$	1	W
Operating Temperature	T_{opr}	—	0 to 70	$^\circ\text{C}$
Storage Temperature	T_{stg}	—	-55 to 150	$^\circ\text{C}$

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

Capacitance

(V_{CC} = 5 V ±10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A8)	C_{IN1}	—	7	pF
Input Capacitance (RAS, LCAS, UCAS, WE, OE)	C_{IN2}	—	7	pF
Output Capacitance (DQ0 - DQ15)	$C_{I/O}$	—	10	pF

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DC Characteristics

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C)

Parameter	Symbol	Condition	MSM5416126A -40		MSM5416126A -45		MSM5416126A -50		MSM5416126A -60		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V _{OH}	I _{OH} = -1.0 mA	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	
Output Low Voltage	V _{OL}	I _{OL} = 1.0 mA	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I _{LI}	0 V ≤ V _I ≤ 6.5 V ; All other pins not under test = 0 V	-10	10	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I _{LO}	DQ _i Disable 0 V ≤ V _O ≤ 5.5 V	-10	10	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ Cycling, t _{RC} = Min.	—	140	—	130	—	120	—	110	mA	1, 2
Power Supply Current (Standby)	I _{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = V _{IH}	—	2	—	2	—	2	—	2	mA	1
Average Power Supply Current (RAS Only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ = Cycling, $\overline{\text{CAS}}$ = V _{IH} , t _{RC} = Min.	—	140	—	130	—	120	—	110	mA	1, 2
Power Supply Current (Standby)	I _{CC5}	$\overline{\text{RAS}}$ = V _{IH} , $\overline{\text{CAS}}$ = V _{IL} , D _{out} = Enable	—	5	—	5	—	5	—	5	mA	1
Average Power Supply Current (CAS before RAS Refresh)	I _{CC6}	$\overline{\text{RAS}}$ = Cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	140	—	130	—	120	—	110	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I _{CC7}	$\overline{\text{RAS}}$ = V _{IL} , $\overline{\text{CAS}}$ Cycling, t _{PC} = Min.	—	130	—	130	—	120	—	110	mA	1, 3

- Notes :
- Specified values are obtained with output open.
 - Address can be changed once or less while $\overline{\text{RAS}}$ = V_{IL}.
 - Address can be changed once or less while $\overline{\text{CAS}}$ = V_{IH}.

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AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM5416126A -40		MSM5416126A -45		MSM5416126A -50		MSM5416126A -60		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	75	—	85	—	100	—	120	—	ns	
Read Modify Write Cycle Time	t _{RWC}	115	—	130	—	145	—	165	—	ns	
Hyper Page Mode Cycle Time	t _{HPC}	20	—	20	—	22	—	25	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	60	—	60	—	65	—	80	—	ns	
Access Time from RAS	t _{RAC}	—	40	—	45	—	50	—	60	ns	4, 9, 10
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	14	—	14	—	14	—	15	ns	4, 9
Access Time from Column Address	t _{AA}	—	22	—	24	—	26	—	30	ns	4, 10
Access Time from $\overline{\text{OE}}$	t _{QEA}	—	14	—	14	—	14	—	15	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	26	—	27	—	29	—	34	ns	4, 9, 10
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	0	—	ns	
Data Hold After $\overline{\text{CAS}}$ Low	t _{COH}	3	—	3	—	3	—	3	—	ns	
Output Buffer Turn-off Delay Time	t _{OFF}	3	8	3	8	3	8	3	10	ns	5
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	3	8	3	8	3	8	3	10	ns	5
Transition Time	t _T	2	35	2	35	2	35	2	35	ns	
Refresh Period	t _{REF}	—	8	—	8	—	8	—	8	ms	
RAS Precharge Time	t _{RP}	25	—	30	—	40	—	50	—	ns	
RAS Pulse Width	t _{RAS}	40	10,000	45	10,000	50	10,000	60	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	40	100,000	45	100,000	50	100,000	60	100,000	ns	
RAS Hold Time	t _{RSH}	14	—	14	—	14	—	15	—	ns	
RAS Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	8	—	8	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	5	—	6	—	7	—	8	—	ns	14
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	8	10,000	8	10,000	9	10,000	12	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	40	—	45	—	50	—	60	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	5	—	5	—	ns	12
RAS to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	18	26	18	31	20	36	20	45	ns	9
RAS to Column Address Delay Time	t _{RAD}	12	18	13	21	15	24	15	30	ns	10
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	8	—	8	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	0	—	ns	11
Column Address Hold Time	t _{CAH}	6	—	6	—	8	—	10	—	ns	11
Column Address Hold Time from $\overline{\text{RAS}}$	t _{AR}	30	—	30	—	35	—	45	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	22	—	24	—	26	—	30	—	ns	

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AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM5416126A -40		MSM5416126A -45		MSM5416126A -50		MSM5416126A -60		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	0	—	ns	11
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	0	—	ns	6, 11
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	0	—	ns	6
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	0	—	ns	8, 11
Write Command Hold Time	t _{WCH}	8	—	8	—	9	—	10	—	ns	11
Write Command Pulse Width	t _{WP}	7	—	8	—	9	—	10	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t _{WCR}	30	—	30	—	35	—	45	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEh}	8	—	8	—	9	—	10	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	7	—	8	—	9	—	12	—	ns	13
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	14	—	14	—	14	—	15	—	ns	
Output Buffer Turn-off Delay Time from $\overline{\text{WE}}$	t _{WEZ}	3	15	3	15	3	15	3	15	ns	5
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{CEZ}	3	8	3	8	3	8	3	10	ns	5
Data to $\overline{\text{CAS}}$ Delay Time	t _{DZC}	0	—	0	—	0	—	0	—	ns	
Data to $\overline{\text{OE}}$ Delay Time	t _{DZO}	0	—	0	—	0	—	0	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	0	—	ns	7, 11
Data-in Hold Time	t _{DH}	7	—	8	—	9	—	10	—	ns	7, 11
Data-in Hold Time referenced to $\overline{\text{RAS}}$	t _{DHR}	30	—	30	—	35	—	45	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OED}	8	—	8	—	8	—	10	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	28	—	30	—	32	—	35	—	ns	8
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	38	—	40	—	44	—	50	—	ns	8
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	60	—	65	—	70	—	80	—	ns	8
$\overline{\text{OE}}$ "L" to $\overline{\text{CAS}}$ "H" Lead Time	t _{OCH}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ "H" to $\overline{\text{OE}}$ "L" Lead Time	t _{CHO}	10	—	10	—	10	—	10	—	ns	
Hi-Z Command Pulse Width	t _{OEP}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	0	—	0	—	0	—	0	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	10	—	10	—	10	—	10	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	10	—	10	—	10	—	10	—	ns	12

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- Notes:
1. An initial pause of 200 μ s is required after power-up, followed by any 8 $\overline{\text{RAS}}$ cycles. (Example : $\overline{\text{RAS}}$ -only-refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 1 TTL load and 50 pF. Output timing reference levels are $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
 5. t_{CEZ} (Max.), t_{OFF} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
 6. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 7. These parameters are referenced to $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, leading edge in an early write cycle, and to $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle or a read modify write cycle.
 8. t_{WCS} , t_{CWD} , t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{Min.})$, the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(\text{Min.})$, $t_{RWD} \geq t_{RWD}(\text{Min.})$ and $t_{AWD} \geq t_{AWD}(\text{Min.})$, the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 9. Operation within the $t_{RCD}(\text{Max.})$ limit insures that $t_{RAC}(\text{Max.})$ can be met. $t_{RCD}(\text{Max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{Max.})$ limit, then access time is controlled by t_{CAC} .
 10. Operation within the $t_{RAD}(\text{Max.})$ limit ensures that $t_{RAC}(\text{Max.})$ can be met. $t_{RAD}(\text{Max.})$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD}(\text{Max.})$ limit, then access time is controlled by t_{AA} .
 11. These parameters are determined by the falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, whichever is earlier.
 12. These parameters are determined by the rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, whichever is later.
 13. t_{CWL} should be satisfied by both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
 14. t_{CP} is determined by the time both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are high.
 15. Input levels at the AC testing are 3.0 V/0.5 V.

TIMING WAVEFORM

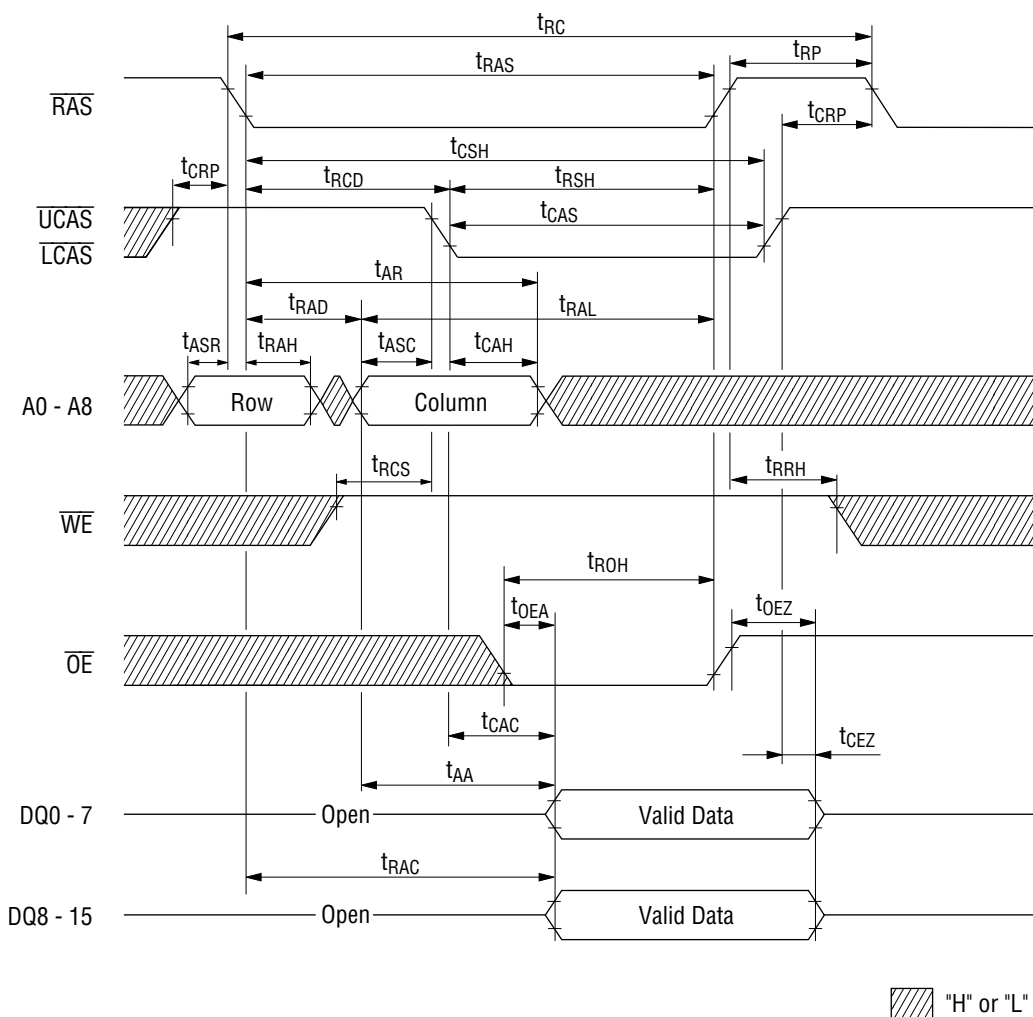
The timing diagram illustrates the relationship between the 64K1602 LCD module and the microcontroller. The signals and their timing parameters are as follows:

- RAS**: Row Address Strobe. Timing parameters include t_{RAS} (high pulse width), t_{CRP} (fall time), t_{RCD} (row-to-column delay), t_{CSH} (high-to-low transition), t_{RSH} (row-to-column delay), t_{CAS} (column address setup), t_{AR} (row address hold), t_{RAD} (row address delay), t_{ASC} (row address setup), t_{CAH} (column address hold), t_{RAL} (row address low), t_{RRH} (row-to-column delay), t_{RRH} (row-to-column delay), t_{RRH} (row-to-column delay).
- UCAS**: User Command Address Strobe. Timing parameter is t_{UCAS} (high pulse width).
- LCAS**: LCD Command Address Strobe. Timing parameter is t_{LCAS} (high pulse width).
- A0 - A8**: Address bus. The diagram shows the **Row** and **Column** address periods.
- WE**: Write Enable. Timing parameter is t_{WE} (high pulse width).
- OE**: Output Enable. Timing parameters include t_{OE} (high pulse width), t_{OEA} (output enable delay), t_{OEZ} (output enable delay), t_{CAC} (column address delay), t_{AA} (address delay), t_{CEZ} (column enable delay), t_{RAC} (row address delay).
- DQ0 - 7**: Data bus (Data 0-7). Timing parameters include t_{DQ0-7} (high pulse width), t_{DQ0-7} (high pulse width), t_{DQ0-7} (high pulse width).
- DQ8 - 15**: Data bus (Data 8-15). Timing parameters include t_{DQ8-15} (high pulse width), t_{DQ8-15} (high pulse width), t_{DQ8-15} (high pulse width).

 "H" or "L"

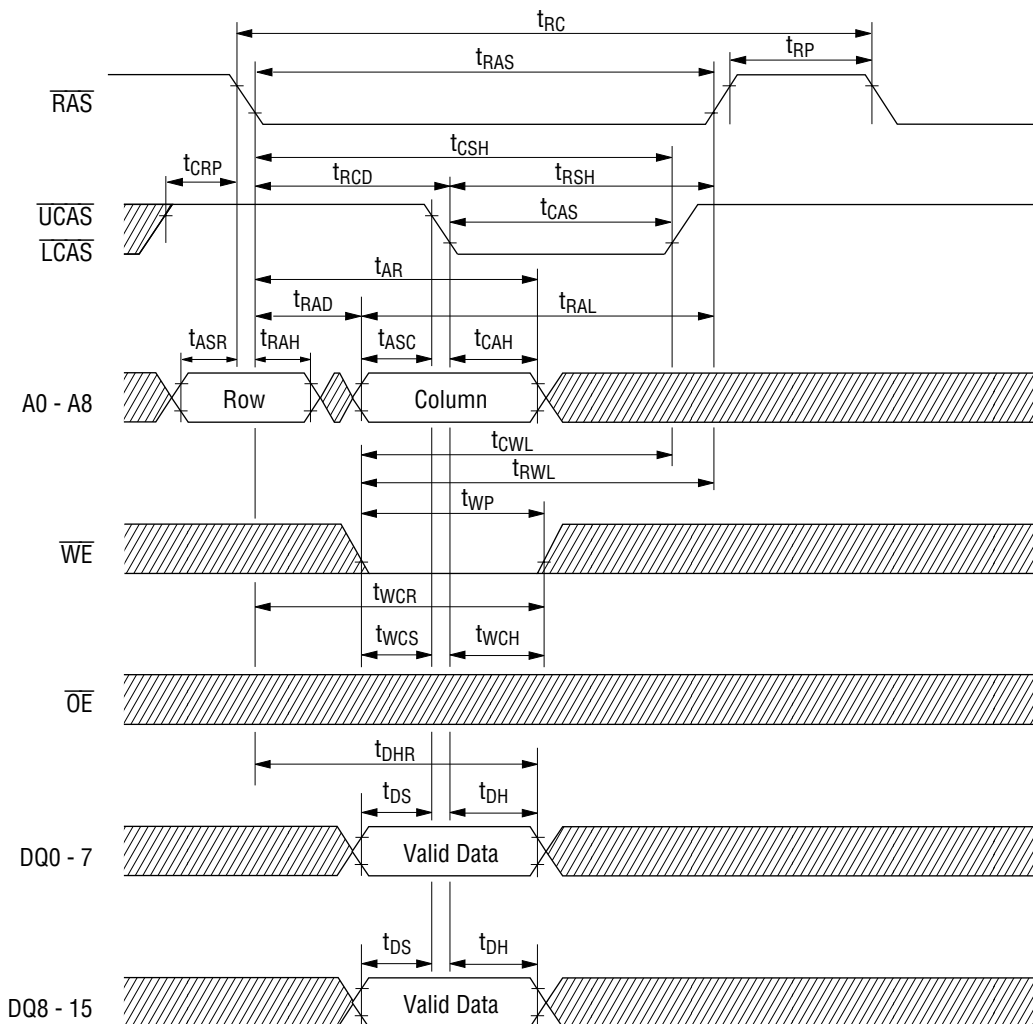
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Read Cycle ($\overline{\text{CAS}}$ Output Control)



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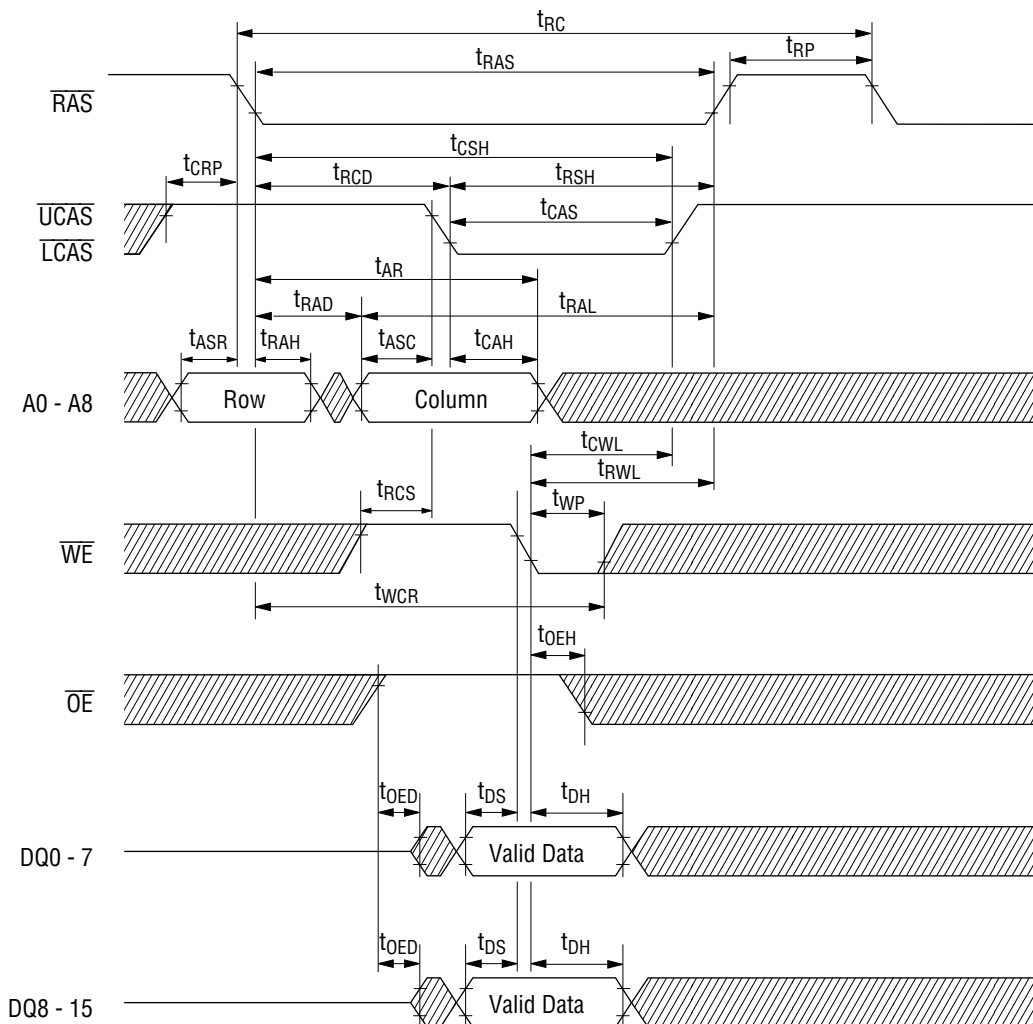
Early Write Cycle ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ Active)



"H" or "L"

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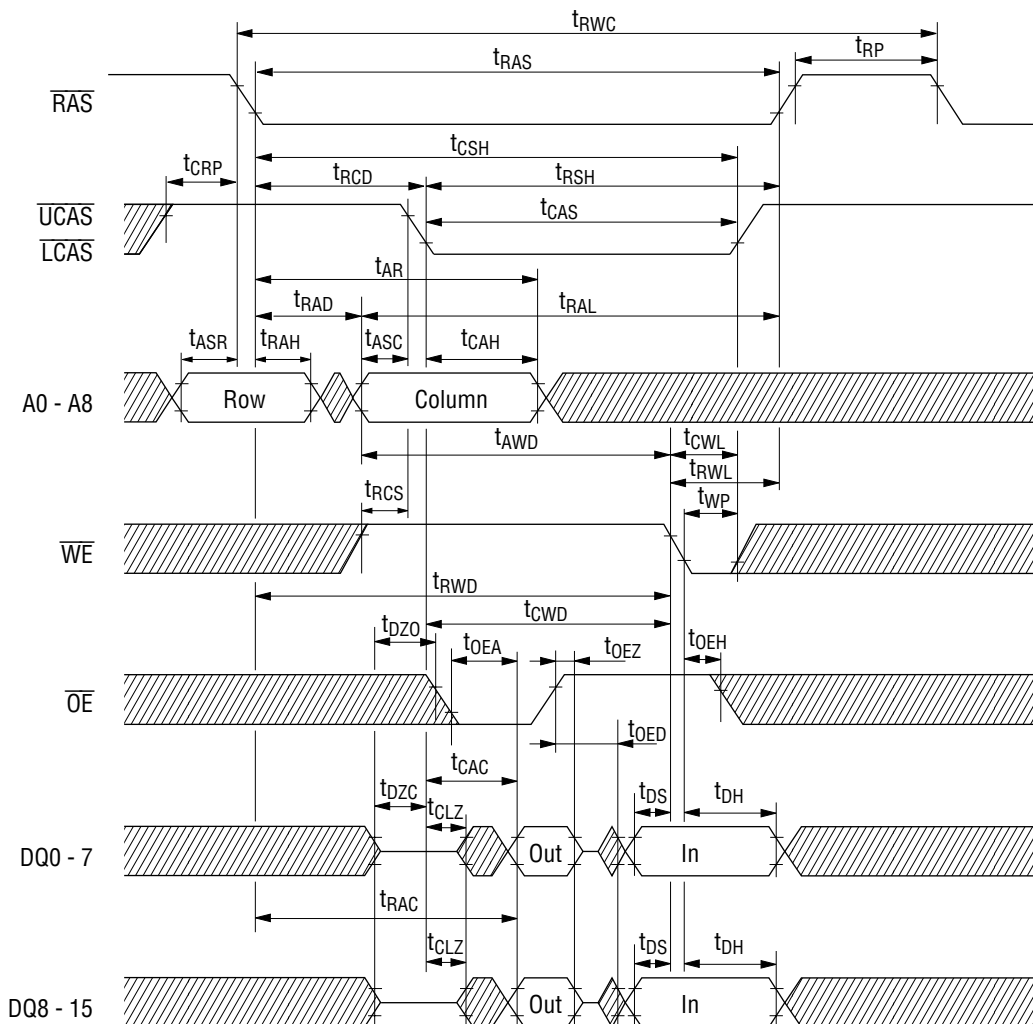
Late Write Cycle ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ Active)



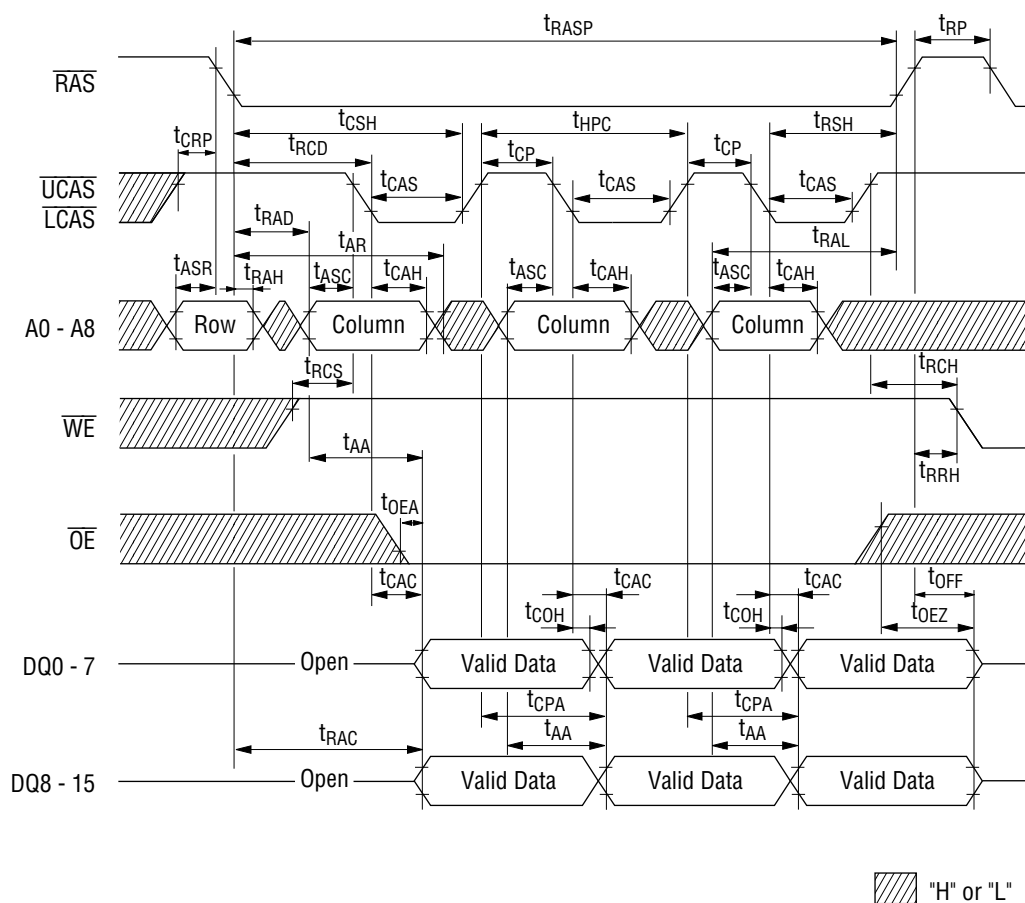
"H" or "L"

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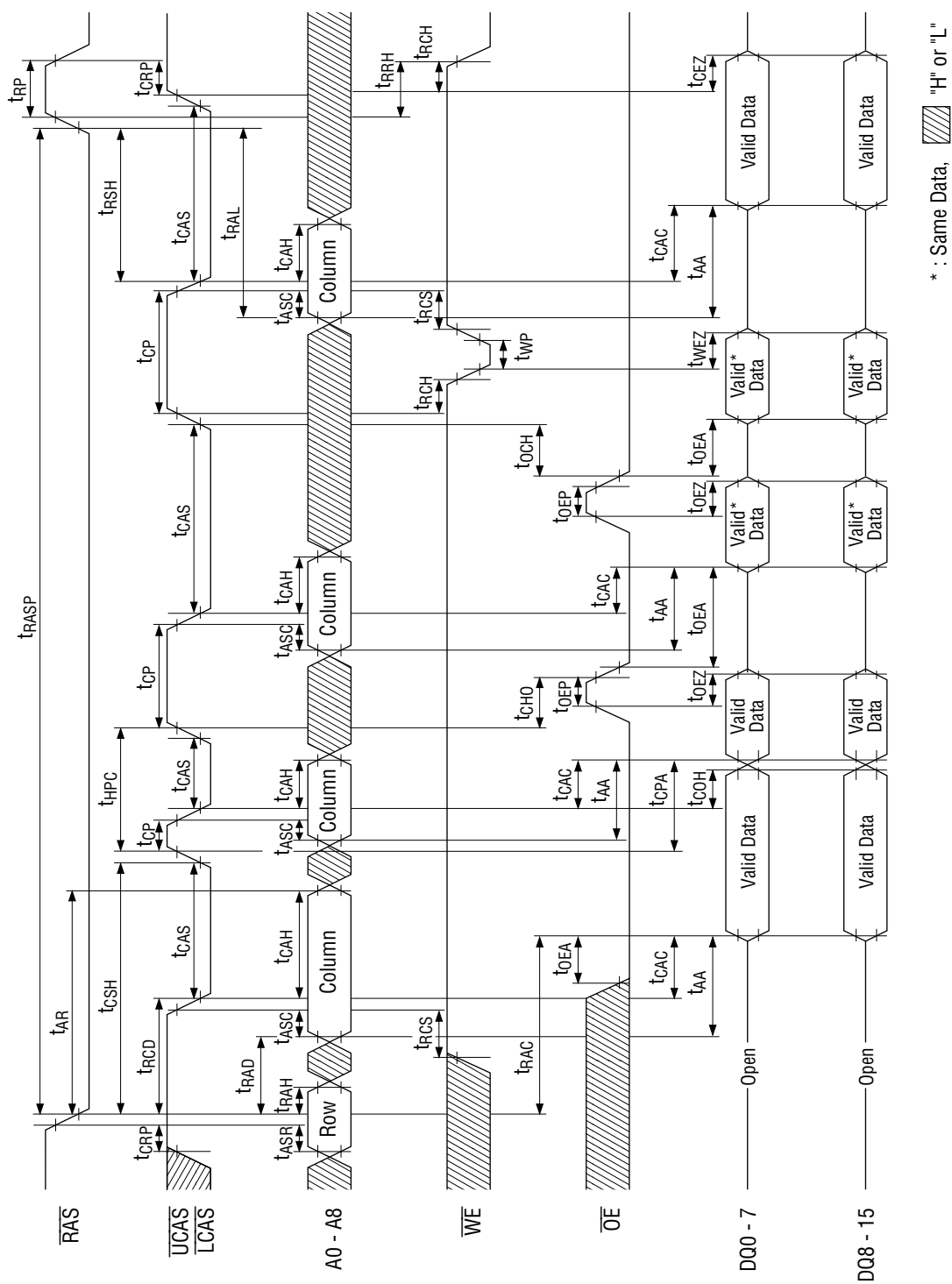
Read Modify Write Cycle ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ Active)



▨ "H" or "L"

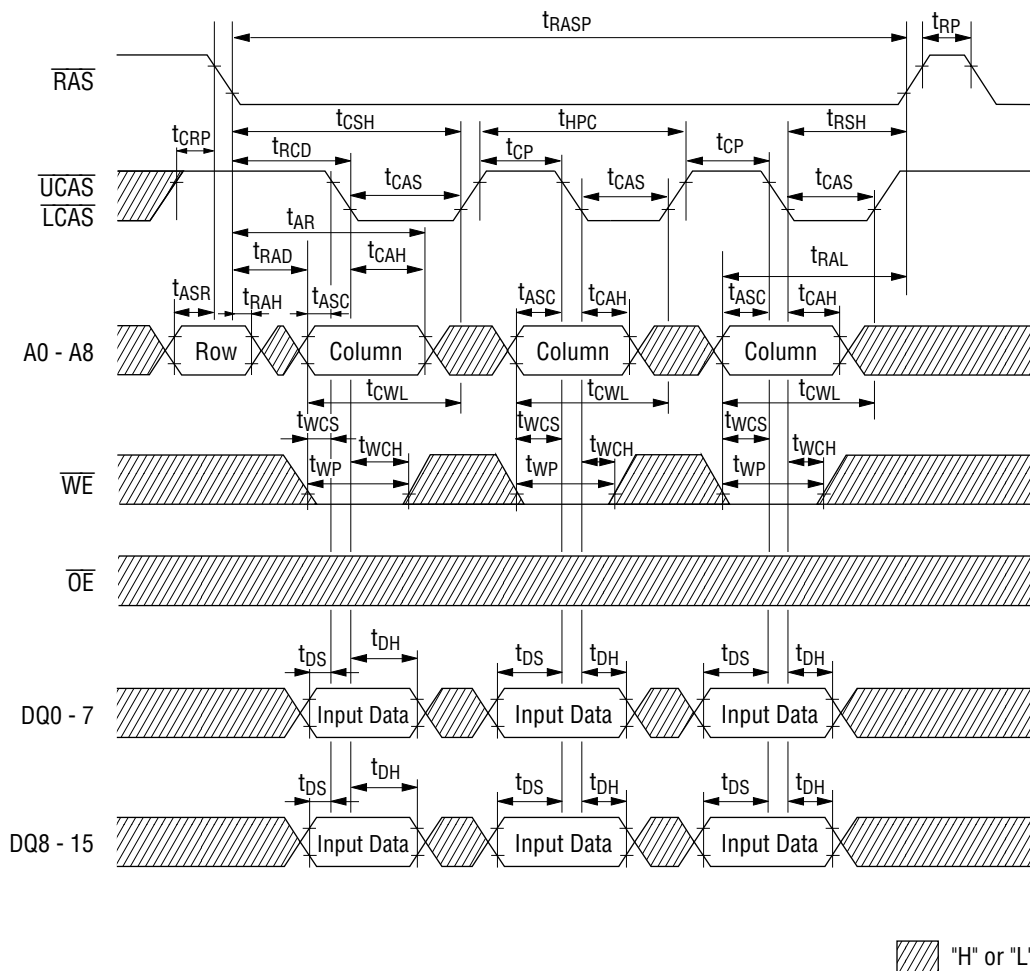


Fast Page Mode Read High-Z Operation

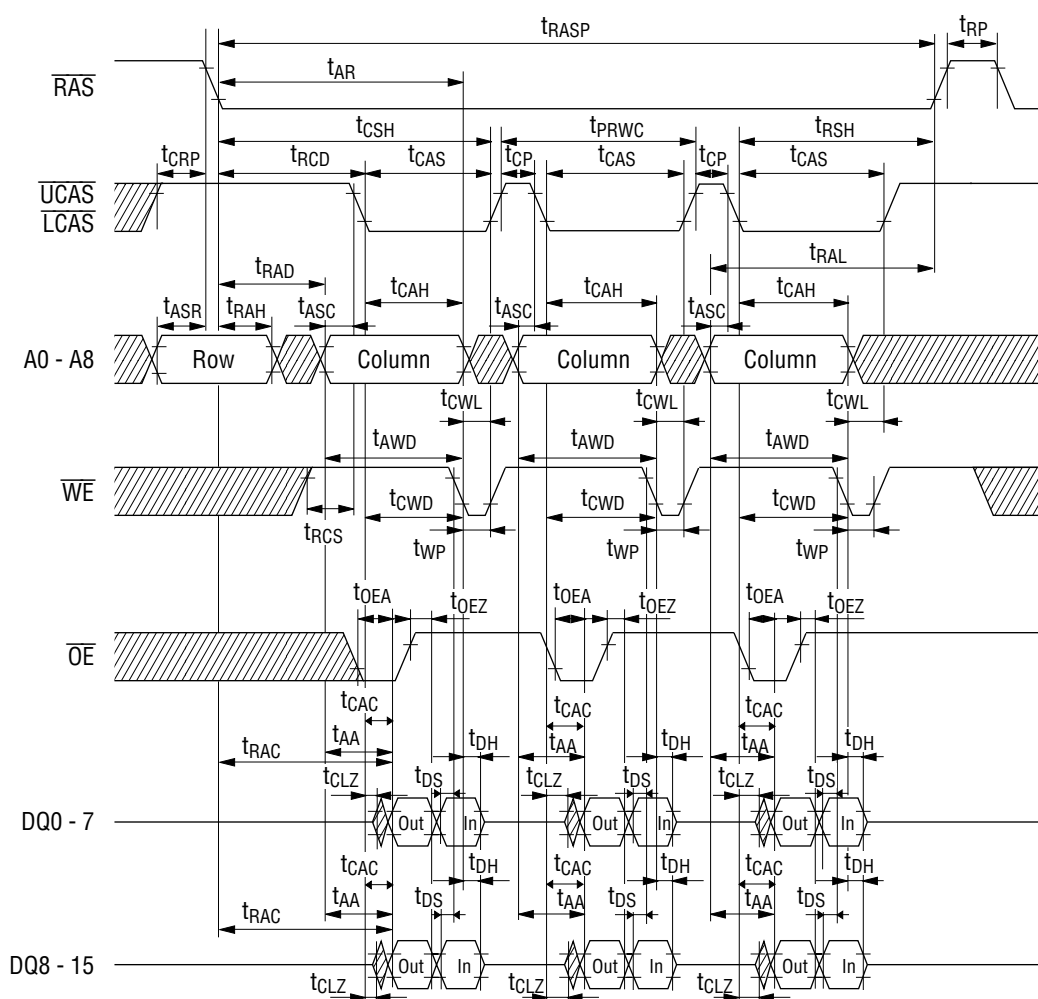


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Fast Page Mode Early Write Cycle



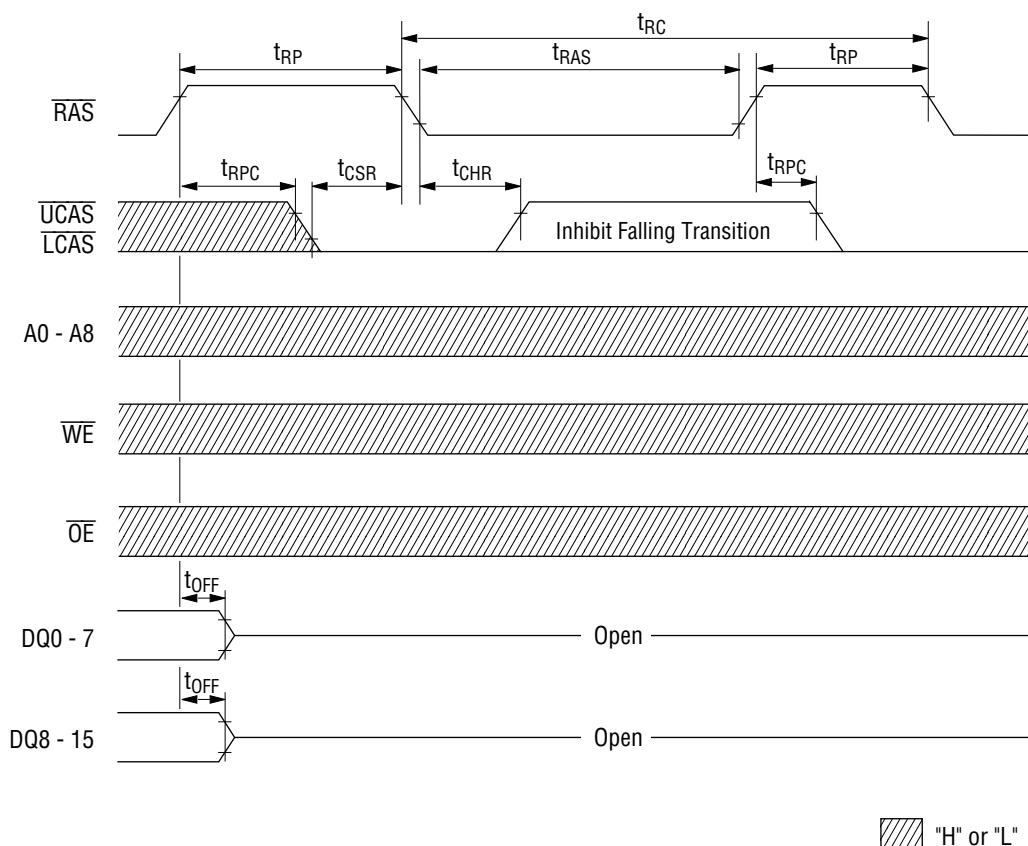
Fast Page Mode Read Modify Write Cycle



 "H" or "L"

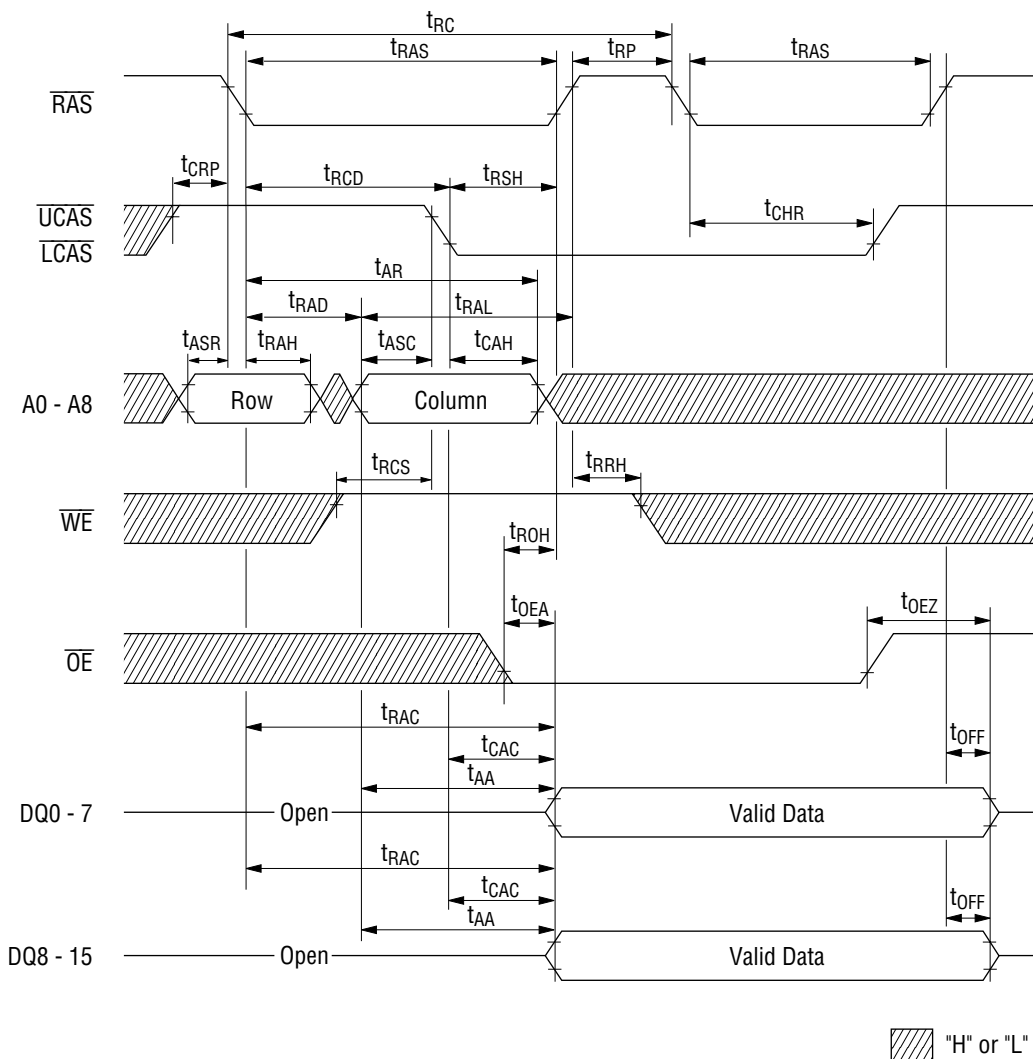
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CAS before RAS Refresh Cycle



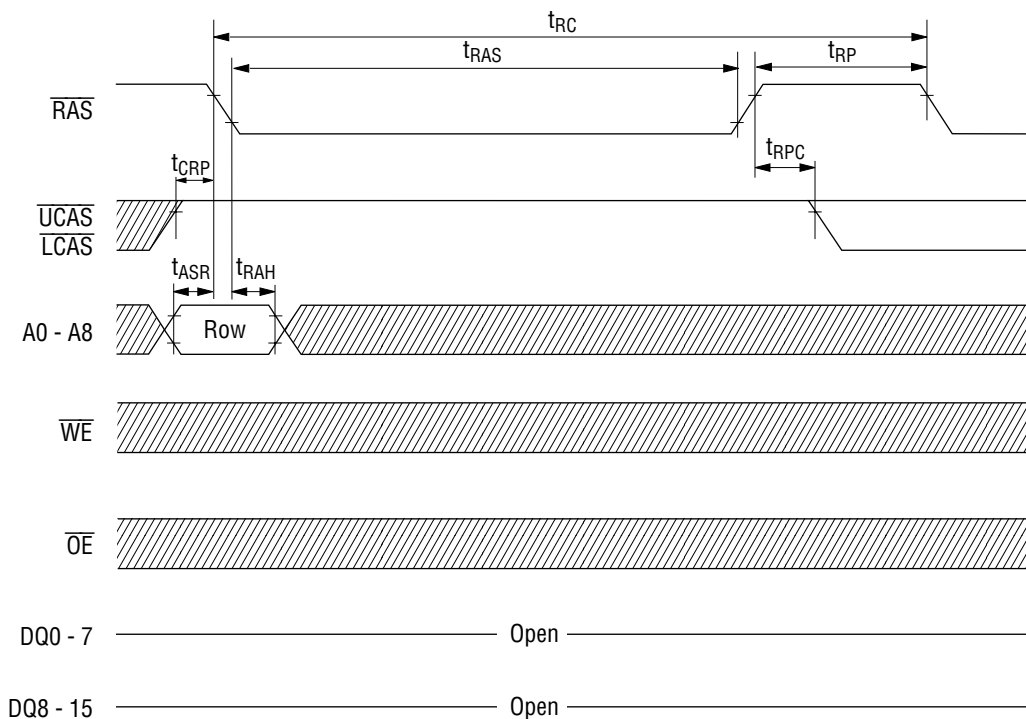
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Hidden Refresh Cycle



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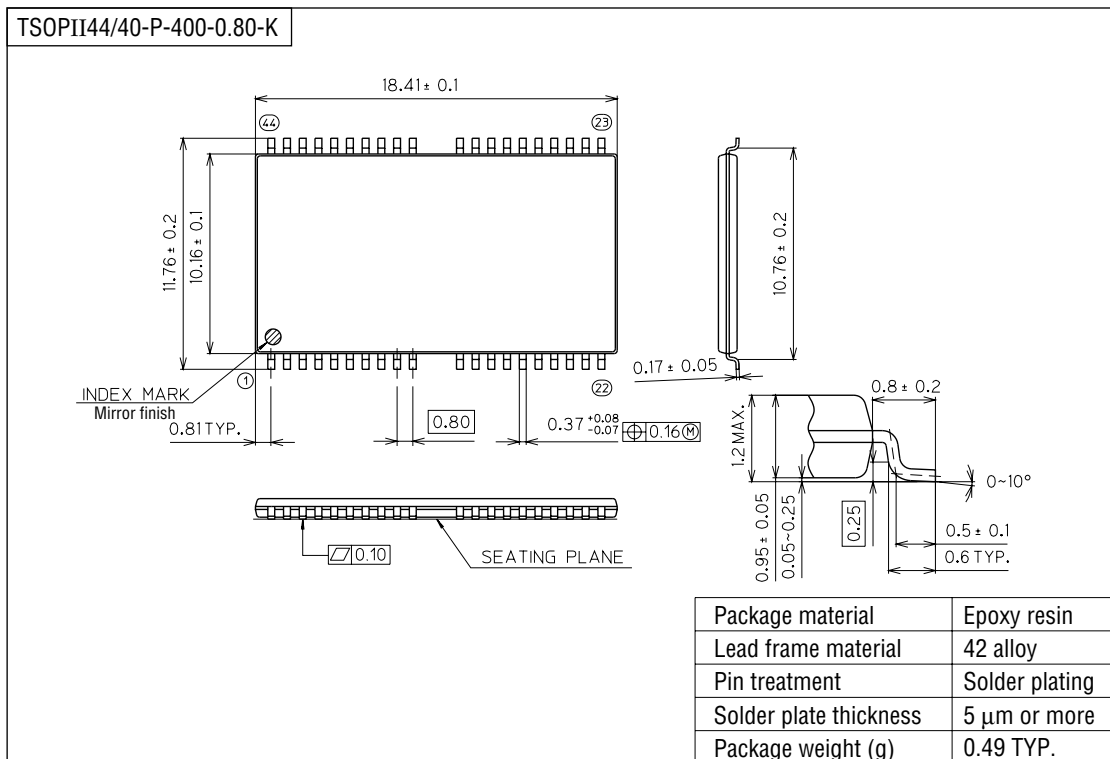
RAS Only Refresh Cycle



"H" or "L"

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(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.
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