

108 dB, 192 kHz 4-In, 8-Out CODEC

FEATURES

- ◆ Four 24-bit A/D, Eight 24-bit D/A Converters
- ◆ ADC Dynamic Range
 - 105 dB Differential
 - 102 dB Single-Ended
- ◆ DAC Dynamic Range
 - 108 dB Differential
 - 105 dB Single-Ended
- ◆ ADC/DAC THD+N
 - -98 dB Differential
 - -95 dB Single-Ended
- ◆ Compatible with Industry-Standard Time Division Multiplexed (TDM) Serial Interface
- ◆ System Sampling Rates up to 192 kHz
- ◆ Programmable ADC High-Pass Filter for DC Offset Calibration
- ◆ Logarithmic Digital Volume Control
- ◆ I²C® & SPI™ Host Control Port
- ◆ Supports Logic Levels Between 5 V and 1.8 V
- ◆ Popguard® Technology

GENERAL DESCRIPTION

The CS42888 CODEC provides four multi-bit analog-to-digital and eight multi-bit digital-to-analog delta-sigma converters. The CODEC is capable of operation with either differential or single-ended inputs and outputs, in a 64-pin LQFP package.

Four fully differential, or single-ended, inputs are available on stereo ADC1 and ADC2. Digital volume control is provided for each ADC channel, with selectable overflow detection.

All eight DAC channels provide digital volume control and can operate with differential or single-ended outputs.

An auxiliary serial input is available for an additional two channels of PCM data.

The CS42888 is available in a 64-pin LQFP package in Commercial (-10° to +70°) and Automotive (-40° to +105°) grades. The CDB42888 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to [“Ordering Information” on page 61](#) for complete ordering information.

The CS42888 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, and automotive audio systems.

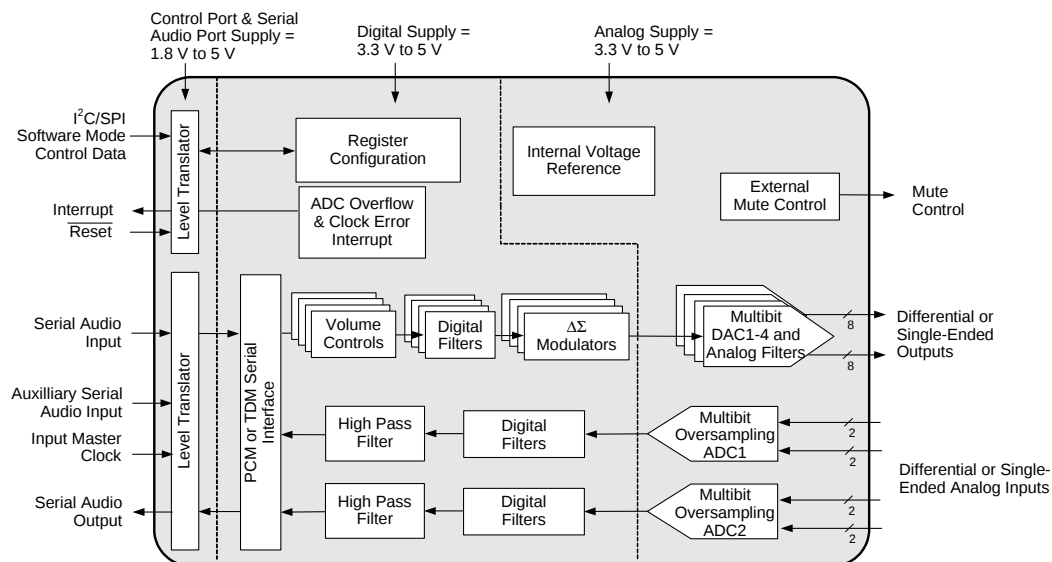


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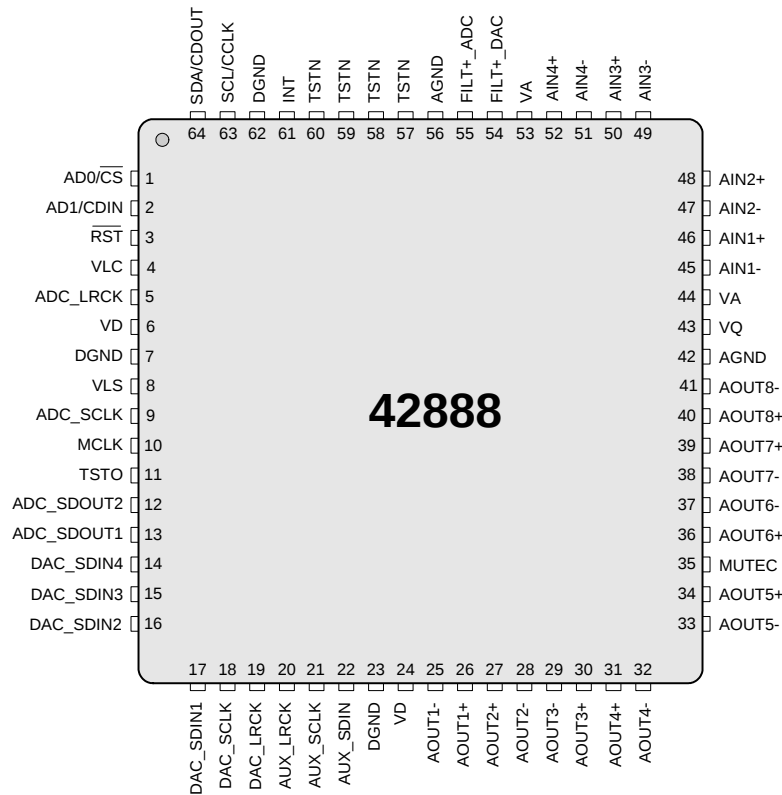
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1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
AD0/CS	1	Address Bit [0]/ Chip Select (Input) - Chip address bit in I ² C Mode. Control signal used to select the chip in SPI Mode.
AD1/CDIN	2	Address Bit [1]/ SPI Data Input (Input) - Chip address bit in I ² C Mode. Input for SPI data.
RST	3	Reset (Input) - The device enters a low power mode and all internal registers are reset to their default settings when low.
VLC	4	Control Port Power (Input) - Determines the required signal level for the control port. See "Digital I/O Pin Characteristics" on page 8.
ADC_LRCK	5	ADC Left/Right Clock (Input/Output) - Determines which channel, Left or Right, is currently active on the ADC serial audio data line. Signals the start of a new TDM frame in the TDM digital interface format.
VD	6, 24	Digital Power (Input) - Positive terminal of the power supply for the digital section.
DGND	7, 23 62	Digital Ground (Input) - Ground terminal of the power supply for the digital section.
VLS	8	Serial Port Interface Power (Input) - Determines the required signal level for the serial interfaces. See "Digital I/O Pin Characteristics" on page 8.
ADC_SCLK	9	ADC Serial Clock (Input/Output) - Serial clock for the ADC serial audio interface. Input frequency must be 256xFs in the TDM digital interface format.
MCLK	10	Master Clock (Input) - Clock source for the delta-sigma modulators and digital filters.
TSTO	11	Test Out - This pin is an output used for test purposes only. This pin must be not be connected to any external trace or other connection.
ADC_SDOUT1	13	Serial Audio Data Output (Output) - Outputs for two's complement serial audio data.
ADC_SDOUT2	12	

DAC_SDIN1	17	DAC Serial Audio Data Input (Input) - Input for two's complement serial audio data.
DAC_SDIN2	16	
DAC_SDIN3	15	
DAC_SDIN4	14	
DAC_SCLK	18	DAC Serial Clock (Input/Output) - Serial clock for the DAC serial audio interface. Input frequency must be 256xFs in the TDM digital interface format.
DAC_LRCK	19	DAC Left/Right Clock (Input/Output) - Determines which channel, Left or Right, is currently active on the DAC serial audio data line. Signals the start of a new TDM frame in the TDM digital interface format.
AUX_LRCK	20	Auxiliary Left/Right Clock (Output) - Determines which channel, Left or Right, is currently active on the Auxiliary serial audio data line. Derived from the ADC serial port and equals Fs.
AUX_SCLK	21	Auxiliary Serial Clock (Output) - Serial clock for the Auxiliary serial audio interface.
AUX_SDIN	22	Auxiliary Serial Input (Input) - Provides an additional serial input for two's complement serial audio data. Used only in the TDM digital interface format.
AOUT1 +,-	26, 25	Differential Analog Output (Output) - The full-scale analog output level is specified in the Analog Characteristics table. Each leg of the differential outputs may also be used single-ended.
AOUT2 +,-	27, 28	
AOUT3 +,-	30, 29	
AOUT4 +,-	31, 32	
AOUT5 +,-	34, 33	
AOUT6 +,-	36, 37	
AOUT7 +,-	38, 39	
AOUT8 +,-	40, 41	
MUTEC	35	Mute Control (Output) - Used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system.
AGND	42, 56	Analog Ground (Input) - Ground reference for the analog section.
VQ	43	Quiescent Voltage (Output) - Filter connection for internal quiescent reference voltage.
VA	44, 53	Analog Power (Input) - Positive power supply for the analog section. See "Digital I/O Pin Characteristics" on page 8 .
AIN1 +,-	46, 45	Differential Analog Input (Input) - Signals are presented differentially or single-ended to the Delta-Sigma modulators. The full-scale input level is specified in the Analog Characteristics specification table.
AIN2 +,-	48, 47	
AIN3 +,-	50, 49	
AIN4 +,-	52, 51	
FILT+_DAC	54	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits of the DAC.
FILT+_ADC	55	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits of the ADC.
TSTN	57, 58 59, 60	Test In - This pin is an input used for test purposes only. It must be tied to ground for normal operation.
INT	61	Interrupt (Output) - Signals either an ADC overflow condition has occurred in one or more of the ADC inputs, or a clocking error has occurred in the DAC/ADC as specified in the Interrupt register.
SCL/CCLK	63	Serial Control Port Clock (Input) - Serial clock for the control port interface.
SDA/CDOUT	64	Serial Control Data I/O (Input/Output) - Input/Output for I ² C data. Output for SPI data.

1.1 Digital I/O Pin Characteristics

Various pins on the CS42888 are powered from separate power supply rails. The logic level for each input should adhere to the corresponding power rail and should not exceed the maximum ratings.

Power Rail	Pin Name	I/O	Driver	Receiver
VLC	$\overline{\text{RST}}$	Input	-	1.8 V - 5.0 V, CMOS
	SCL/CCLK	Input	-	1.8 V - 5.0 V, CMOS, with Hysteresis
	SDA/CDOUT	Input/ Output	1.8 V - 5.0 V, CMOS/Open Drain	1.8 V - 5.0 V, CMOS, with Hysteresis
	AD0/ $\overline{\text{CS}}$	Input	-	1.8 V - 5.0 V, CMOS
	AD1/CDIN	Input	-	1.8 V - 5.0 V, CMOS
	INT	Output	1.8 V - 5.0 V, CMOS/Open Drain	-
VLS	MCLK	Input	-	1.8 V - 5.0 V, CMOS
	ADC_LRCK	Input/ Output	1.8 V - 5.0 V, CMOS	1.8 V - 5.0 V, CMOS
	ADC_SCLK	Input/ Output	1.8 V - 5.0 V, CMOS	1.8 V - 5.0 V, CMOS
	ADC_SDOUT1-2	Input/ Output	1.8 V - 5.0 V, CMOS	-
	DAC_LRCK	Input/ Output	1.8 V - 5.0 V, CMOS	1.8 V - 5.0 V, CMOS
	DAC_SCLK	Input/ Output	1.8 V - 5.0 V, CMOS	1.8 V - 5.0 V, CMOS
	DAC_SDIN1-4	Input	-	1.8 V - 5.0 V, CMOS
	AUX_LRCK	Output	1.8 V - 5.0 V, CMOS	-
	AUX_SCLK	Output	1.8 V - 5.0 V, CMOS	-
	AUX_SDIN	Input	-	1.8 V - 5.0 V, CMOS
VA	MUTEC	Output	3.3 V - 5.0 V, CMOS	-

Table 1. I/O Power Rails

2. TYPICAL CONNECTION DIAGRAM

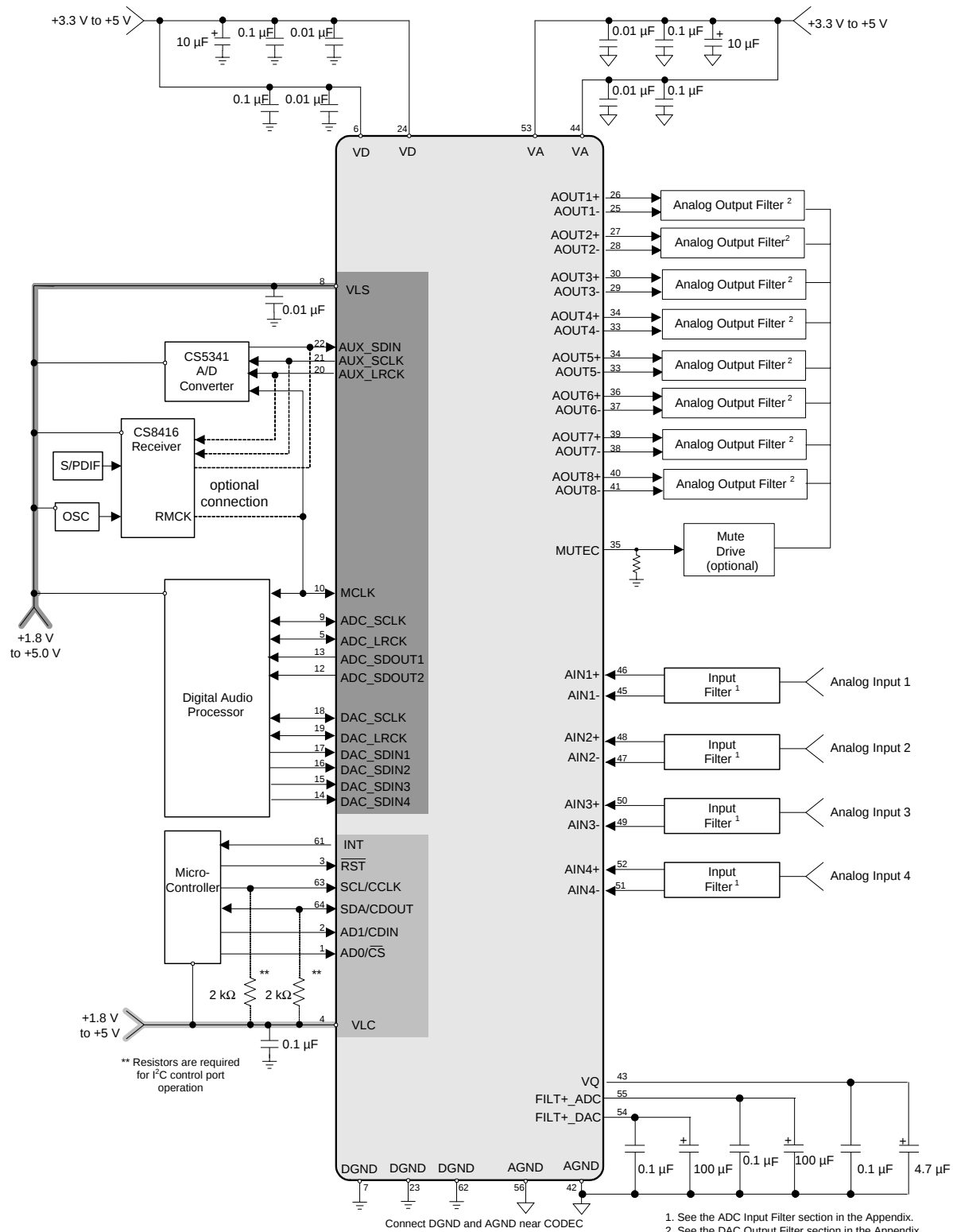


Figure 1. Typical Connection Diagram

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply				
Analog (Note 1)	VA	3.14	5.25	V
Digital	VD	3.14	5.25	V
Serial Audio Interface (Note 2)	VLS	1.71	5.25	V
Control Port Interface	VLC	1.71	5.25	V
Ambient Temperature				
Commercial -CQZ	T _A	-10	+70	°C
Automotive -DQZ		-40	+105	°C

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	Analog VA	-0.3	6.0	V
	Digital VD	-0.3	6.0	V
	Serial Port Interface VLS	-0.3	6.0	V
	Control Port Interface VLC	-0.3	6.0	V
Input Current (Note 3)	I _{in}	-	±10	mA
Analog Input Voltage (Note 4)	V _{IN}	AGND-0.7	VA+0.7	V
Digital Input Voltage (Note 4)	Serial Port Interface V _{IND-S}	-0.3	VLS+ 0.4	V
	Control Port Interface V _{IND-C}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)	T _A	-50	+125	°C
Storage Temperature	T _{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. Typical Analog input/output performance will slightly degrade at VA = 3.3 V.
2. The ADC_SDOUT may not meet timing requirements in TDM, Double-Speed Mode.
3. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
4. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS (COMMERCIAL)

(Test Conditions (unless otherwise specified): $T_A = -10$ to $+70^\circ\text{C}$; $V_D = V_{LS} = V_{LC} = 3.3\text{ V} \pm 5\%$, $V_A = 5\text{ V} \pm 5\%$;
 Full-scale input sine wave: 1 kHz through the active input filter in [Figure 25 on page 51](#) and [Figure 26 on page 51](#);
 Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential			Single-Ended			Unit
		Min	Typ	Max	Min	Typ	Max	
Fs=48 kHz, 96 kHz, 192 kHz								
Dynamic Range	A-weighted	99	105	-	96	102	-	dB
	unweighted	96	102	-	93	99	-	dB
	40 kHz bandwidth unweighted	-	99	-		96	-	dB
Total Harmonic Distortion + Noise (Note 5)	-1 dB	-	-98	-92	-	-95	-89	dB
	-20 dB	-	-82	-	-	-79	-	dB
	-60 dB	-	-42	-	-	-39	-	dB
	40 kHz bandwidth	-	-90	-	-	-90	-	dB
	-1 dB	-	-90	-	-	-90	-	dB
ADC1-2 Interchannel Isolation		-	90	-	-	90	-	dB
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Analog Input								
Full-Scale Input Voltage		1.06*VA	1.12*VA	1.18*VA	0.53*VA	0.56*VA	0.59*VA	Vpp
Differential Input Impedance (Note 6)		18	-	-	-	-	-	kΩ
Single-Ended Input Impedance (Note 7)		-	-	-	18	-	-	kΩ
Common Mode Rejection Ratio (CMRR)		-	82	-	-	-	-	dB

ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE)

(Test Conditions (unless otherwise specified): $T_A = -40$ to $+85^{\circ}\text{C}$; $V_D = V_{LS} = V_{LC} = 3.3\text{ V} \pm 5\%$, $V_A = 5\text{ V} \pm 5\%$;
 Full-scale input sine wave: 1 kHz through the active input filter in [Figure 25 on page 51](#) and [Figure 26 on page 51](#);
 Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential			Single-Ended			Unit
		Min	Typ	Max	Min	Typ	Max	
Fs=48 kHz, 96 kHz, 192 kHz								
Dynamic Range	A-weighted	97	105	-	94	102	-	dB
	unweighted	94	102	-	91	99	-	dB
	40 kHz bandwidth unweighted	-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise (Note 5)	-1 dB	-	-98	-90	-	-95	-87	dB
	-20 dB	-	-82	-	-	-79	-	dB
	-60 dB	-	-42	-	-	-39	-	dB
	40 kHz bandwidth	-	-87	-	-	-87	-	dB
	-1 dB	-	-87	-	-	-87	-	dB
ADC1-2 Interchannel Isolation		-	90	-	-	90	-	dB
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Analog Input								
Full-Scale Input Voltage		1.04*VA	1.12*VA	1.20*VA	0.52*VA	0.56*VA	0.60*VA	Vpp
Differential Input Impedance (Note 6)		18	-	-	-	-	-	kΩ
Single-Ended Input Impedance (Note 7)		-	-	-	18	-	-	kΩ
Common Mode Rejection Ratio (CMRR)		-	82	-	-	-	-	dB

Notes:

5. Referred to the typical full-scale voltage.
6. Measured between AINx+ and AINx-.
7. Measured between AINxx and AGND.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Notes 8, 9)		Min	Typ	Max	Unit
Single-Speed Mode (Note 9)					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4896	Fs
Passband Ripple		-	-	0.08	dB
Stopband		0.5688	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay		-	12/Fs	-	s
Double-Speed Mode (Note 9)					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4896	Fs
Passband Ripple		-	-	0.16	dB
Stopband		0.5604	-	-	Fs
Stopband Attenuation		69	-	-	dB
Total Group Delay		-	9/Fs	-	s
Quad-Speed Mode (Note 9)					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.2604	Fs
Passband Ripple		-	-	0.16	dB
Stopband		0.5000	-	-	Fs
Stopband Attenuation		60	-	-	dB
Total Group Delay		-	5/Fs	-	s
High-Pass Filter Characteristics					
Frequency Response	-3.0 dB	-	1	-	Hz
	-0.13 dB		20	-	Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Settling Time		-	$10^5/Fs$	0	s

Notes:

8. Filter response is guaranteed by design.
9. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 31 to 42) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL)

(Test Conditions (unless otherwise specified): $T_A = -10$ to $+70^\circ\text{C}$; $V_D = V_{LS} = V_{LC} = 3.3\text{ V} \pm 5\%$, $V_A = 5\text{ V} \pm 5\%$; Full-scale 997 Hz output sine wave (see [Note 11](#)) into passive filter in [Figure 31 on page 54](#) and active filter in [Figure 31 on page 54](#); Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential			Single-Ended			Unit
		Min	Typ	Max	Min	Typ	Max	
<i>F_s = 48 kHz, 96 kHz, 192 kHz</i>								
Dynamic Range	18 to 24-Bit	102	108	-	99	105	-	dB
	A-weighted							
	unweighted	99	105	-	96	102	-	dB
	16-Bit	-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise	18 to 24-Bit	-	-98	-92	-	-95	-89	dB
	0 dB							
	-20 dB							
	-60 dB	-	-45	-	-	-42	-	dB
	16-Bit	-	-93	-	-	-90	-	dB
	0 dB							
	-20 dB							
Interchannel Isolation	(1 kHz)	-	100	-	-	100	-	dB
<i>Analog Output</i>								
Full-Scale Output		1.235•V _A	1.300•V _A	1.365•V _A	0.618•V _A	0.650•V _A	0.683•V _A	V _{pp}
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Output Impedance		-	100	-	-	100	-	Ω
DC Current draw from an AOUT pin (Note 10)		-	-	10	-	-	10	μA
AC-Load Resistance (R _L) (Note 12)		3	-	-	3	-	-	kΩ
Load Capacitance (C _L) (Note 12)		-	-	100	-	-	100	pF

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE)

(Test Conditions (unless otherwise specified): $T_A = -40$ to $+85^\circ\text{C}$; $V_D = V_{LS} = V_{LC} = 3.3\text{ V} \pm 5\%$, $V_A = 5\text{ V} \pm 5\%$; Full-scale 997 Hz output sine wave (see [Note 11](#)) in [Figure 31 on page 54](#) and [Figure 31 on page 54](#); Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential			Single-Ended			Unit
		Min	Typ	Max	Min	Typ	Max	
<i>Fs = 48 kHz, 96 kHz, 192 kHz</i>								
Dynamic Range 18 to 24-Bit	A-weighted	100	108	-	97	105	-	dB
	unweighted	97	105	-	94	102	-	dB
	A-weighted	-	99	-	-	96	-	dB
	unweighted	-	96	-	-	93	-	dB
Total Harmonic Distortion + Noise 18 to 24-Bit	0 dB	-	-98	-90	-	-95	-87	dB
	-20 dB	-	-85	-	-	-82	-	dB
	-60 dB	-	-45	-	-	-42	-	dB
	0 dB	-	-93	-	-	-90	-	dB
	-20 dB	-	-76	-	-	-73	-	dB
	-60 dB	-	-36	-	-	-33	-	dB
16-Bit	0 dB	-	-93	-	-	-90	-	dB
	-20 dB	-	-76	-	-	-73	-	dB
16-Bit	-60 dB	-	-36	-	-	-33	-	dB
Interchannel Isolation	(1 kHz)	-	100	-	-	100	-	dB
<i>Analog Output</i>								
Full-Scale Output		1.210•VA	1.300•VA	1.392•VA	0.605•VA	0.650•VA	0.696•VA	V _{pp}
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Output Impedance		-	100	-	-	100	-	Ω
DC Current draw from an AOUT pin (Note 10)		-	-	10	-	-	10	μA
AC-Load Resistance (R_L) (Note 12)		3	-	-	3	-	-	kΩ
Load Capacitance (C_L) (Note 12)		-	-	100	-	-	100	pF

Notes:

10. Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC-blocking capacitors.
11. One-half LSB of triangular PDF dither is added to data.
12. Guaranteed by design. See [Figure 2](#). R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the dominant pole of the two-pole amp in the output stage. Increasing this value beyond the recommended 100 pF can cause the internal op-amp to become unstable. See ["External Filters" on page 51](#) for a recommended output filter.

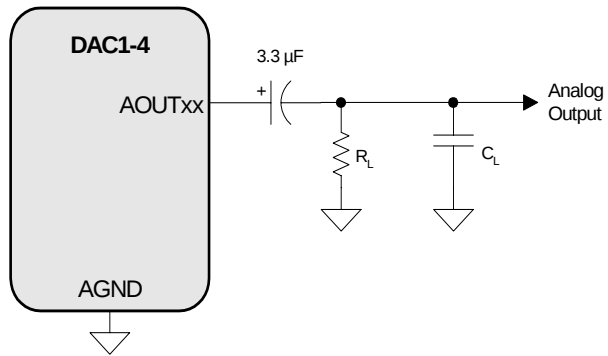


Figure 2. Output Test Circuit for Maximum Load

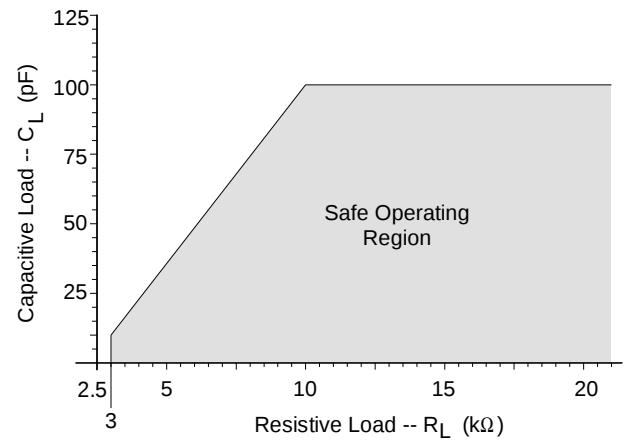


Figure 3. Maximum Loading

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Notes 8, 13)	Min	Typ	Max	Unit
Single-Speed Mode				
Passband (Frequency Response) to -0.05 dB corner to -3 dB corner	0	-	0.4780	Fs
	0	-	0.4996	Fs
Frequency Response 10 Hz to 20 kHz	-0.2	-	+0.08	dB
StopBand	0.5465	-	-	Fs
StopBand Attenuation (Note 14)	50	-	-	dB
Group Delay	-	10/Fs	-	s
De-emphasis Error (Note 15)	Fs = 32 kHz	-	+1.5/+0	dB
	Fs = 44.1 kHz	-	+0.05/-0.25	dB
	Fs = 48 kHz	-	-0.2/-0.4	dB
Double-Speed Mode				
Passband (Frequency Response) to -0.1 dB corner to -3 dB corner	0	-	0.4650	Fs
	0	-	0.4982	Fs
Frequency Response 10 Hz to 20 kHz	-0.2	-	+0.7	dB
StopBand	0.5770	-	-	Fs
StopBand Attenuation (Note 14)	55	-	-	dB
Group Delay	-	5/Fs	-	s
Quad-Speed Mode				
Passband (Frequency Response) to -0.1 dB corner to -3 dB corner	0	-	0.397	Fs
	0	-	0.476	Fs
Frequency Response 10 Hz to 20 kHz	-0.2	-	+0.05	dB
StopBand	0.7	-	-	Fs
StopBand Attenuation (Note 14)	51	-	-	dB
Group Delay	-	2.5/Fs	-	s

Notes:

13. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 43 to 54) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
14. Single- and Double-Speed Mode Measurement Bandwidth is from Stopband to 3 Fs.
Quad-Speed Mode Measurement Bandwidth is from Stopband to 1.34 Fs.
15. De-emphasis is only available in Single-Speed Mode.

SWITCHING SPECIFICATIONS - ADC/DAC PORT

(Inputs: Logic 0 = DGND, Logic 1 = VLS, ADC_SDOOUT C_{LOAD} = 15 pF.)

Parameters (Note 20)	Symbol	Min	Max	Units
Slave Mode				
RST pin Low Pulse Width (Note 16)		1	-	ms
MCLK Frequency		0.512	50	MHz
MCLK Duty Cycle (Note 17)		45	55	%
Input Sample Rate (LRCK) Single-Speed Mode Double-Speed Mode (Note 18) Quad-Speed Mode (Note 19)	F _s	4	50	kHz
	F _s	50	100	kHz
	F _s	100	200	kHz
LRCK Duty Cycle		45	55	%
SCLK Duty Cycle		45	55	%
SCLK High Time	t _{sckh}	8	-	ns
SCLK Low Time	t _{sckl}	8	-	ns
LRCK Rising Edge to SCLK Rising Edge	t _{fss} t _{lcks}	5	-	ns
SCLK Rising Edge to LRCK Falling Edge	t _{fsh}	16	-	ns
SCLK Falling Edge to ADC_SDOUT Output Valid	t _{dpd}	-	35	ns
DAC_SDIN Setup Time Before SCLK Rising Edge	t _{ds}	3	-	ns
DAC_SDIN Hold Time After SCLK Rising Edge	t _{dh}	5	-	ns
DAC_SDIN Hold Time After SCLK Rising Edge	t _{dh1}	5	-	ns
ADC_SDOUT Hold Time After SCLK Rising Edge	t _{dh2}	10	-	ns
ADC_SDOUT Valid Before SCLK Rising Edge	t _{dval}	15	-	ns
Master Mode				
Output Sample Rate (LRCK) All Speed Modes	F _s	-	MCLK / 256	kHz
LRCK Duty Cycle		45	55	%
SCLK Frequency		-	64 x F _s	MHz
SCLK Duty Cycle		45	55	%
LRCK Edge to SCLK Rising Edge	t _{lcks}	-	5	ns
SCLK Falling Edge to ADC_SDOUT Output Valid	t _{dpd}	-	35	ns
DAC_SDIN Setup Time Before SCLK Rising Edge	t _{ds}	3	-	ns
DAC_SDIN Hold Time After SCLK Rising Edge	t _{dh1}	5	-	ns

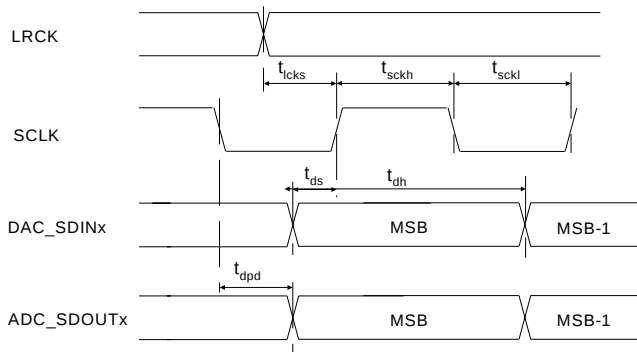


Figure 4. Serial Audio Interface Slave Mode Timing

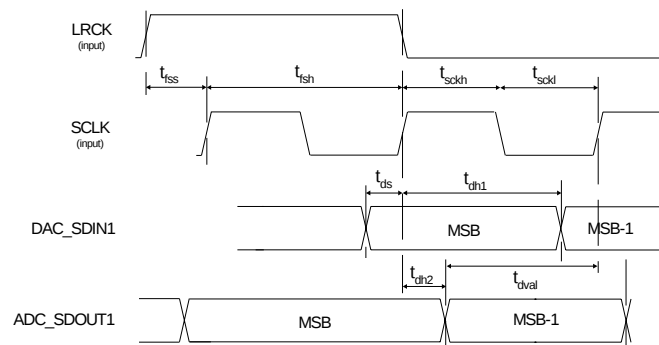


Figure 5. TDM Serial Audio Interface Timing

Notes:

16. After powering up the CS42888, $\overline{\text{RST}}$ should be held low after the power supplies and clocks are settled.
17. See [Table 10 on page 42](#) and [Table 11 on page 43](#) for suggested MCLK frequencies.
18. When operating in TDM interface format, VLS is limited to nominal 2.5 V to 5.0 V operation only.
19. ADC - I²S, Left-Justified, Right-Justified interface formats only. DAC - I²S, Left-Justified, Right-Justified and Time Division Multiplexed interface formats only.
20. "LRCK" and "SCLK" shall refer to the ADC and DAC left/right clock and serial clock, respectively.

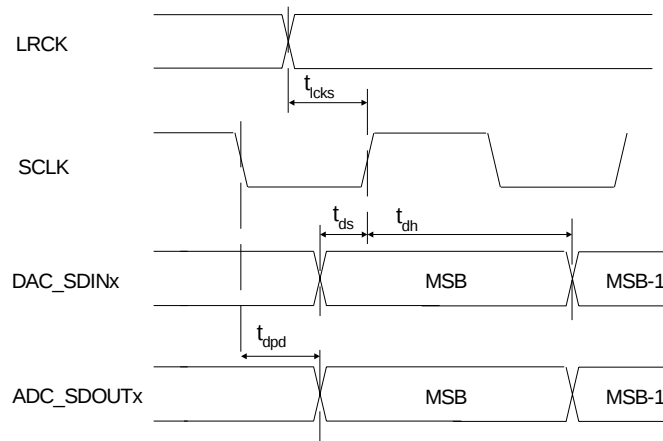


Figure 6. Serial Audio Interface Master Mode Timing

SWITCHING CHARACTERISTICS - AUX PORT

(Inputs: Logic 0 = DGND, Logic 1 = VLS.)

Parameters	Symbol	Min	Max	Units
Master Mode				
Output Sample Rate (AUX_LRCK) All Speed Modes	F_s	-	ADC_LRCK	kHz
AUX_SCLK Frequency		-	$64 \cdot \text{ADC_LRCK}$	kHz
AUX_SCLK Duty Cycle		45	55	%
AUX_LRCK Edge to SCLK Rising Edge	t_{lcks}	-	5	ns
AUX_SDIN Setup Time Before SCLK Rising Edge	t_{ds}	3	-	ns
AUX_SDIN Hold Time After SCLK Rising Edge	t_{dh}	5	-	ns

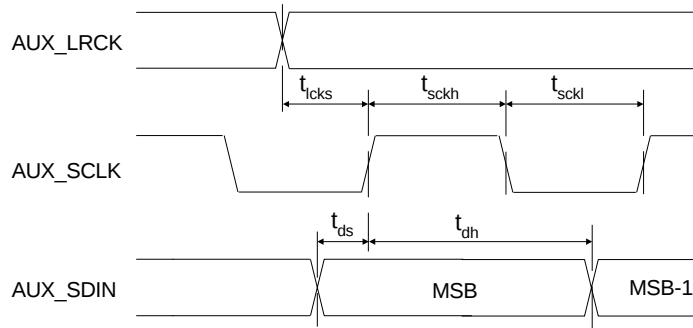


Figure 7. Serial Audio Interface Slave Mode Timing

SWITCHING SPECIFICATIONS - CONTROL PORT - I²C MODE

(VLC = 1.8 V - 5.0 V, VLS = VD = 3.3 V, VA = 5.0 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, SDA C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
RST Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	μs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	μs
Clock Low time	t_{low}	4.7	-	μs
Clock High Time	t_{high}	4.0	-	μs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	μs
SDA Hold Time from SCL Falling (Note 21)	t_{hdd}	0	-	μs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA (Note 22)	t_{rc}	-	1	μs
Fall Time SCL and SDA (Note 22)	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	μs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Notes:

21. Data must be held for sufficient time to bridge the transition time, t_{fc} , of SCL.
22. Guaranteed by design.

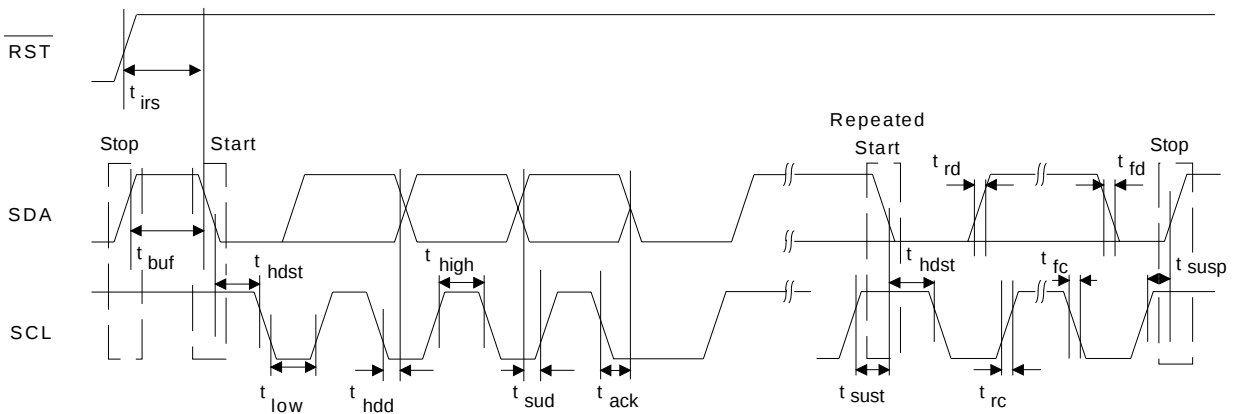


Figure 8. Control Port Timing - I²C Format

SWITCHING SPECIFICATIONS - CONTROL PORT - SPI FORMAT

(VLC = 1.8 V - 5.0 V, VLS = VD = 3.3 V, VA = 5.0 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, CDOUT C_L = 30 pF)

Parameter	Symbol	Min	Max	Units
CCLK Clock Frequency	f_{sck}	0	6.0	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling	t_{srs}	20	-	ns
$\overline{CS}$ Falling to CCLK Edge	t_{css}	20	-	ns
$\overline{CS}$ High Time Between Transmissions	t_{csh}	1.0	-	μ s
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 23)	t_{dh}	15	-	ns
CCLK Falling to CDOUT Stable	t_{pd}	-	50	ns
Rise Time of CDOUT	t_{r1}	-	25	ns
Fall Time of CDOUT	t_{f1}	-	25	ns
Rise Time of CCLK and CDIN (Note 24)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 24)	t_{f2}	-	100	ns

Notes:

23. Data must be held for sufficient time to bridge the transition time of CCLK.

24. For $f_{sck} < 1$ MHz.

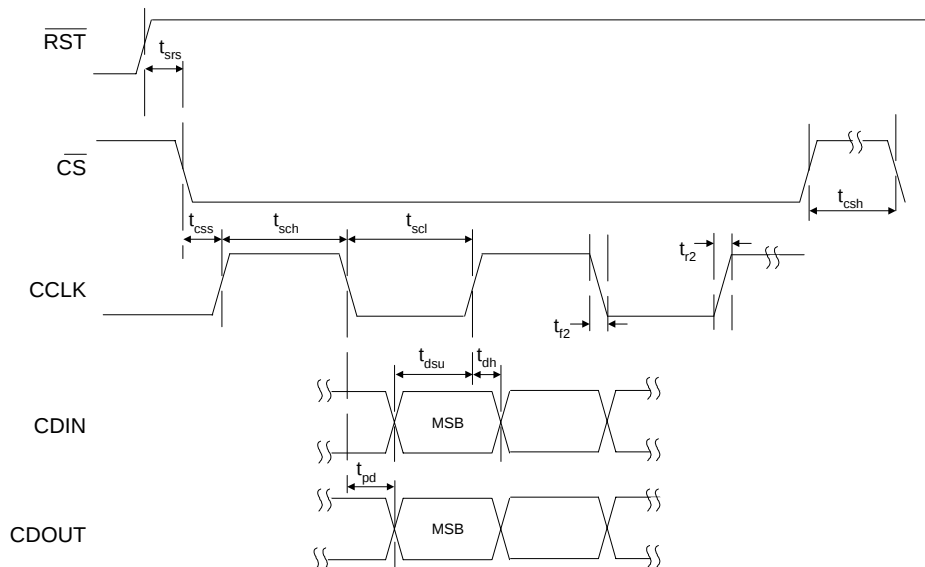


Figure 9. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Typ	Max	Units
Normal Operation (Note 25)					
Power Supply Current $V_A = 5.0\text{ V}$	I_A	-	80	-	mA
$V_{LS} = V_{LC} = V_D = 3.3\text{ V}$ (Note 26)	I_{DT}	-	60.6	-	mA
Power Dissipation All Supplies = 5 V		-	600	850	mW
Power Supply Rejection Ratio 1 kHz (Note 27) 60 Hz	PSRR	-	60	-	dB
		-	40	-	dB
Power-Down Mode (Note 28)					
Power Dissipation All Supplies = $V_A = 5\text{ V}$		-	1.25	-	mW
VQ Characteristics					
Nominal Voltage		-	$0.5 \cdot V_A$	-	V
Output Impedance		-	23	-	k Ω
DC Current Source/Sink (Note 29)		-	-	10	μA
FILT+ _ADC Nominal Voltage		-	V_A	-	V
FILT+ _DAC Nominal Voltage		-	V_A	-	V

Notes:

25. Normal operation is defined as $\overline{\text{RST}} = \text{HI}$ with a 997 Hz, 0 dBFS input to the DAC and AUX port, and a 1 kHz, -1 dB analog input to the ADC port sampled at the highest F_s for each speed mode. DAC outputs are open, unless otherwise specified.
26. I_{DT} measured with no external loading on pin 64 (SDA).
27. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.
28. Power-Down Mode is defined as $\overline{\text{RST}} = \text{LO}$ with all clocks and data lines held static and no analog input.
29. Guaranteed by design. The DC current draw represents the allowed current draw from the VQ pin due to typical leakage through the electrolytic de-coupling capacitors.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 30)	Symbol	Min	Typ	Max	Units
High-Level Output Voltage at $I_O = 2\text{ mA}$	V_{OH}	Serial Port	VLS-1.0	-	V
Control Port		VLC-1.0	-	-	V
MUTEC		VA-1.0	-	-	V
Low-Level Output Voltage at $I_O = 2\text{ mA}$	V_{OL}	Serial Port	-	0.4	V
Control Port		-	-	0.4	V
MUTEC		-	-	0.4	V
High-Level Input Voltage	V_{IH}	Serial Port	$0.7 \times V_{LS}$	-	V
Control Port		$0.7 \times V_{LC}$	-	-	V
Low-Level Input Voltage	V_{IL}	Serial Port	-	$0.2 \times V_{LS}$	V
Control Port		-	-	$0.2 \times V_{LC}$	V
Leakage Current	I_{in}	-	-	± 10	μA
Input Capacitance (Note 22)		-	-	10	pF
MUTEC Drive Current		-	3	-	mA

Notes:

30. See "Digital I/O Pin Characteristics" on page 8 for serial and control port power rails.

4. APPLICATIONS

4.1 Overview

The CS42888 is a highly integrated mixed signal 24-bit audio CODEC comprised of 4 analog-to-digital converters (ADC) implemented using multi-bit delta-sigma techniques and 8 digital-to-analog converters (DAC) also implemented using multi-bit delta-sigma techniques.

Other functions integrated within the CODEC include independent digital volume controls for each DAC, digital de-emphasis filters for the DAC, digital volume control with gain on each ADC channel, ADC high-pass filters, an on-chip voltage reference, and Popguard technology that minimizes the effects of output transients on power-up and power-down.

All serial data is transmitted through two independent serial ports: the DAC serial port and the ADC serial port. Each serial port can be configured independently to operate at different sample and clock rates, but both must run synchronous to each other.

The serial audio interface ports allow up to 8 DAC channels and 6 ADC channels in a Time-Division Multiplexed (TDM) interface format. In the One-Line Mode (OLM) interface format, the CS42888 will allow up to 6 ADC channels on one data line and up to 8 DAC channels on 2 data lines.

The CS42888 features an Auxiliary Port used to accommodate an additional two channels of PCM data on the ADC_SDOOUT data line in the TDM digital interface format. See [“AUX Port Digital Interface Formats” on page 33](#) for details.

The CS42888 operates in one of three oversampling modes based on the input sample rate. When operating the CODEC as a slave, mode selection is determined automatically based on the MCLK frequency setting. When operating as a master, mode selection is determined by the ADC and DAC FM bits in register [“Functional Mode \(Address 03h\)” on page 42](#). Single-Speed Mode (SSM) supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed Mode (DSM) supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed Mode (QSM) supports input sample rates up to 200 kHz and uses an oversampling ratio of 32x (**Note:** QSM for the ADC is only supported in the I²S, Left-Justified, Right-Justified interface formats. QSM for the DAC is supported in the I²S, Left-Justified, Right-Justified and Time Division Multiplexed interface formats).

All functions can be configured through software via a serial control port operable in SPI Mode or in I²C Mode.

[Figure 2 on page 16](#) shows the recommended connections for the CS42888. See [“Register Description” on page 40](#) for the default register settings and options.

4.2 Analog Inputs

4.2.1 Line-Level Inputs

AINx+ and AINx- are the line-level differential analog inputs internally biased to V_Q, approximately V_A/2. [Figure 10 on page 25](#) shows the full-scale analog input levels. The CS42888 also accommodates single-ended signals on all inputs, AIN1-AIN4. See [“ADC Input Filter” on page 51](#) for the recommended input filters.

For single-ended operation on ADC1-ADC2 (AIN1 to AIN4), the ADCx_SINGLE bit in the register [“ADC Control & DAC De-Emphasis \(Address 05h\)” on page 44](#) must be set appropriately (see [Figure 26 on page 51](#) for required external components).

The gain/attenuation of the signal can be adjusted for each AINx independently through the [“AINX Volume Control \(Address 11h-14h\)” on page 48](#).

The ADC output data is in 2's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFFH or 800000H, respectively, and cause the ADC Overflow bit in the register ["Status \(Address 19h\) \(Read Only\)" on page 49](#) to be set to a '1'.

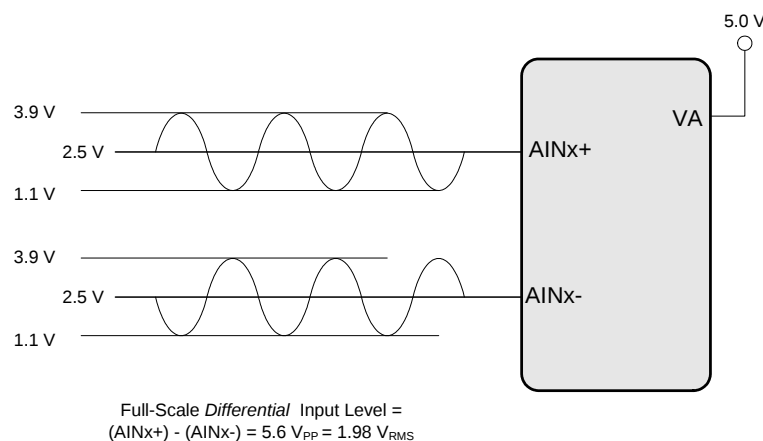


Figure 10. Full-Scale Input

4.2.2 High-Pass Filter and DC Offset Calibration

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the high-pass filter is disabled during normal operation, the current value of the DC offset for the corresponding channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS42888 with the high-pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.

Disabling the high-pass filter and freezing the stored DC offset. The high-pass filter for ADC1/ADC2 can be enabled and disabled. The high-pass filters are controlled using the HPF_FREEZE bit in the register ["ADC Control & DAC De-Emphasis \(Address 05h\)" on page 44](#).

4.3 Analog Outputs

4.3.1 Initialization

The initialization and Power-Down sequence flow chart is shown in [Figure 11 on page 26](#). The CS42888 enters a power-down state upon initial power-up. The interpolation and decimation filters, delta-sigma modulators and control port registers are reset. The internal voltage reference, multi-bit digital-to-analog and analog-to-digital converters and switched-capacitor low-pass filters are powered down.

The device remains in the power-down state until the $\overline{\text{RST}}$ pin is brought high. The control port is accessible once $\overline{\text{RST}}$ is high, and the desired register settings can be loaded per the interface descriptions in the ["Control Port Description and Timing" on page 33](#).

Once MCLK is valid, VQ will ramp up to VA/2, and the internal voltage references, FILT+_ADC and FILT+_DAC, will begin powering up to normal operation. Power is applied to the D/A converters and switched-capacitor filters, and the analog outputs are clamped to the quiescent voltage, VQ. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio. After an approximate 2000 sample period delay, normal operation begins.

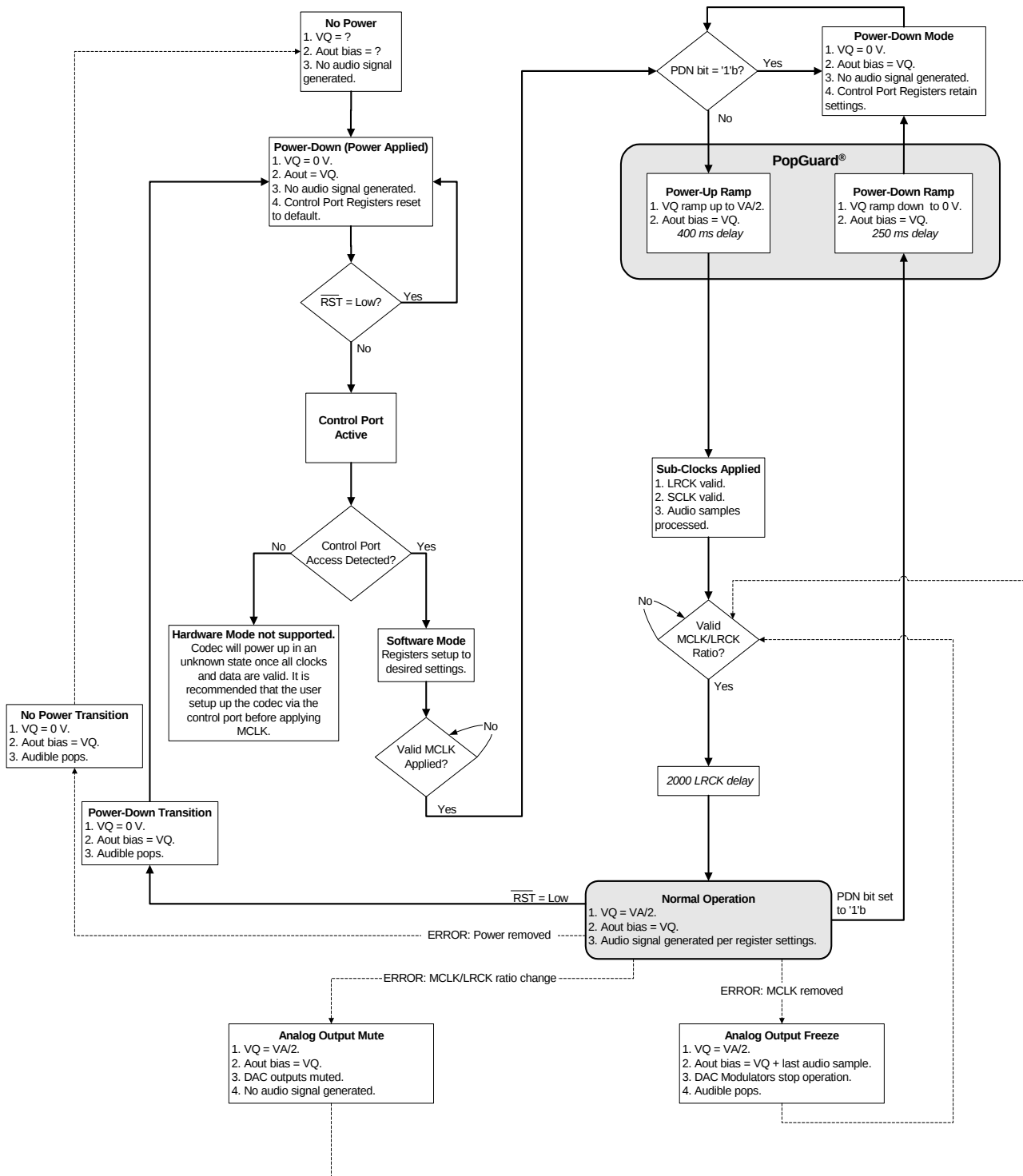


Figure 11. Audio Output Initialization Flow Chart

4.3.2 **Output Transient Control**

The 42888 uses Popguard technology to minimize the effects of output transients during power-up and power-down. This technique eliminates the audio transients commonly produced by single-ended single-supply converters when it is implemented with external DC-blocking capacitors connected in series with the audio outputs. To make best use of this feature, it is necessary to understand its operation. See [“Popguard” on page 27](#) for details.

A Mute Control pin is also available for use with an optional mute circuit to mask output transients on the analog outputs. See [“Mute Control” on page 27](#) for details.

When changing clock ratio or sample rate, it is recommended that zero data (or near zero data) be present on DAC_SDINx for at least 10 LRCK samples before the change is made. During the clocking change, the DAC outputs will always be in a zero-data state. If no zero audio is present at the time of switching, a slight click or pop may be heard as the DAC output automatically goes to its zero-data state.

4.3.3 **Popguard**

4.3.3.1 **Power-Up**

When the device is initially powered up, the audio outputs, AOUTxx, are clamped to VQ which is initially low. After the $\overline{\text{RST}}$ pin is brought high and MCLK is applied, the outputs begin to ramp with VQ towards the nominal quiescent voltage. This ramp takes approximately 400 ms to complete. The gradual voltage ramping allows time for the external DC-blocking capacitors to charge to VQ, effectively blocking the quiescent DC voltage. Once valid DAC_LRCK, DAC_SCLK and DAC_SDINx are applied, audio output begins approximately 2000 sample periods later.

4.3.3.2 **Power-Down**

To prevent audio transients at power-down, the DC-blocking capacitors must fully discharge before turning off the power. In order to do this, the PDN bit in register [“Power Control \(Address 02h\)” on page 41](#) must be set to ‘1’ for a period of about 250 ms before removing power. During this time, voltage on VQ and the audio outputs discharge gradually to AGND. If power is removed before this 250 ms time period has passed, a transient will occur when the VA supply drops below that of VQ. There is no minimum time for a power cycle. Power may be re-applied at any time.

4.3.4 **Mute Control**

The Mute Control pin, MUTE $\overline{\text{C}}$, is typically connected to an external mute control circuit. The use of external mute circuits is not mandatory, but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.

MUTE $\overline{\text{C}}$ is in high-impedance mode during power up or when the 42888 is in Power-Down Mode by setting the PDN bit in the register [“Power Control \(Address 02h\)” on page 41](#) to a ‘1’. Once out of Power-Down Mode, the pin can be controlled by the user via the control port (see [“MUTE \$\overline{\text{C}}\$ Pin Control \(Address 1Bh\)” on page 50](#)) or automatically asserted to the active state when zero data is present on all DAC inputs, when all DAC outputs are muted, or when serial port clock errors occur.

To prevent large transients on the output, it is recommended to mute the DAC outputs before the Mute Control pin is asserted.

4.3.5 Line-Level Outputs and Filtering

The CS42888 contains on-chip buffer amplifiers capable of producing line-level differential as well as single-ended outputs on AOUT1-AOUT8. These amplifiers are biased to a quiescent DC level of approximately V_Q.

The delta-sigma conversion process produces high-frequency noise beyond the audio passband, most of which is removed by the on-chip analog filters. The remaining out-of-band noise can be attenuated using an off-chip low-pass filter.

See [“DAC Output Filter” on page 53](#) for recommended output filter. The active filter configuration accounts for the normally differing AC loads on the AOUTx+ and AOUTx- differential output pins. Also shown is a passive filter configuration which minimizes costs and the number of components.

[Figure 12](#) shows the full-scale analog output levels. All outputs are internally biased to V_Q, approximately V_A/2.

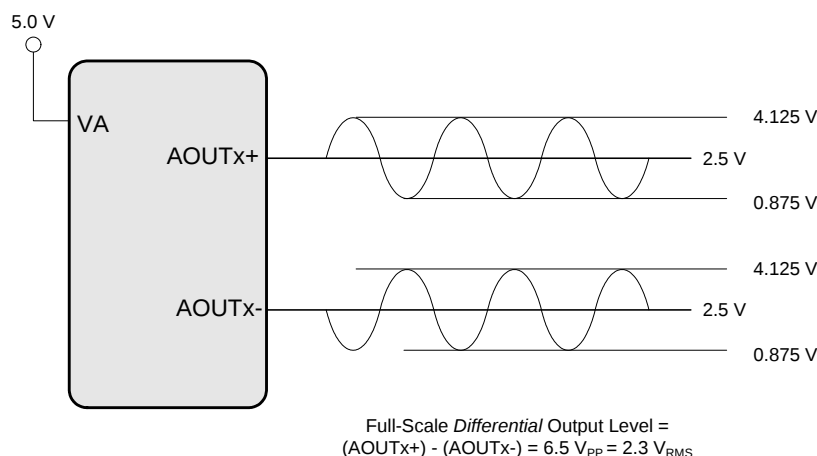


Figure 12. Full-Scale Output

4.3.6 Digital Volume Control

Each DAC's output level is controlled via the Volume Control registers operating over the range of 0 to -127.5 dB attenuation with 0.5 dB resolution. See [“AOUTX Volume Control \(Addresses 08h- 0Fh\)” on page 47](#). Volume control changes are programmable to ramp in increments of 0.125 dB at the rate controlled by the SZC[1:0] bits in the Digital Volume Control register. See [“Transition Control \(Address 06h\)” on page 45](#).

Each output can be independently muted via mute control bits in the register [“DAC Channel Mute \(Address 07h\)” on page 47](#). When enabled, each AOUTx_MUTE bit attenuates the corresponding DAC to its maximum value (-127.5 dB). When the AOUTx_MUTE bit is disabled, the corresponding DAC returns to the attenuation level set in the Volume Control register. The attenuation is ramped up and down at the rate specified by the SZC[1:0] bits.

4.3.7 De-Emphasis Filter

The CS42888 includes on-chip digital de-emphasis optimized for a sample rate of 44.1 kHz. The filter response is shown in [Figure 13](#). The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 μs pre-emphasis equalization as a means of noise reduction.

De-emphasis is only available in Single-Speed Mode. Please see [“DAC De-Emphasis Control \(DAC_DEM\)” on page 45](#) for de-emphasis control.

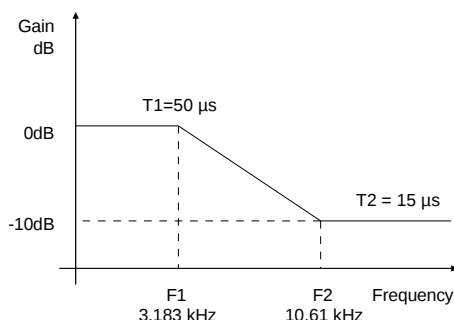


Figure 13. De-Emphasis Curve

4.4 System Clocking

The CODEC (ADC & DAC) serial audio interface ports operate both as a slave or master. The serial ports accept externally generated clocks in slave mode and will generate synchronous clocks derived from an input master clock in master mode. In the TDM format the ADC and DAC serial ports will only operate as a slave. In OLM #2 the serial ports will accept or output a 256Fs SCLK. See the registers [“DAC Functional Mode \(DAC_FM\[1:0\]\)” on page 42](#) and [“ADC Functional Mode \(ADC_FM\[1:0\]\)” on page 42](#) for setting up master/slave mode.

The CODEC requires external generation of the master clock (MCLK). The frequency of this clock must be an integer multiple of, and synchronous with, the system sample rate, Fs.

The required integer ratios, along with some common frequencies, are illustrated in tables [Tables 2 to 4](#). The frequency range of MCLK must be specified using the MFREQ bits in register [“MCLK Frequency \(MFREQ\[2:0\]\)” on page 42](#).

Sample Rate (kHz)	MCLK (MHz)				
	256x	384x	512x	768x	1024x
32	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	11.2896	16.9344	22.5792	33.8688	45.1584
48	12.2880	18.4320	24.5760	36.8640	49.1520

Table 2. Single-Speed Mode Common Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	128x	192x	256x	384x	512x
64	8.1920	12.2880	16.3840	24.5760	32.7680
88.2	11.2896	16.9344	22.5792	33.8688	45.1584
96	12.2880	18.4320	24.5760	36.8640	49.1520

Table 3. Double-Speed Mode Common Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	64x	96x	128x	192x	256x
176.4	11.2896	16.9344	22.5792	33.8688	45.1584
192	12.2880	18.4320	24.5760	36.8640	49.1520

Table 4. Quad-Speed Mode Common Frequencies

4.5 CODEC Digital Interface Formats

The ADC and DAC serial ports support the I²S, Left-Justified, Right-Justified, One-Line Mode (OLM) and TDM digital interface formats with varying bit depths from 16 to 32 as shown in [Figures 15-19](#). Data is clocked out of the ADC on the falling edge of SCLK and clocked into the DAC on the rising edge. The serial bit clock, DAC_SCLK and/or ADC_SCLK, must be synchronously derived from the master clock and be equal to 256x, 128x, 64x, 48x or 32x Fs, depending on the interface format selected and desired speed mode. One-Line Mode #1 and One-Line Mode #2 will operate in master or slave mode. Refer to [Table 5](#) for required clock ratios. The SCLK to sample rate (LRCK) ratios are shown in [Tables 5 through 8](#).

Ratio	I ² S, Left-Justified, Right-Justified		
	SSM	DSM	QSM
MCLK/LRCK	256x, 384x, 512x, 768x, 1024x	128x, 192x, 256x, 384x, 512x	64x, 96x, 128x, 192x, 256x
SCLK/LRCK (Slave Mode)	32x, 48x, 64x	32x, 48x, 64x	32x, 48x, 64x
SCLK/LRCK (Master Mode)	64x	64x	64x

Table 5. I²S, LJ, RJ Clock Ratios

	OLM #1		
	SSM	DSM	QSM
MCLK/LRCK	256x, 384x, 512x, 768x, 1024x	256x, 384x, 512x	N/A
SCLK/LRCK (Slave Mode)	128x	128x	N/A
SCLK/LRCK (Master Mode)	128x	128x	N/A

Table 6. OLM#1 Clock Ratios

	OLM #2		
	SSM	DSM	QSM
MCLK/LRCK	256x, 384x, 512x, 768x, 1024x	256x, 384x, 512x	N/A
SCLK/LRCK (Slave Mode)	256x	256x	N/A
SCLK/LRCK (Master Mode)	256x	256x	N/A

Table 7. OLM#2 Clock Ratios

	TDM		
	SSM	DSM	QSM (DAC only)
MCLK/LRCK	256x, 384x, 512x, 768x, 1024x	256x, 384x, 512x	256x
SCLK/LRCK (Slave Mode)	256X	256X	256X
SCLK/LRCK (Master Mode)	N/A	N/A	N/A

Table 8. TDM Clock Ratios

4.5.1 I²S

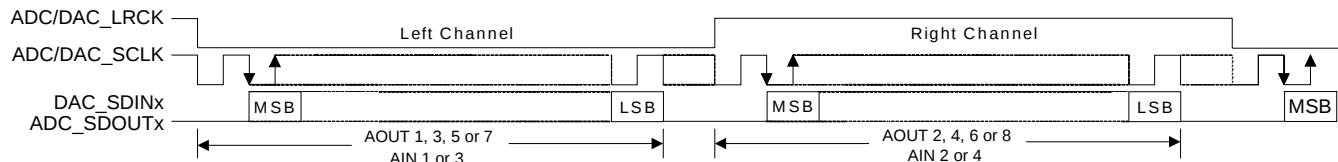


Figure 14. I²S Format

4.5.2 Left-Justified

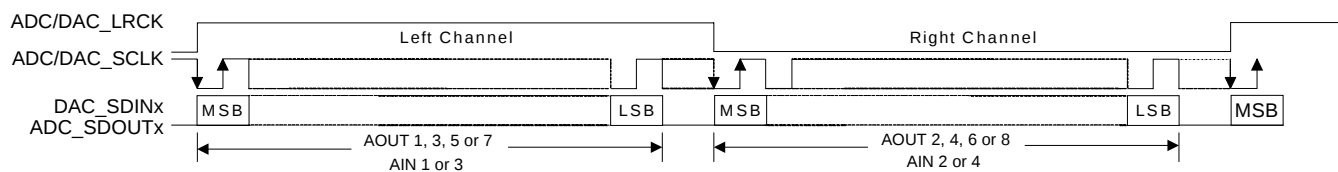


Figure 15. Left-Justified Format

4.5.3 Right-Justified

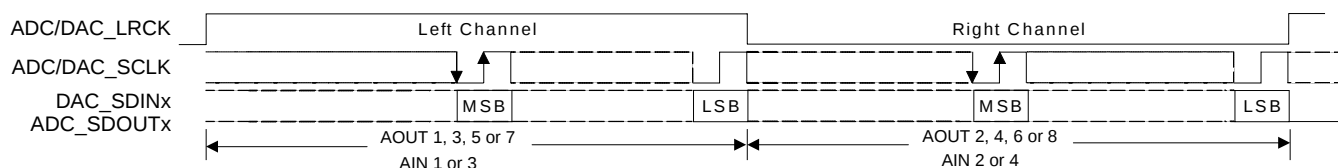


Figure 16. Right-Justified Format

4.5.4 OLM #1

OLM #1 serial audio interface format operates in Single- or Double-Speed Mode only and will master or slave ADC/DAC_SCLK at 128 Fs.

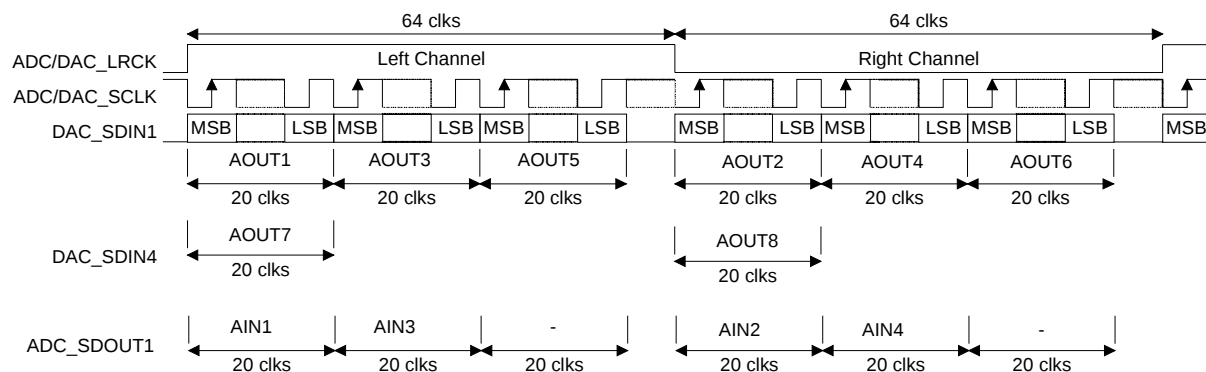


Figure 17. One-Line Mode #1 Format

4.5.5 OLM #2

OLM #2 serial audio interface format operates in Single- or Double-Speed Mode and will master or slave ADC/DAC_SCLK at 256Fs.

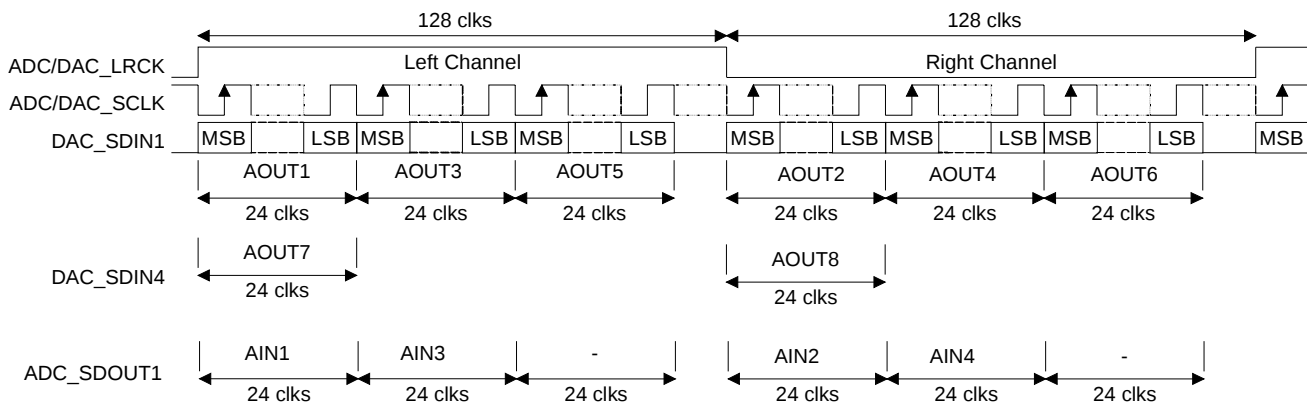


Figure 18. One-Line Mode #2 Format

4.5.6 TDM

TDM data is received most significant bit (MSB) first, on the second rising edge of the DAC_SCLK occurring after a DAC_LRCK rising edge. All data is valid on the rising edge of DAC_SCLK. The AIN1 MSB is transmitted early, but is guaranteed valid for a specified time after SCLK rises. All other bits are transmitted on the falling edge of ADC_SCLK. Each time slot is 32 bits wide, with the valid data sample left justified within the time slot. Valid data lengths are 16, 18, 20, or 24.

ADC/DAC_SCLK must operate at 256Fs. ADC/DAC_LRCK identifies the start of a new frame and is equal to the sample rate, Fs.

ADC/DAC_LRCK is sampled as valid on the rising ADC/DAC_SCLK edge preceding the most significant bit of the first data sample and must be held valid for at least 1 ADC/DAC_SCLK period.

Note: The ADC does not meet the timing requirements for proper operation in Quad-Speed Mode.

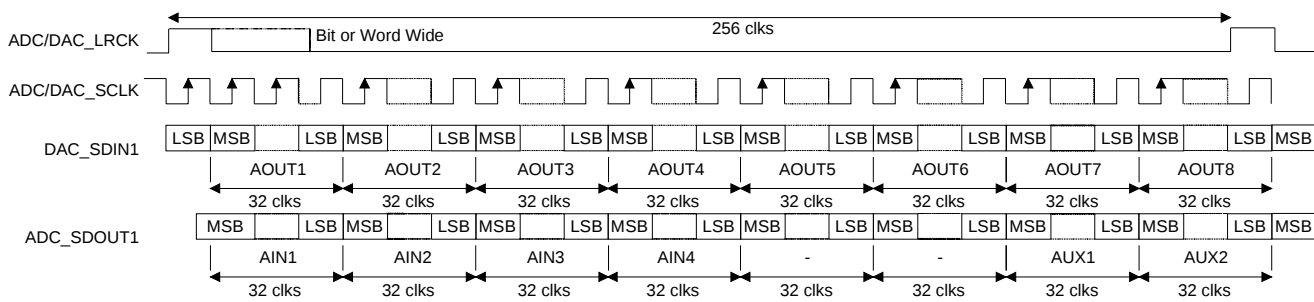


Figure 19. TDM Format

4.5.7 I/O Channel Allocation

Digital Input/Output	Interface Format	Analog Output/Input Channel Allocation from/to Digital I/O
DAC_SDIN1	I ² S, LJ, RJ OLM TDM	AOUT 1,2 AOUT 1,2,3,4,5,6 AOUT 1,2,3,4,5,6,7,8
ADC_SDOUT1	I ² S, LJ, RJ OLM TDM	AIN 1,2 AIN 1,2,3,4 AIN 1,2,3,4 (2 additional channels from AUX_SDIN)

Table 9. Serial Audio Interface Channel Allocations

4.6 AUX Port Digital Interface Formats

These serial data lines are used when supporting the TDM Mode of operation with an external ADC or S/PDIF receiver attached. The AUX serial port operates only as a clock master. The AUX_SCLK will operate at 64x F_s , where F_s is equal to the ADC sample rate (ADC_LRCK). If the AUX_SDIN signal is not being used, it should be tied to AGND via a pull-down resistor.

The AUX port will operate in either the Left-Justified or I²S digital interface format with bit depths ranging from 16 to 24 bits. Settings for the AUX port are made through the register “[Interface Formats \(Address 04h\)](#)” on page 43.

4.6.1 I²S

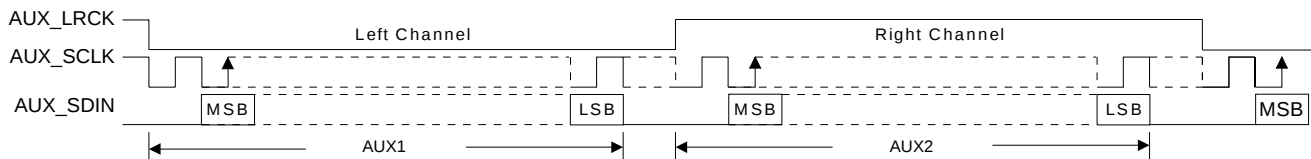


Figure 20. AUX I²S Format

4.6.2 Left-Justified

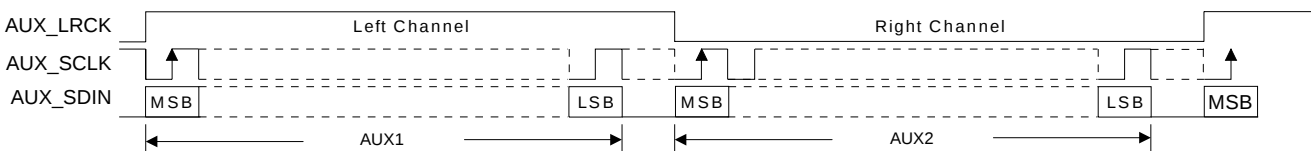


Figure 21. AUX Left-Justified Format

4.7 Control Port Description and Timing

The control port is used to access the registers allowing the CS42888 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has two modes: SPI and I²C, with the CS42888 acting as a slave device. SPI Mode is selected if there is a high-to-low transition on the AD0/CS pin, after the RST pin has been brought high. I²C Mode is selected by connecting the AD0/CS pin through a resistor to VLC or DGND, thereby permanently selecting the desired AD0 bit address state.

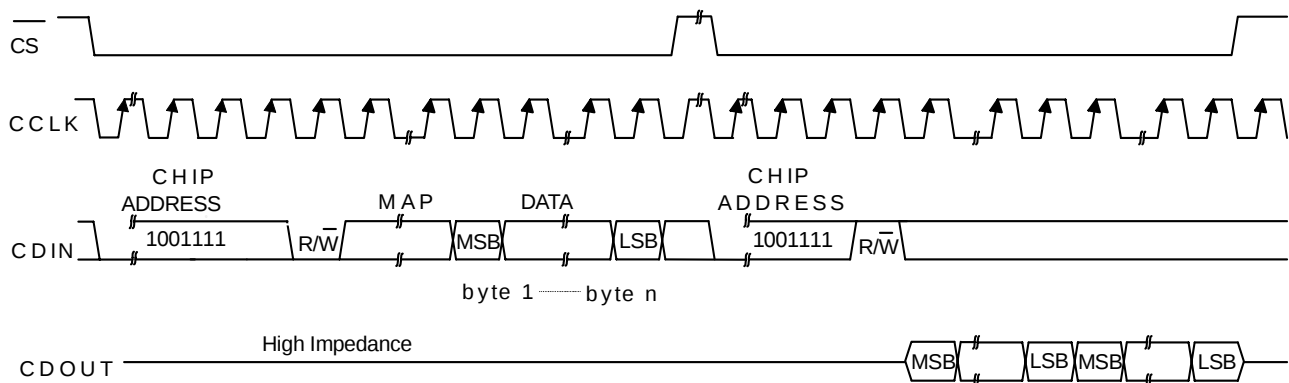
4.7.1 SPI Mode

In SPI Mode, $\overline{CS}$ is the CS42888 chip-select signal, CCLK is the control port bit clock (input into the CS42888 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 22 shows the operation of the control port in SPI Mode. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 1001111. The eighth bit is a read/write indicator ($R/\overline{W}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 k Ω resistor, if desired.

There is a MAP auto-increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{CS}$ high) immediately after the MAP byte. The MAP auto-increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{CS}$ low, send out the chip address and set the read/write bit ($R/\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto-increment bit is set to 1, the data for successive registers will appear consecutively.



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 22. Control Port Timing in SPI Mode

4.7.2 I²C Mode

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no $\overline{CS}$ pin. Pins AD0 and AD1 form the two least-significant bits of the chip address and should be connected through a resistor to VLC or DGND as desired. The state of the pins is sensed while the CS42888 is being reset.

The signal timings for a read and write cycle are shown in Figure 23 and Figure 24. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS42888 after a Start condition consists of a 7-bit chip address field and a $R/\overline{W}$ bit (high for a read, low

for a write). The upper 5 bits of the 7-bit address field are fixed at 10010. To communicate with a CS42888, the chip address field, which is the first byte sent to the CS42888, should match 10010 followed by the settings of the AD1 and AD0. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS42888 after each input byte is read, and is input to the CS42888 from the microcontroller after each transmitted byte.

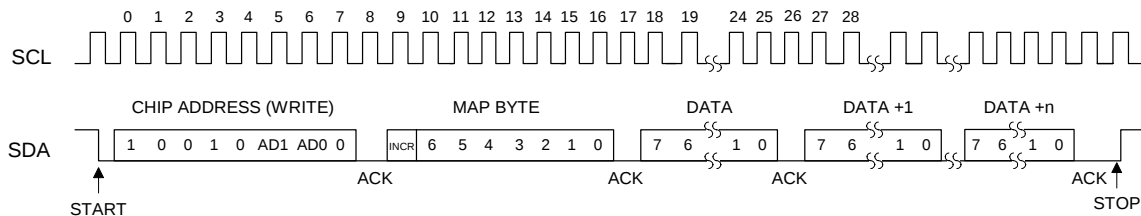


Figure 23. Control Port Timing, I²C Write

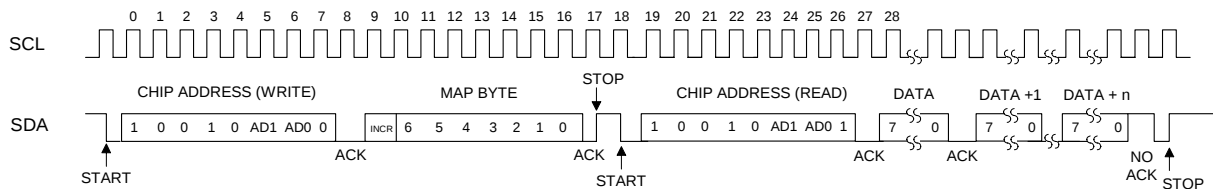


Figure 24. Control Port Timing, I²C Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 24, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 10010xx0 (chip address & write operation).

Receive acknowledge bit.

Send MAP byte, auto increment off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 10010xx1(chip address & read operation).

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto-increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

4.8 Interrupts

The 42888 has a comprehensive interrupt capability. The INT output pin is intended to drive the interrupt input pin on the host microcontroller. The INT pin may be configured as an active low or active high CMOS driver or an open-drain driver. This last mode is used for active low, wired-OR hook-ups, with multiple peripherals connected to the microcontroller interrupt input pin.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions. See [“Status \(Address 19h\) \(Read Only\)” on page 49](#). Each source may be masked off through mask register bits. In addition, each source may be set to rising edge, falling edge, or level sensitive. Combined with the option of level sensitive or edge sensitive modes within the microcontroller, many different configurations are possible, depending on the needs of the system designer.

4.9 Recommended Power-Up Sequence

1. Hold $\overline{\text{RST}}$ low until the power supply and clocks are stable. In this state, the control port is reset to its default settings and VQ will remain low.
2. Bring $\overline{\text{RST}}$ high. The device will initially be in a low power state with VQ low. All features will default as described in the [“Register Quick Reference” on page 38](#).
3. Perform a write operation to the Power Control register ([“Power Control \(Address 02h\)” on page 41](#)) to set bit 0 to a ‘1’b. This will place the device in a power down state.
4. Load the desired register settings while keeping the PDN bit set to ‘1’b.
5. Mute all DACs. Muting the DACs suppresses any noise associated with the CODEC’s first initialization after power is applied.
6. Set the PDN bit in the power control register to ‘0’b. VQ will ramp to approximately $V_A/2$ according to the Popguard specification in section [“Popguard” on page 27](#).
7. Following approximately 2000 LRCK cycles, the device is initialized and ready for normal operation.
8. After the CODEC is initialized, wait ~90 LRCK cycles (~1.9 ms @48 kHz) and then unmute the DACs.
9. Normal operation begins.

4.10 Reset and Power-Up

It is recommended that reset be activated if the analog or digital supplies drop below the recommended operating condition to prevent power-glitch-related issues.

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by setting the $\overline{\text{RST}}$ pin high. However, the voltage reference will take much longer to reach a final value due to the presence of external capacitance on the ADC/DAC_FILT+ pins. A time delay of approximately 400 ms is required after applying power to the device or after exiting a reset state. During this voltage reference ramp delay, all serial ports and DAC outputs will be automatically muted.

4.11 Power Supply, Grounding, and PCB Layout

As with any high-resolution converter, the CS42888 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. [Figure 2](#) shows the recommended power arrangements, with V_A connected to clean supplies. V_D , which powers the digital circuitry, may be run from the system logic supply. Alternatively, V_D may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from V_D .

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as near to the pins of the CS42888 as possible. The low value ceramic capacitor should be the nearest to the pin and should be mounted on the same

side of the board as the CS42888 to minimize inductance effects. All signals, especially clocks, should be kept away from the ADC/DAC_FILT+, VQ pins in order to avoid unwanted coupling into the modulators. The ADC/DAC_FILT+ and VQ decoupling capacitors, particularly the 0.1 μ F, must be positioned to minimize the electrical path from ADC/DAC_FILT+ and AGND. The CDB42448 evaluation board demonstrates the optimum layout and power supply arrangements.

For optimal heat dissipation from the package, it is recommended that the area directly under the part be filled with copper and tied to the ground plane. The use of vias connecting the topside ground to the backside ground is also recommended.

5. REGISTER QUICK REFERENCE

Note: The default value in all "Reserved" registers must be preserved.

Addr	Function	7	6	5	4	3	2	1	0
01h	ID p 40 default	Chip_ID3 0	Chip_ID2 0	Chip_ID1 0	Chip_ID0 0	Rev_ID3 0	Rev_ID2 0	Rev_ID1 0	Rev_ID0 1
02h	Power Control p 41 default	Reserved 0	PDN_ADC2 0	PDN_ADC1 0	PDN_DAC4 0	PDN_DAC3 0	PDN_DAC2 0	PDN_DAC1 0	PDN 0
03h	Functional Mode p 42 default	DAC_FM1 1	DAC_FM0 1	ADC_FM1 1	ADC_FM0 1	MFreq2 0	MFreq1 0	MFreq0 0	Reserved 0
04h	Interface Formats p 43 default	FREEZE 0	AUX_DIF 0	DAC_DIF2 1	DAC_DIF1 1	DAC_DIF0 0	ADC_DIF2 1	ADC_DIF1 1	ADC_DIF0 0
05h	ADC Control (w/DAC_DEM) p 44 default	ADC1-2_HP FREEZE 0	Reserved 0	DAC_DEM 0	ADC1 SINGLE 0	ADC2 SINGLE 0	Reserved 0	Reserved 0	Reserved 0
06h	Transition Control p 45 default	DAC_SNG VOL 0	DAC_SZC1 0	DAC_SZC0 0	AMUTE 1	MUTE ADC_SP 0	ADC_SNG VOL 0	ADC_SZC1 0	ADC_SZC0 0
07h	Channel Mute p 47 default	AOUT8 MUTE 0	AOUT7 MUTE 0	AOUT6 MUTE 0	AOUT5 MUTE 0	AOUT4 MUTE 0	AOUT3 MUTE 0	AOUT2 MUTE 0	AOUT1 MUTE 0
08h	Vol. Control AOUT1 p 47 default	AOUT1 VOL7 0	AOUT1 VOL6 0	AOUT1 VOL5 0	AOUT1 VOL4 0	AOUT1 VOL3 0	AOUT1 VOL2 0	AOUT1 VOL1 0	AOUT1 VOL0 0
09h	Vol. Control AOUT2 p 47 default	AOUT2 VOL7 0	AOUT2 VOL6 0	AOUT2 VOL5 0	AOUT2 VOL4 0	AOUT2 VOL3 0	AOUT2 VOL2 0	AOUT2 VOL1 0	AOUT2 VOL0 0
0Ah	Vol. Control AOUT3 p 47 default	AOUT3 VOL7 0	AOUT3 VOL6 0	AOUT3 VOL5 0	AOUT3 VOL4 0	AOUT3 VOL3 0	AOUT3 VOL2 0	AOUT3 VOL1 0	AOUT3 VOL0 0
0Bh	Vol. Control AOUT4 p 47 default	AOUT4 VOL7 0	AOUT4 VOL6 0	AOUT4 VOL5 0	AOUT4 VOL4 0	AOUT4 VOL3 0	AOUT4 VOL2 0	AOUT4 VOL1 0	AOUT4 VOL0 0
0Ch	Vol. Control AOUT5 p 47 default	AOUT5 VOL7 0	AOUT5 VOL6 0	AOUT5 VOL5 0	AOUT5 VOL4 0	AOUT5 VOL3 0	AOUT5 VOL2 0	AOUT5 VOL1 0	AOUT5 VOL0 0
0Dh	Vol. Control AOUT6 p 47 default	AOUT6 VOL7 0	AOUT6 VOL6 0	AOUT6 VOL5 0	AOUT6 VOL4 0	AOUT6 VOL3 0	AOUT6 VOL2 0	AOUT6 VOL1 0	AOUT6 VOL0 0
0Eh	Vol. Control AOUT7 p 47 default	AOUT7 VOL7 0	AOUT7 VOL6 0	AOUT7 VOL5 0	AOUT7 VOL4 0	AOUT7 VOL3 0	AOUT7 VOL2 0	AOUT7 VOL1 0	AOUT7 VOL0 0
0Fh	Vol. Control AOUT8 p 47 default	AOUT8 VOL7 0	AOUT8 VOL6 0	AOUT8 VOL5 0	AOUT8 VOL4 0	AOUT8 VOL3 0	AOUT8 VOL2 0	AOUT8 VOL1 0	AOUT8 VOL0 0
10h	DAC Channel Invert p 48 default	INV_AOUT8 0	INV_AOUT7 0	INV_AOUT6 0	INV_AOUT5 0	INV_AOUT4 0	INV_AOUT3 0	INV_AOUT2 0	INV_AOUT1 0

Addr	Function	7	6	5	4	3	2	1	0
11h	Vol. Control AIN1 p 47 default	AIN1 VOL7 0	AIN1 VOL6 0	AIN1 VOL5 0	AIN1 VOL4 0	AIN1 VOL3 0	AIN1 VOL2 0	AIN1 VOL1 0	AIN1 VOL0 0
12h	Vol. Control AIN2 p 48 default	AIN2 VOL7 0	AIN2 VOL6 0	AIN2 VOL5 0	AIN2 VOL4 0	AIN2 VOL3 0	AIN2 VOL2 0	AIN2 VOL1 0	AIN2 VOL0 0
13h	Vol. Control AIN3 p 47 default	AIN3 VOL7 0	AIN3 VOL6 0	AIN3 VOL5 0	AIN3 VOL4 0	AIN3 VOL3 0	AIN3 VOL2 0	AIN3 VOL1 0	AIN3 VOL0 0
14h	Vol. Control AIN4 p 48 default	AIN4 VOL7 0	AIN4 VOL6 0	AIN4 VOL5 0	AIN4 VOL4 0	AIN4 VOL3 0	AIN4 VOL2 0	AIN4 VOL1 0	AIN4 VOL0 0
15h	Reserved default	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
16h	Reserved default	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
17h	ADC Chan- nel Invert p 48 default	Reserved 0	Reserved 0	Reserved 0	Reserved 0	INV_A4 0	INV_A3 0	INV_A2 0	INV_A1 0
18h	Status Con- trol p 49 default	Reserved 0	Reserved 0	Reserved 0	Reserved 0	INT1 0	INT0 0	Reserved 0	Reserved 0
19h	Status p 49 default	Reserved 0	Reserved 0	Reserved 0	DAC_CLK Error X	ADC_CLK Error X	Reserved X	ADC2 OVFL X	ADC1 OVFL X
1Ah	Status Mask p 50 default	Reserved 0	Reserved 0	Reserved 0	DAC_CLK Error_M 0	ADC_CLK Error_M 0	Reserved 0	ADC2 OVFL_M 0	ADC1 OVFL_M 0

6. REGISTER DESCRIPTION

All registers are read/write except for the I.D. and Revision Register and Interrupt Status Register which are read only. See the following bit-definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description.

6.1 Memory Address Pointer (MAP)

Not a register

7	6	5	4	3	2	1	0
INCR	MAP6	MAP5	MAP4	MAP3	MAP2	MAP1	MAP0

6.1.1 Increment (INCR)

Default = 1

Function:

Memory address pointer auto increment control

0 - MAP is not incremented automatically.

1 - Internal MAP is automatically incremented after each read or write.

6.1.2 Memory Address Pointer (MAP[6:0])

Default = 0000001

Function:

Memory address pointer (MAP). Sets the register address that will be read or written by the control port.

6.2 Chip I.D. and Revision Register (Address 01h) (Read Only)

7	6	5	4	3	2	1	0
Chip_ID3	Chip_ID2	Chip_ID1	Chip_ID0	Rev_ID3	Rev_ID2	Rev_ID1	Rev_ID0

6.2.1 Chip I.D. (CHIP_ID[3:0])

Default = 0000

Function:

I.D. code for the CS42888. Permanently set to 0000.

6.2.2 Chip Revision (REV_ID[3:0])

Default = 0001

Function:

CS42888 revision level. Revision A is coded as 0001.

6.3 Power Control (Address 02h)

7	6	5	4	3	2	1	0
Reserved	PDN_ADC2	PDN_ADC1	PDN_DAC4	PDN_DAC3	PDN_DAC2	PDN_DAC1	PDN

6.3.1 Power Down ADC Pairs (PDN_ADCX)

Default = 0

0 - Disable

1 - Enable

Function:

When enabled, the respective ADC channel pair (ADC1 - AIN1/AIN2; and ADC2 - AIN3/AIN4) will remain in a reset state.

6.3.2 Power Down DAC Pairs (PDN_DACX)

Default = 0

0 - Disable

1 - Enable

Function:

When enabled, the respective DAC channel pair (DAC1 - AOUT1/AOUT2; DAC2 - AOUT3/AOUT4; DAC3 - AOUT5/AOUT6; and DAC4 - AOUT7/AOUT8) will remain in a reset state. It is advised that any change of these bits be made while the DACs are muted or the power down bit (PDN) is enabled to eliminate the possibility of audible artifacts.

6.3.3 Power Down (PDN)

Default = 0

0 - Disable

1 - Enable

Function:

The entire device will enter a low-power state when this function is enabled. The contents of the control registers are retained in this mode.

6.4 Functional Mode (Address 03h)

7	6	5	4	3	2	1	0
DAC_FM1	DAC_FM0	ADC_FM1	ADC_FM0	MFreq2	MFreq1	MFreq0	Reserved

6.4.1 DAC Functional Mode (DAC_FM[1:0])

Default = 11

Master Mode

00 - Single-Speed Mode (4 to 50 kHz sample rates)

01 - Double-Speed Mode (50 to 100 kHz sample rates)

10 - Quad-Speed Mode (100 to 200 kHz sample rates)

Slave Mode

11 - (Auto-detect sample rates)

Function:

Selects the required range of sample rates for the DAC serial port.

6.4.2 ADC Functional Mode (ADC_FM[1:0])

Default = 11

Master Mode

00 - Single-Speed Mode (4 to 50 kHz sample rates)

01 - Double-Speed Mode (50 to 100 kHz sample rates)

10 - Quad-Speed Mode (100 to 200 kHz sample rates)

Slave Mode

11 - (Auto-detect sample rates)

Function:

Selects the required range of sample rates for the ADC serial port.

6.4.3 MCLK Frequency (MFREQ[2:0])

Default = 000

Function:

Sets the appropriate frequency for the supplied MCLK. For TDM and OLM #2 operation, ADC/DAC_SCLK must equal 256Fs. For OLM #1 operation, ADC/DAC_SCLK must equal 128Fs. MCLK can be equal to or greater than the higher frequency of ADC_SCLK or DAC_SCLK.

				Ratio (xFs)		
MFreq2	MFreq1	MFreq0	Description	SSM	DSM	QSM
0	0	0	1.0290 MHz to 12.8000 MHz	256	128	64
0	0	1	1.5360 MHz to 19.2000 MHz	384	192	96
0	1	0	2.0480 MHz to 25.6000 MHz	512	256	128
0	1	1	3.0720 MHz to 38.4000 MHz	768	384	192
1	X	X	4.0960 MHz to 51.2000 MHz	1024	512	256

Table 10. MCLK Frequency Settings for I²S, Left and Right Justified Interface Formats

				Ratio (xFs)		
MFreq2	MFreq1	MFreq0	Description	SSM	DSM	QSM
0	0	0	1.0290 MHz to 12.8000 MHz	256	N/A	N/A
0	0	1	1.5360 MHz to 19.2000 MHz	384	N/A	N/A
0	1	0	2.0480 MHz to 25.6000 MHz	512	256	N/A
0	1	1	3.0720 MHz to 38.4000 MHz	768	384	N/A
1	X	X	4.0960 MHz to 51.2000 MHz	1024	512	256

Table 11. MCLK Frequency Settings for TDM & OLM Interface Formats

6.5 Interface Formats (Address 04h)

7	6	5	4	3	2	1	0
FREEZE	AUX_DIF	DAC_DIF2	DAC_DIF1	DAC_DIF0	ADC_DIF2	ADC_DIF1	ADC_DIF0

6.5.1 Freeze Controls (FREEZE)

Default = 0

Function:

This function will freeze the previous settings of, and allow modifications to be made to the channel mutes, the DAC and ADC Volume Control/Channel Invert registers without the changes taking effect until the FREEZE is disabled. To have multiple changes in these control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

6.5.2 Auxiliary Digital Interface Format (AUX_DIF)

Default = 0

0 - Left Justified
 1 - I²S

Function:

This bit selects the digital interface format used for the AUX Serial Port. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in [Figures 22-23](#).

6.5.3 DAC Digital Interface Format (DAC_DIF[2:0])

Default = 110

Function:

These bits select the digital interface format used for the DAC Serial Port. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format; the options are detailed in the section "[CODEC Digital Interface Formats](#)" on page 30.

Refer to [Table 9, "Serial Audio Interface Channel Allocations,"](#) on page 33.

DAC_DIF2	DAC_DIF1	DAC_DIF0	Description	Format	Figure
0	0	0	Left Justified, up to 24-bit data	0	Figure 15
0	0	1	I ² S, up to 24-bit data	1	Figure 14
0	1	0	Right Justified, 24-bit data	2	Figure 16

Table 12. DAC Digital Interface Formats

DAC_DIF2	DAC_DIF1	DAC_DIF0	Description	Format	Figure
0	1	1	Right Justified, 16-bit data	3	Figure 16
1	0	0	One-Line #1, 20-bit	4	Figure 17
1	0	1	One-Line #2, 24-bit	5	Figure 18
1	1	0	TDM Mode, 24-bit (slave only)	6	Figure 19
1	1	1	Reserved	-	-

Table 12. DAC Digital Interface Formats

6.5.4 ADC Digital Interface Format (ADC_DIF[2:0])

Default = 110

Function:

These bits select the digital interface format used for the ADC serial port. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in the section “CODEC Digital Interface Formats” on page 30. Refer to [Table 9, “Serial Audio Interface Channel Allocations,”](#) on page 33.

Note: The ADC does not meet Quad-Speed Mode timing specifications in the TDM interface format.

ADC_DIF2	ADC_DIF1	ADC_DIF0	Description	Format	Figure
0	0	0	Left Justified, up to 24-bit data	0	Figure 15
0	0	1	I²S, up to 24-bit data	1	Figure 14
0	1	0	Right Justified, 24-bit data	2	Figure 16
0	1	1	Right Justified, 16-bit data	3	Figure 16
1	0	0	One-Line #1, 20-bit	4	Figure 17
1	0	1	One-Line #2, 24-bit	5	Figure 18
1	1	0	TDM Mode, 24-bit (slave only)	6	Figure 19
1	1	1	Reserved	-	-

Table 13. ADC Digital Interface Formats

6.6 ADC Control & DAC De-Emphasis (Address 05h)

7	6	5	4	3	2	1	0
ADC1-2_HP FREEZE	Reserved	DAC_DEM	ADC1 SINGLE	ADC2 SINGLE	Reserved	Reserved	Reserved

6.6.1 ADC1-2 High-Pass Filter Freeze (ADC1-2_HP FREEZE)

Default = 0

Function:

When this bit is set, the internal high-pass filter will be disabled for ADC1 and ADC2. The current DC offset value will be frozen and continue to be subtracted from the conversion result. See “[ADC Digital Filter Characteristics](#)” on page 13.

6.6.2 DAC De-Emphasis Control (DAC_DEM)

Default = 0

0 - No De-Emphasis

1 - De-Emphasis Enabled (Auto-Detect Fs)

Function:

Enables the digital filter to maintain the standard 15 μ s/50 μ s digital de-emphasis filter response at the auto-detected sample rate of either 32, 44.1, or 48 kHz. De-emphasis will not be enabled, regardless of this register setting, at any other sample rate.

6.6.3 ADC1 Single-Ended Mode (ADC1 SINGLE)

Default = 0

0 - Disabled; Differential input to ADC1

1 - Enabled; Single-Ended input to ADC1

Function:

When enabled, this bit allows the user to apply a single-ended input to the positive terminal of ADC1. A +6 dB digital gain is automatically applied to the serial audio data of ADC1. The negative leg must be driven to the common mode of the ADC. See [Figure 26 on page 51](#) for a graphical description.

6.6.4 ADC2 Single-Ended Mode (ADC2 SINGLE)

Default = 0

0 - Disabled; Differential input to ADC2

1 - Enabled; Single-Ended input to ADC2

Function:

When enabled, this bit allows the user to apply a single-ended input to the positive terminal of ADC2. A +6 dB digital gain is automatically applied to the serial audio data of ADC2. The negative leg must be driven to the common mode of the ADC. See [Figure 26 on page 51](#) for a graphical description.

6.7 Transition Control (Address 06h)

7	6	5	4	3	2	1	0
DAC_SNGVOL	DAC_SZC1	DAC_SZC0	AMUTE	MUTE ADC_SP	ADC_SNGVOL	ADC_SZC1	ADC_SZC0

6.7.1 Single Volume Control (DAC_SNGVOL, ADC_SNGVOL)

Default = 0

Function:

The individual channel volume levels are independently controlled by their respective Volume Control registers when this function is disabled. When enabled, the volume on all channels is determined by the AOUT1 and AIN1 Volume Control register and the other Volume Control registers are ignored.

6.7.2 **Soft Ramp and Zero Cross Control (ADC_SZC[1:0], DAC_SZC[1:0])**

Default = 00

00 - Immediate Change

01 - Zero Cross

10 - Soft Ramp

11 - Soft Ramp on Zero Crossings

Function:

Immediate Change

When Immediate Change is selected, all volume-level changes will take effect immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by gain changes, attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp

Soft Ramp allows level changes, either by gain changes, attenuation changes or muting, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Soft Ramp on Zero Crossing

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by gain changes, attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

6.7.3 **Auto-Mute (AMUTE)**

Default = 1

0 - Disabled

1 - Enabled

Function:

The Digital-to-Analog converters of the CS42888 will mute the output following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the MUTE pin will go active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits (SZC[1:0]).

6.7.4 Mute ADC Serial Port (MUTE_ADC_SP)

Default = 0

0 - Disabled

1 - Enabled

Function:

When enabled, the ADC Serial Port will be muted.

6.8 DAC Channel Mute (Address 07h)

7	6	5	4	3	2	1	0
AOUT8_MUTE	AOUT7_MUTE	AOUT6_MUTE	AOUT5_MUTE	AOUT4_MUTE	AOUT3_MUTE	AOUT2_MUTE	AOUT1_MUTE

6.8.1 Independent Channel Mute (AOUTX_MUTE)

Default = 0

0 - Disabled

1 - Enabled

Function:

The respective Digital-to-Analog converter outputs of the CS42888 will mute when enabled. The quiescent voltage on the outputs will be retained. The muting function is affected by the DAC Soft and Zero Cross bits (DAC_SZC[1:0]). When all channels are muted, the MUTE pin will become active.

6.9 AOUTX Volume Control (Addresses 08h- 0Fh)

7	6	5	4	3	2	1	0
AOUTx_VOL7	AOUTx_VOL6	AOUTx_VOL5	AOUTx_VOL4	AOUTx_VOL3	AOUTx_VOL2	AOUTx_VOL1	AOUTx_VOL0

6.9.1 Volume Control (AOUTX_VOL[7:0])

Default = 00h

Function:

The AOUTx Volume Control registers allow independent setting of the signal levels in 0.5 dB increments from 0 dB to -127.5 dB. Volume settings are decoded as shown in Table 14. The volume changes are implemented as dictated by the Soft and Zero Cross bits (DAC_SZC[1:0]). All volume settings less than -127.5 dB are equivalent to enabling the AOUTx_MUTE bit for the given channel.

Binary Code	Volume Setting
00000000	0 dB
00101000	-20 dB
01010000	-40 dB
01111000	-60 dB
10110100	-90 dB

Table 14. Example AOUT Volume Settings

6.10 DAC Channel Invert (Address 10h)

7	6	5	4	3	2	1	0
INV_AOUT8	INV_AOUT7	INV_AOUT6	INV_AOUT5	INV_AOUT4	INV_AOUT3	INV_AOUT2	INV_AOUT1

6.10.1 Invert Signal Polarity (INV_AOUTX)

Default = 0

0 - Disabled

1 - Enabled

Function:

When enabled, these bits will invert the signal polarity of their respective channels.

6.11 AINX Volume Control (Address 11h-14h)

7	6	5	4	3	2	1	0
AINx_VOL7	AINx_VOL6	AINx_VOL5	AINx_VOL4	AINx_VOL3	AINx_VOL2	AINx_VOL1	AINx_VOL0

6.11.1 AINX Volume Control (AINX_VOL[7:0])

Default = 00h

Function:

The level of AIN1 - AIN6 can be adjusted in 0.5 dB increments as dictated by the ADC Soft and Zero Cross bits (ADC_SZC[1:0]) from +24 to -64 dB. Levels are decoded in two's complement, as shown in [Table 15](#).

Binary Code	Volume Setting
0111 1111	+24 dB
...	...
0011 0000	+24 dB
...	...
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1 dB
...	...
1000 0000	-64 dB

Table 15. Example AIN Volume Settings

6.12 ADC Channel Invert (Address 17h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	INV_AIN4	INV_AIN3	INV_AIN2	INV_AIN1

6.12.1 Invert Signal Polarity (INV_AINX)

Default = 0

0 - Disabled

1 - Enabled

Function:

6.13 When enabled, these bits will invert the signal polarity of their respective channels. **Status Control (Address 18h)**

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	INT1	INT0	Reserved	Reserved

6.13.1 Interrupt Pin Control (INT[1:0])

Default = 00

00 - Active high; high output indicates interrupt condition has occurred

01 - Active low, low output indicates an interrupt condition has occurred

10 - Open drain, active low. Requires an external pull-up resistor on the INT pin.

11 - Reserved

Function:

Determines how the Interrupt pin (INT) will indicate an interrupt condition.

For DAC and ADC clock errors, the INT pin is set to "Level Active Mode" and will become active *during* the clock error. For the ADCx_OVFL error, the INT pin is set to Level Active Mode and will become active *during* the overflow error.

6.14 Status (Address 19h) (Read Only)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	DAC_CLK Error	ADC_CLK Error	Reserved	ADC2_OVFL	ADC1_OVFL

For all bits in this register, a "1" means the associated error condition has occurred at least once since the register was last read. A "0" means the associated error condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0. Status bits that are masked off in the associated mask register will always be "0" in this register.

6.14.1 DAC CLOCK ERROR (DAC_CLK ERROR)

Default = x

Function:

Indicates an invalid MCLK to DAC_LRCK ratio. This status flag is set to "Level Active Mode" and becomes active *during* the error condition. See ["System Clocking" on page 29](#) for valid clock ratios.

6.14.2 ADC CLOCK ERROR (ADC_CLK ERROR)

Default = x

Function:

Indicates an invalid MCLK to ADC_LRCK ratio. This status flag is set to “Level Active Mode” and becomes active *during* the error condition. See [“System Clocking” on page 29](#) for valid clock ratios.

6.14.3 ADC Overflow (ADCX_OVFL)

Default = x

Function:

Indicates that there is an over-range condition anywhere in the CS42888 ADC signal path of each of the associated ADC’s. These status flags become active on the *arrival* of the error condition.

6.15 Status Mask (Address 1Ah)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	DAC_CLK Error_M	ADC_CLK Error_M	Reserved	ADC2_OVFL_M	ADC1_OVFL_M

Default = 00000

Function:

The bits of this register serve as a mask for the error sources found in the register [“Status \(Address 19h\) \(Read Only\)” on page 49](#). If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the INT pin or the status register. The bit positions align with the corresponding bits in the Status register.

6.16 MUTEK Pin Control (Address 1Bh)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCPolarity	MUTEK ACTIVE

6.17 MUTEK Polarity Select (MCPOLARITY)

Default = 0

0 - Active low

1 - Active high

Function:

Determines the polarity of the MUTEK pin.

6.18 MUTE CONTROL ACTIVE (MUTEK ACTIVE)

Default = 0

0 - MUTEK pin is not active.

1 - MUTEK pin is active.

Function:

The MUTEK pin will go high or low (depending on the MUTEK Polarity Select bit) when this bit is enabled.

7.1.1 Passive Input Filter

The passive filter implementation shown in Figure 27 will attenuate any noise energy at 6.144 MHz but will not provide optimum source impedance for the ADC modulators. Full analog performance will therefore not be realized using a passive filter. Figure 27 illustrates the unity gain, passive input filter solution. In this topology the distortion performance is affected, but the dynamic range performance is not limited.

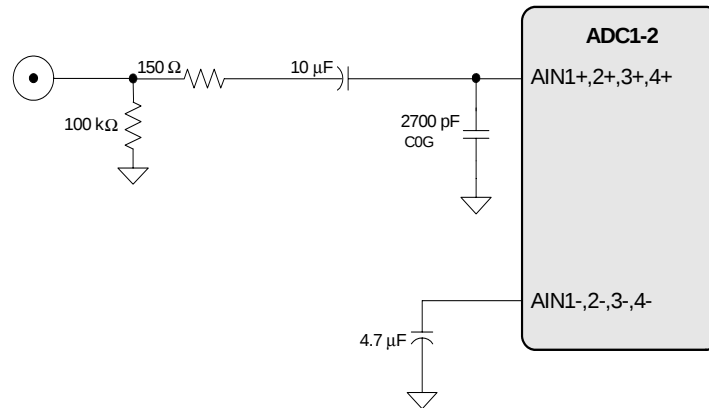


Figure 27. Passive Input Filter

7.1.2 Passive Input Filter w/Attenuation

Some applications may require signal attenuation prior to the ADC. The full-scale input voltage will scale with the analog power supply voltage. For $V_A = 5.0\text{ V}$, the full-scale input voltage is approximately 2.8 Vpp, or 1 Vrms (most consumer audio line-level outputs range from 1.5 to 2 Vrms).

Figure 28 shows a passive input filter with 6 dB of signal attenuation. Due to the relatively high input impedance on the analog inputs, the full distortion performance cannot be realized. Also, the resistor divider circuit will determine the input impedance into the input filter. In the circuit shown in Figure 28, the input impedance is approximately 5 kΩ. By doubling the resistor values, the input impedance will increase to 10 kΩ. However, in this case the distortion performance will drop due to the increase in series resistance on the analog inputs.

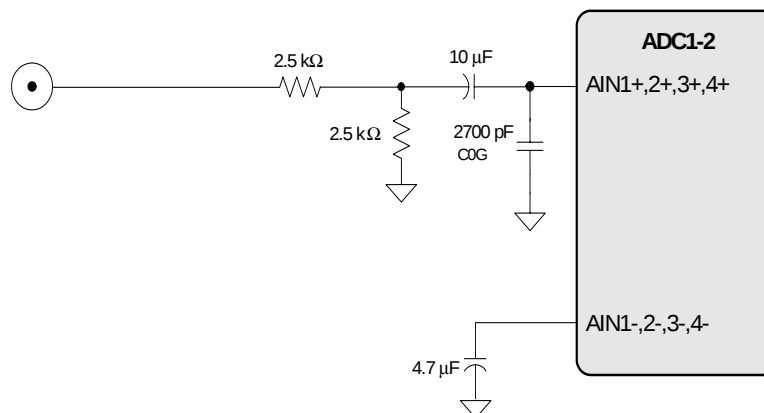


Figure 28. Passive Input Filter w/Attenuation

7.2 DAC Output Filter

The CS42888 is a linear phase design and does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry. Shown below is the recommended active and passive output filters.

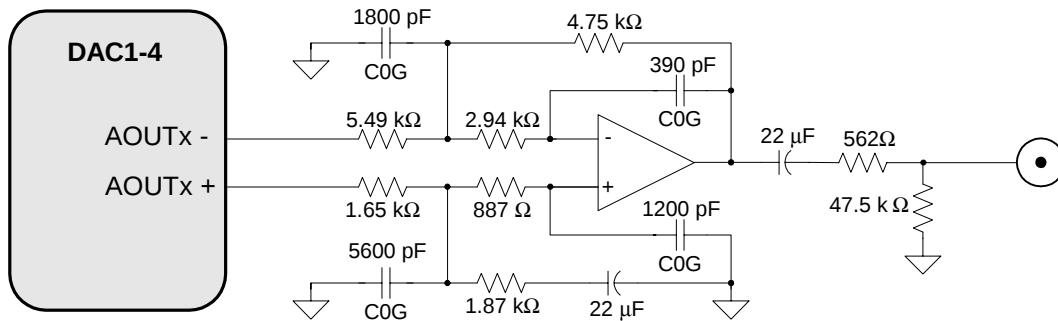


Figure 29. Active Analog Output Filter

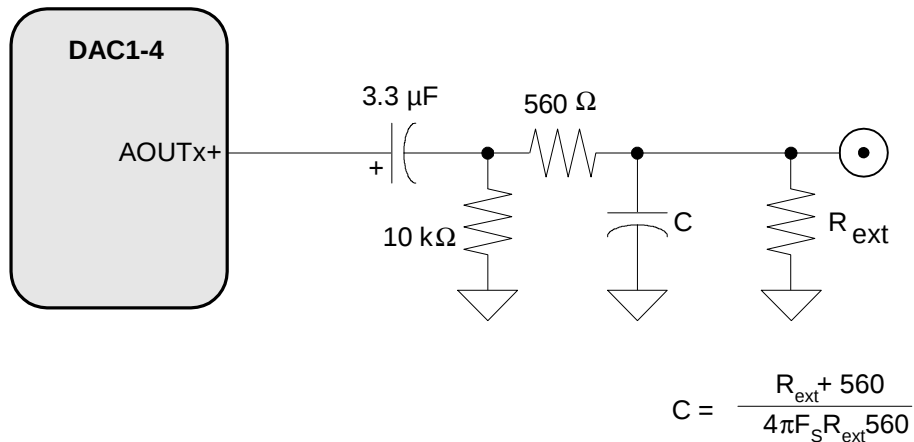


Figure 30. Passive Analog Output Filter

8. ADC FILTER PLOTS

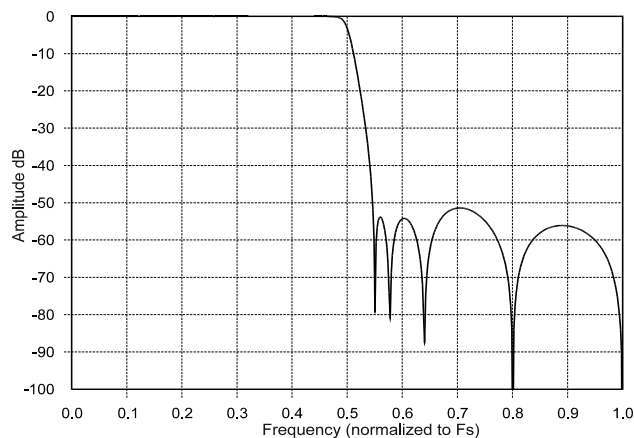


Figure 31. SSM Stopband Rejection

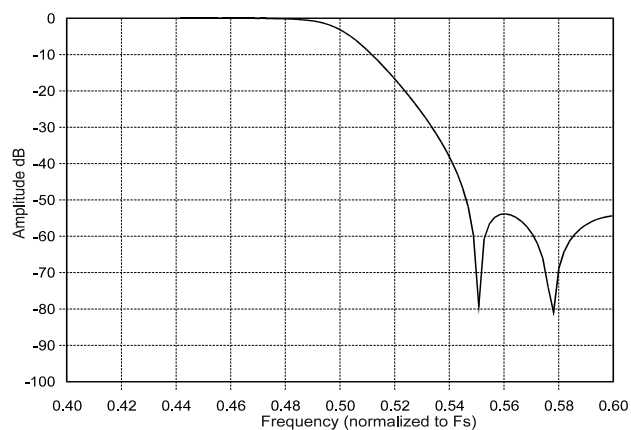


Figure 32. SSM Transition Band

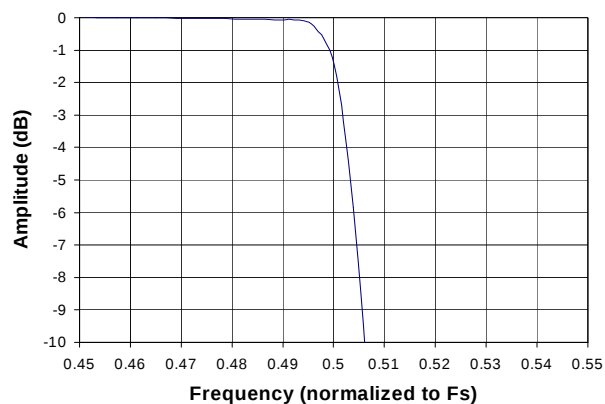


Figure 33. SSM Transition Band (Detail)

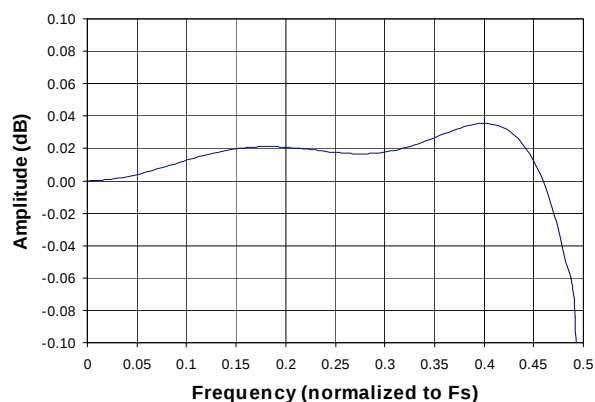


Figure 34. SSM Passband Ripple

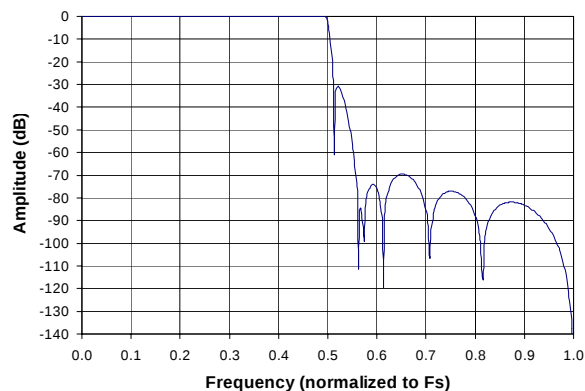


Figure 35. DSM Stopband Rejection

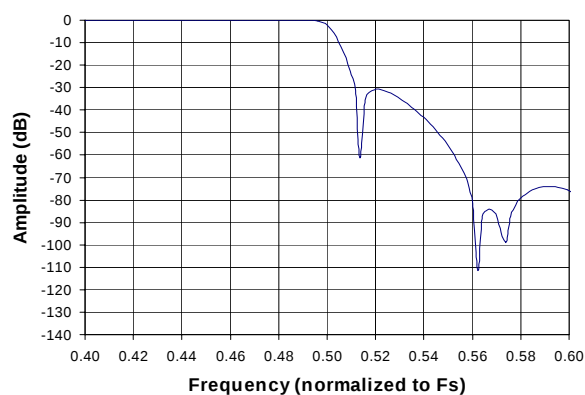


Figure 36. DSM Transition Band

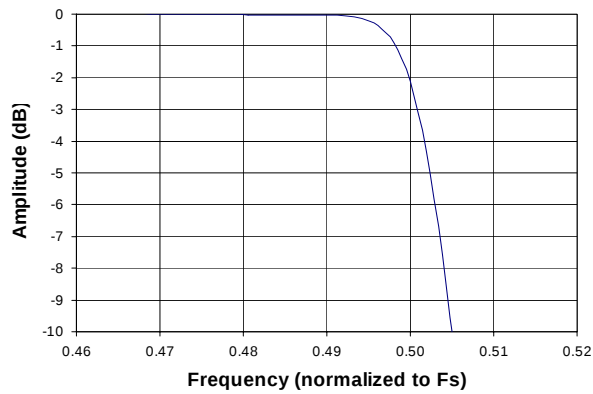


Figure 37. DSM Transition Band (Detail)

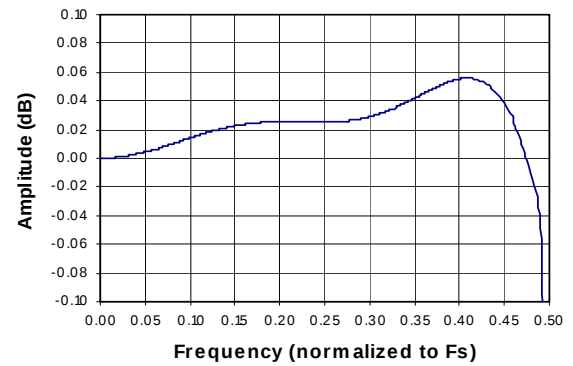


Figure 38. DSM Passband Ripple

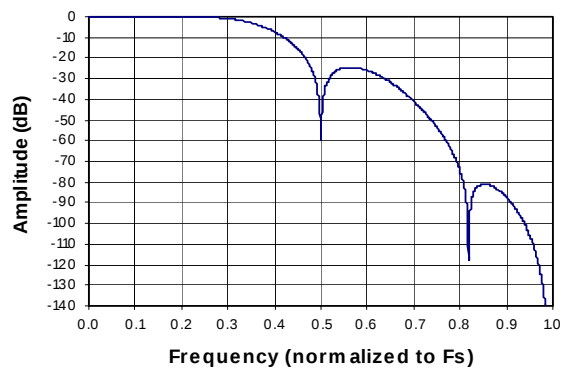


Figure 39. QSM Stopband Rejection

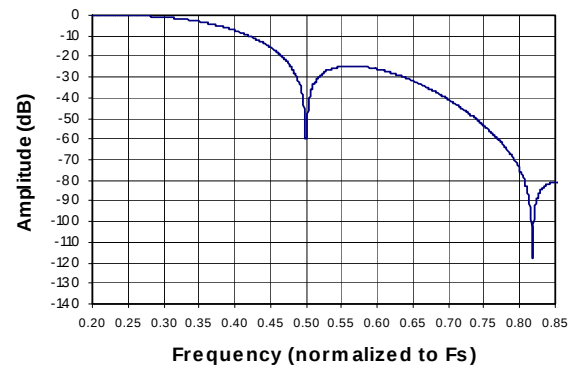


Figure 40. QSM Transition Band

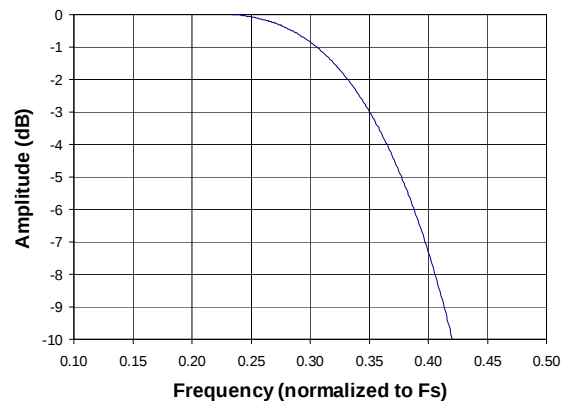


Figure 41. QSM Transition Band (Detail)

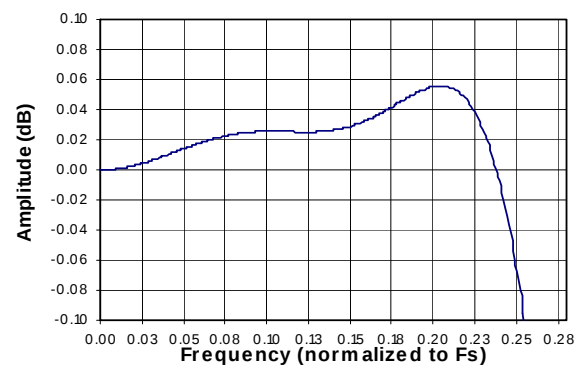


Figure 42. QSM Passband Ripple

9. DAC FILTER PLOTS

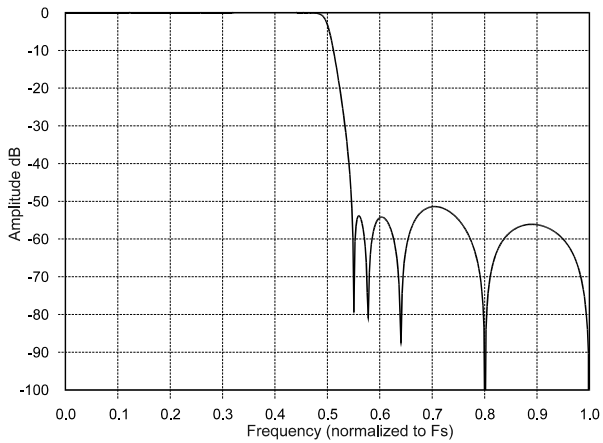


Figure 43. SSM Stopband Rejection

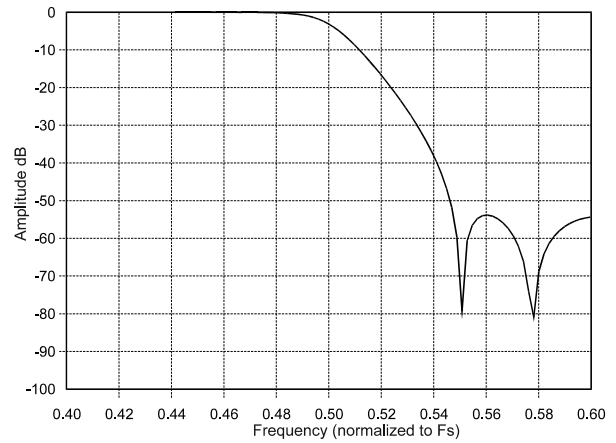


Figure 44. SSM Transition Band

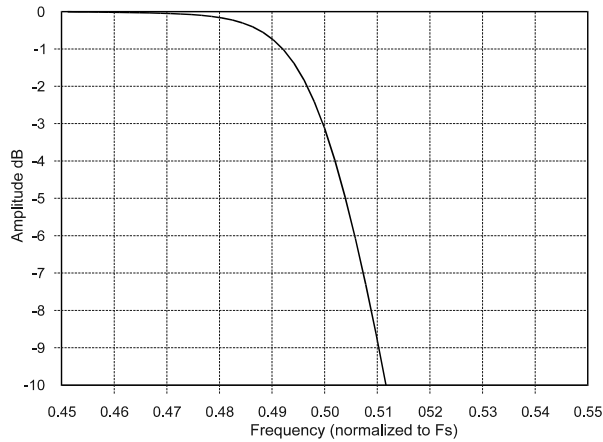


Figure 45. SSM Transition Band (detail)

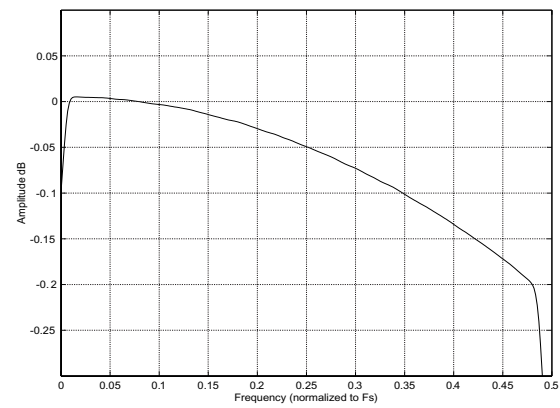


Figure 46. SSM Passband Ripple

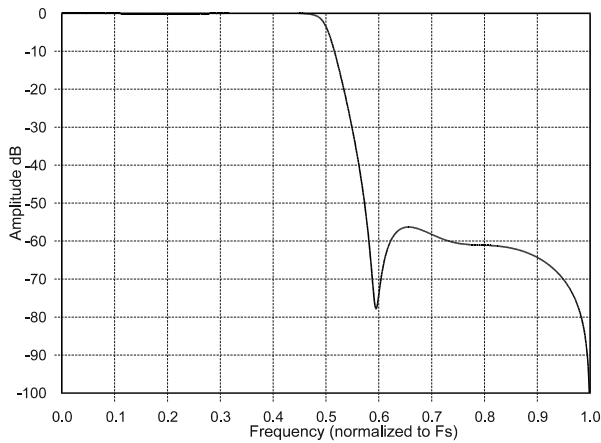


Figure 47. DSM Stopband Rejection

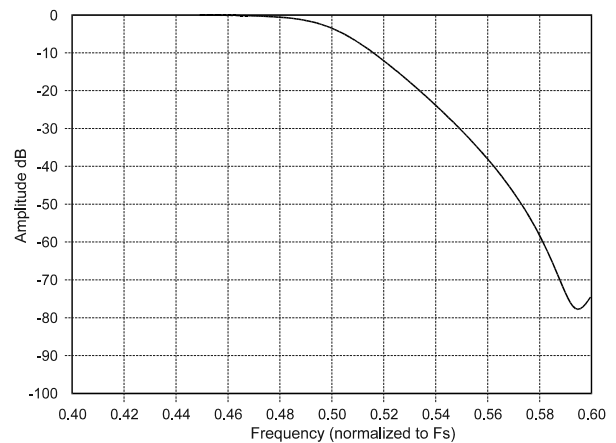


Figure 48. DSM Transition Band

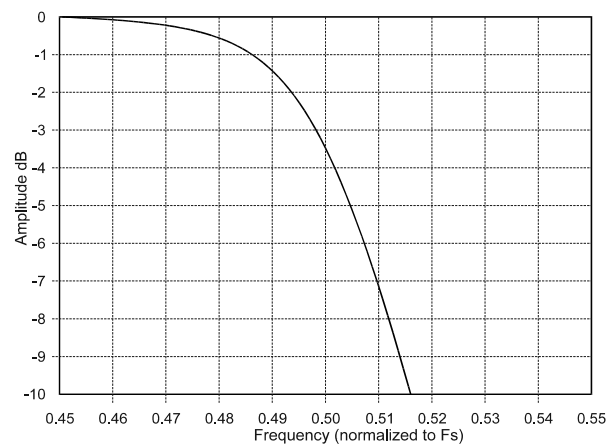


Figure 49. DSM Transition Band (detail)

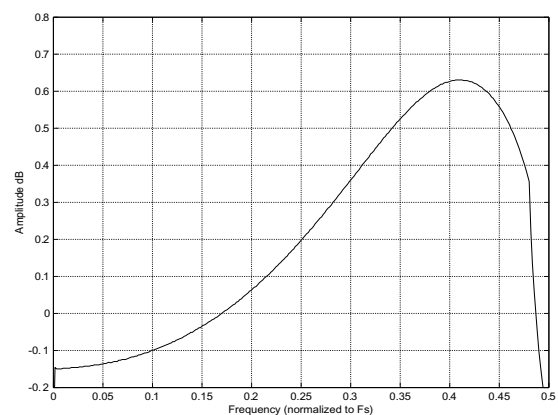


Figure 50. DSM Passband Ripple

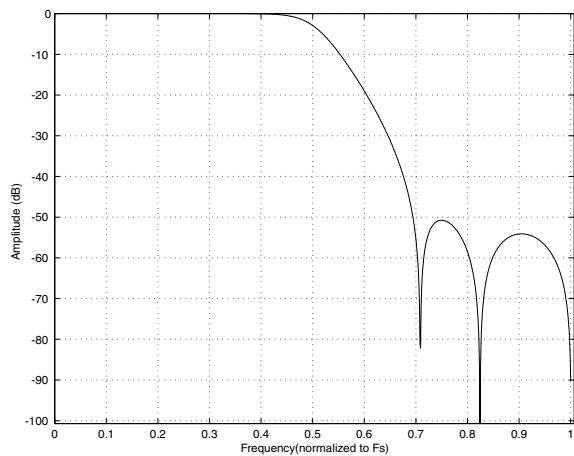


Figure 51. QSM Stopband Rejection

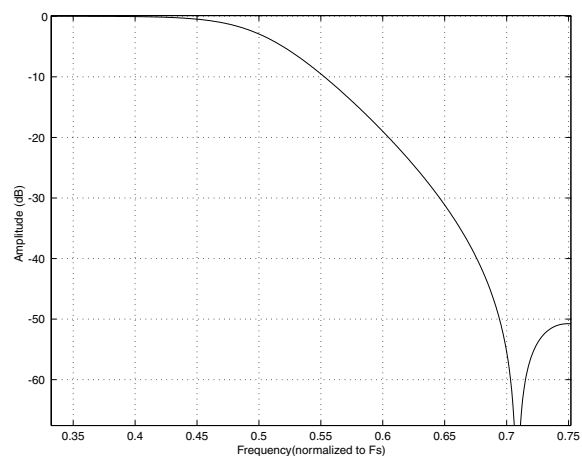


Figure 52. QSM Transition Band

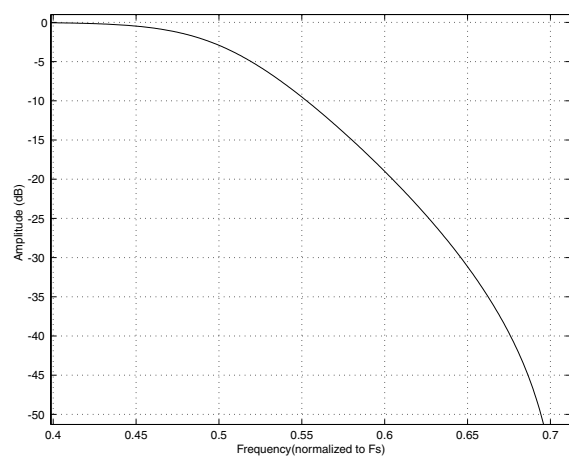


Figure 53. QSM Transition Band (detail)

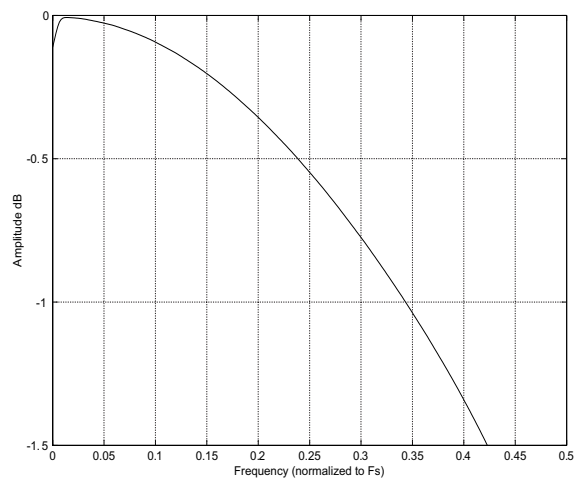


Figure 54. QSM Passband Ripple

10. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channel pairs. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channel pairs. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

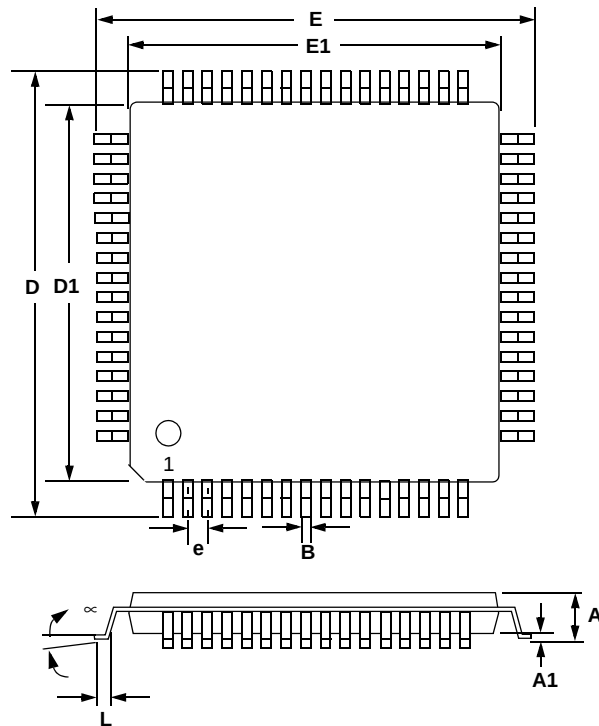
The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

11. REFERENCES

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3. Cirrus Logic, *A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio*, by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.
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6. Cirrus Logic, *How to Achieve Optimum Performance from Delta-Sigma A/D and D/A Converters*, by Steven Harris. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.
7. Cirrus Logic, *A Fifth-Order Delta-Sigma Modulator with 110 dB Audio Dynamic Range*, by I. Fujimori, K. Hamashita and E.J. Swanson. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.
8. Philips Semiconductor, *The I²C-Bus Specification: Version 2.1*, January 2000.
<http://www.semiconductors.philips.com>

12.PACKAGE INFORMATION

64L LQFP PACKAGE DRAWING



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.55	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.008	0.011	0.17	0.20	0.27
D	0.461	0.472 BSC	0.484	11.70	12.0 BSC	12.30
D1	0.390	0.393 BSC	0.398	9.90	10.0 BSC	10.10
E	0.461	0.472 BSC	0.484	11.70	12.0 BSC	12.30
E1	0.390	0.393 BSC	0.398	9.90	10.0 BSC	10.10
e*	0.016	0.020 BSC	0.024	0.40	0.50 BSC	0.60
L	0.018	0.024	0.030	0.45	0.60	0.75
∞	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm
Controlling dimension is mm.
JEDEC Designation: MS026

12.1 Thermal Characteristics

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	2 Layer Board	θ_{JA}	-	50	-	°C/Watt
	4 Layer Board	θ_{JA}	-	37	-	°C/Watt

13.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS42888	4-in, 8-out CODEC for Surround Sound Apps	64L-LQFP	YES	Commercial	-10° to +70° C	Rail	CS42888-CQZ
				Automotive	-40° to +105° C	Tape & Reel	CS42888-CQZR
						Rail	CS42888-DQZ
						Tape & Reel	CS42888-DQZR
CDB42448	CS42888 Evaluation Board	-	-	-	-	-	CDB42448

14.REVISION HISTORY

Revision	Changes
PP1	Initial Release
F1	Updated temperature and voltage specifications in "Recommended Operating Conditions" on page 10. Added test conditions to the Analog Input and Analog Output Characteristics tables.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest you, go to www.cirrus.com.

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