

54F/74F823

9-Bit D-Type Flip-Flop

General Description

The 'F823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems.

The 'F823 is functionally and pin compatible with AMD's Am29823.

Features

- TRI-STATE® outputs
- Clock Enable and Clear
- Direct replacement for AMD's Am29823

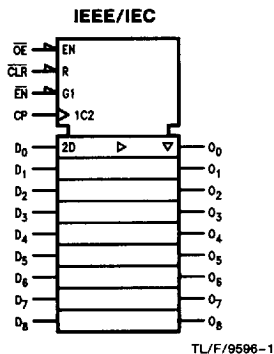
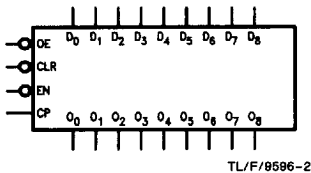
Ordering Code: See Section 11

Commercial	Military	Package Number	Package Description
74F823SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F823SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F823SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F823FM (Note 2)	W24C	24-Lead Cerpack
	54F823LM (Note 2)	E28A	24-Lead Ceramic Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX.

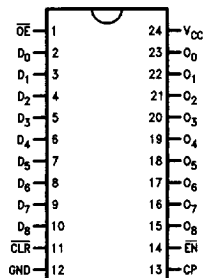
Note 2: Military grade device with environmental and burn-in processing. Use suffix = SDMQB, FMQB and LMQB.

Logic Symbols

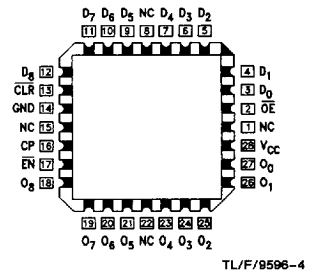


Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0-D_8	Data Inputs	1.0/1.0	20 μA / -0.6 mA
\overline{OE}	Output Enable Input	1.0/1.0	20 μA / -0.6 mA
\overline{CLR}	Clear	1.0/1.0	20 μA / -0.6 mA
CP	Clock Input	1.0/2.0	20 μA / -1.2 mA
\overline{EN}	Clock Enable	1.0/1.0	20 μA / -0.6 mA
O_0-O_8	TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

Functional Description

The 'F823 device consists of nine D-type edge-triggered flip-flops. It has TRISTATE™ Outputs and is organized in broadside pinning. The buffered Clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the \overline{OE} LOW the contents of the flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, the 'F823 has Clear (\overline{CLR}) and Clock Enable (\overline{EN}) pins.

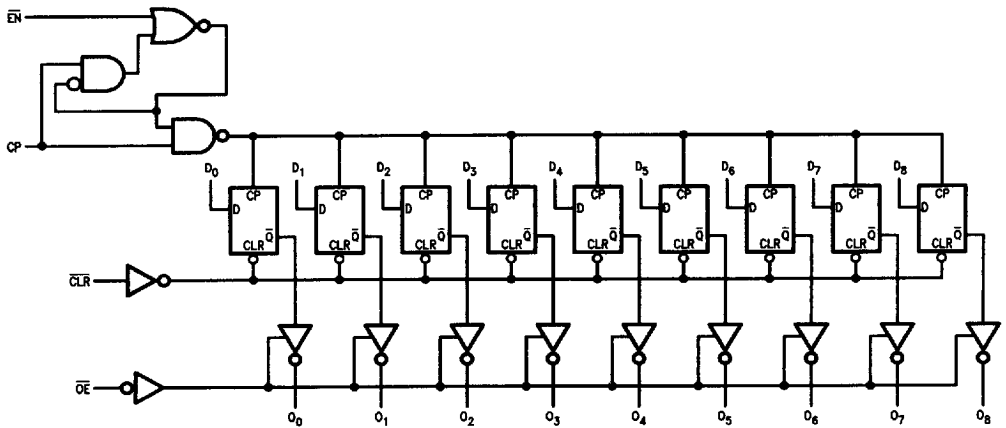
When the \overline{CLR} is LOW and the \overline{OE} is LOW, the outputs are LOW. When \overline{CLR} is HIGH, data can be entered into the flip-flops. When \overline{EN} is LOW, data on the inputs is transferred to the outputs on the LOW to HIGH clock state regardless of the \overline{EN} is HIGH, the outputs do not change state regardless of the data or clock inputs transitions. This device is ideal for parity bus interfacing in high performance systems.

Function Table

Inputs					Internal	Output	Function
\overline{OE}	\overline{CLR}	\overline{EN}	CP	D	\overline{Q}	O	
H	H	L	H	X	NC	Z	Hold
H	H	L	L	X	NC	Z	Hold
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	Clear
H	H	L	↗	H	H	Z	Load
H	H	L	↘	H	L	Z	Load
L	H	L	↗	L	H	L	Data Available
L	H	L	↘	H	L	H	Data Available
L	H	L	H	X	NC	NC	No Change in Data
L	H	L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level
 H = HIGH Voltage Level
 X = Immaterial
 Z = High Impedance
 ↗ = LOW-to-HIGH Transition
 ↘ = HIGH-to-LOW Transition
 NC = No Change

Logic Diagram



TL/F/9596-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions	
		Min	Typ	Max				
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal	
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal	
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA	
		54F 10% V _{CC}	2.4				I _{OH} = -3 mA	
		74F 10% V _{CC}	2.5				I _{OH} = -1 mA	
		74F 10% V _{CC}	2.4				I _{OH} = -3 mA	
		74F 5% V _{CC}	2.7				I _{OH} = -1 mA	
		74F 5% V _{CC}	2.7				I _{OH} = -3 mA	
V _{OL}	Output LOW Voltage	54F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA	
		74F 10% V _{CC}		0.5			I _{OL} = 24 mA	
I _{IH}	Input HIGH Current	54F		20.0	μA	Max	V _{IN} = 2.7V	
		74F		5.0				
I _{BV}	Input HIGH Current Breakdown Test	54F		100	μA	Max	V _{IN} = 7.0V	
		74F		7.0				
I _{CEX}	Output HIGH Leakage Current	54F		250	μA	Max	V _{OUT} = V _{CC}	
		74F		50				
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded	
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded	
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V (OE, CLR, EN) V _{IN} = 0.5V (CP)	
				-1.2				
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V	
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V	
I _{OS}	Output Short-Circuit Current			-60	-150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Buss Drainage Test				500	μA	0.0V	V _{OUT} = 5.25V
I _{CCZ}	Power Supply Current			75	100	mA	Max	V _O = HIGH Z

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AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{\max}	Maximum Clock Frequency	100	160		60		70	MHz	2-1	
t_{PLH}	Propagation Delay CP to O_n	2.0	5.6	9.5	2.0	10.5	2.0	10.5	ns	2-3
t_{PHL}	Propagation Delay CLR to O_n	2.0	5.2	9.5	2.0	10.5	2.0	10.5		
t_{PHL}	Propagation Delay CLR to O_n	4.0	7.1	12.0	4.0	13.0	4.0	13.0	ns	2-3
t_{PZH}	Output Enable Time \overline{OE} to O_n	2.0	5.8	10.5	2.0	13.0	2.0	11.5	ns	2-5
t_{PZL}	Output Enable Time \overline{OE} to O_n	2.0	5.5	10.5	2.0	13.0	2.0	11.5		
t_{PHZ}	Output Disable Time OE to O_n	1.5	2.9	7.0	1.0	7.5	1.5	7.5	ns	2-5
t_{PLZ}	Output Disable Time OE to O_n	1.5	2.7	7.0	1.0	7.5	1.5	7.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(H)$	Setup Time, HIGH or LOW	2.5		4.0		3.0		ns	2-6
$t_s(L)$	D_n to CP	2.5		4.0		3.0			
$t_h(H)$	Hold Time, HIGH or LOW	2.5		2.5		2.5		ns	2-6
$t_h(L)$	D_n to CP	2.5		2.5		2.5			
$t_s(H)$	Setup Time, HIGH or LOW	4.5		5.0		5.0		ns	2-6
$t_s(L)$	\overline{EN} to CP	2.5		3.0		3.0			
$t_h(H)$	Hold Time, HIGH or LOW	2.0		3.0		2.0		ns	2-6
$t_h(L)$	\overline{EN} to CP	0		1.0		0			
$t_w(H)$	CP Pulse Width	5.0		6.0		6.0		ns	2-4
$t_w(L)$	HIGH or LOW	5.0		6.0		6.0			
$t_w(L)$	\overline{CLR} Pulse Width, LOW	5.0		5.0		5.0		ns	2-4
t_{rec}	\overline{CLR} Recovery Time	5.0		5.0		5.0		ns	2-6