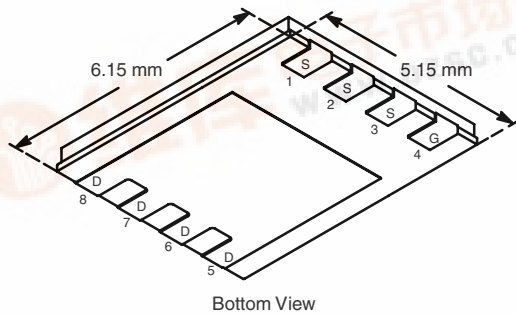


P-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
- 100	0.041 at V _{GS} = - 10 V	- 28	54 nC
	0.047 at V _{GS} = - 4.5 V	- 28	

PowerPAK SO-8



Bottom View

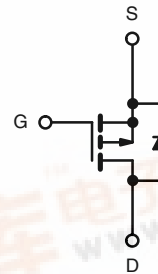
Ordering Information: Si7489DP-T1-E3 (Lead (Pb)-free)
 Si7489DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET



RoHS
 COMPLIANT
HALOGEN
FREE
 Available



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 28 ^a
		T _C = 70 °C	- 24.9 ^a
		T _A = 25 °C	- 7.8 ^{b, c}
		T _A = 70 °C	- 6.2 ^{b, c}
Pulsed Drain Current	I _{DM}	- 40	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	- 28 ^a
		T _A = 25 °C	- 4.3 ^{b, c}
Avalanche Current	I _{AS}	- 35	
Single-Pulse Avalanche Energy	E _{AS}	61	mJ
Maximum Power Dissipation	P _D	T _C = 25 °C	83
		T _C = 70 °C	53
		T _A = 25 °C	5.2 ^{b, c}
		T _A = 70 °C	3.3 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	19	24	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.2	1.5	

Notes:

- Package Limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 65 °C/W.



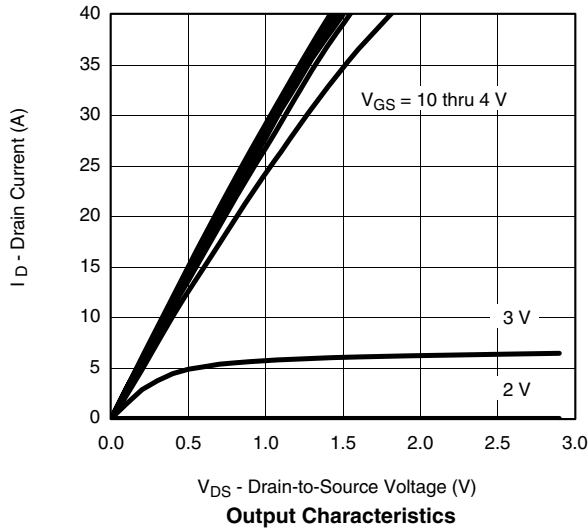
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 113		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1		- 3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = -10\text{ V}$	- 40			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -7.8\text{ A}$		0.033	0.041	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -7.3\text{ A}$		0.038	0.047	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -7.8\text{ A}$		38		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		4600		pF
Output Capacitance	C_{oss}			230		
Reverse Transfer Capacitance	C_{rss}			175		
Total Gate Charge	Q_g	$V_{DS} = -50\text{ V}, V_{GS} = -10\text{ V}, I_D = -7.8\text{ A}$		106	160	nC
				54	81	
Gate-Source Charge	Q_{gs}	$V_{DS} = -50\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -7.8\text{ A}$		14		nC
Gate-Drain Charge	Q_{gd}			26		
Gate Resistance	R_g		$f = 1\text{ MHz}$		4	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 8.1\text{ }\Omega$ $I_D \cong -6.2\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			110	165	
Fall Time	t_f			100	150	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 8.1\text{ }\Omega$ $I_D \cong -6.2\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		42	65	
Rise Time	t_r			160	240	
Turn-Off Delay Time	$t_{d(off)}$			100	150	
Fall Time	t_f			100	150	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			- 28	A
Pulse Diode Forward Current ^a	I_{SM}				- 40	
Body Diode Voltage	V_{SD}	$I_S = -6.2\text{ A}$		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -6.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		60	90	ns
Body Diode Reverse Recovery Charge	Q_{rr}			150	225	nC
Reverse Recovery Fall Time	t_a			46		ns
Reverse Recovery Rise Time	t_b			14		

Notes:

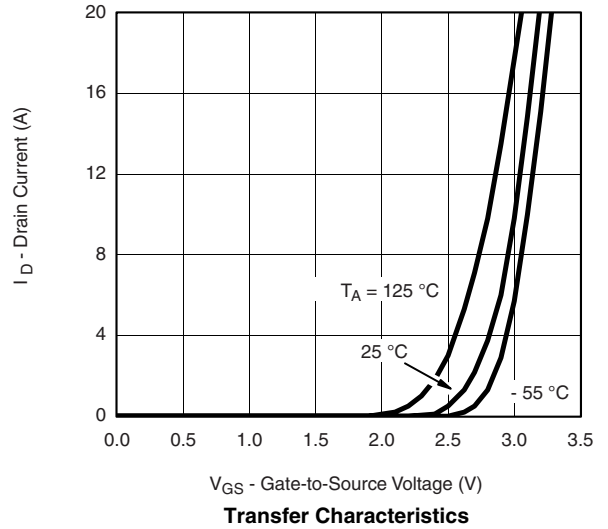
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

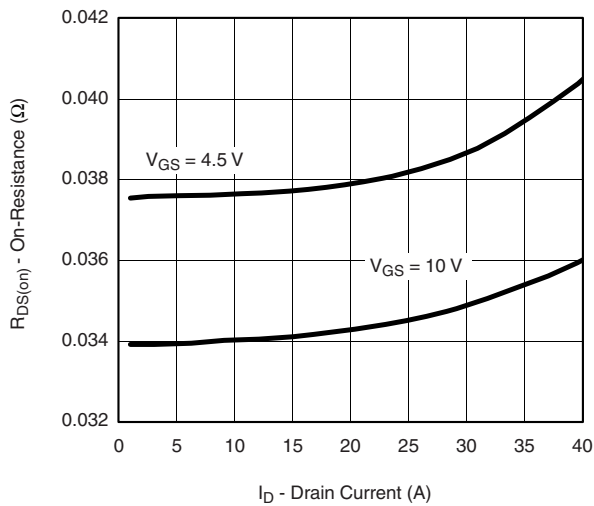
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



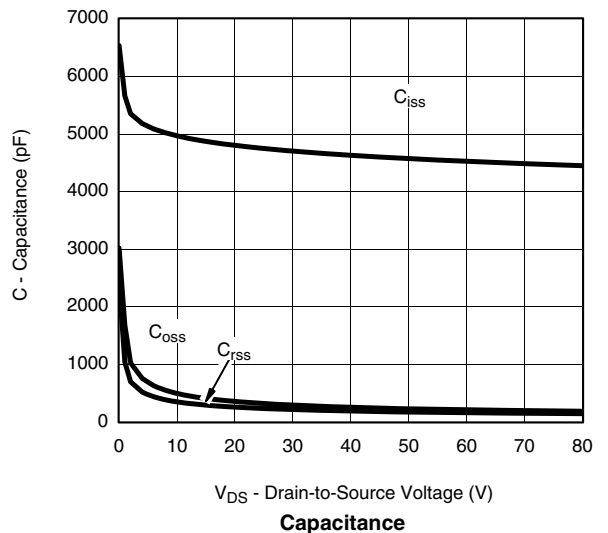
Output Characteristics



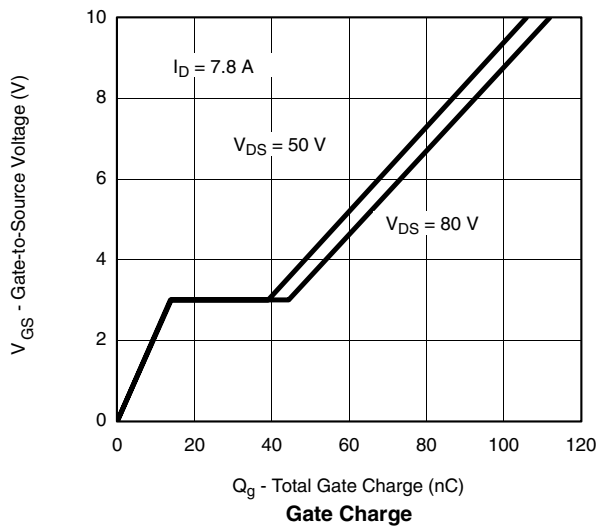
Transfer Characteristics



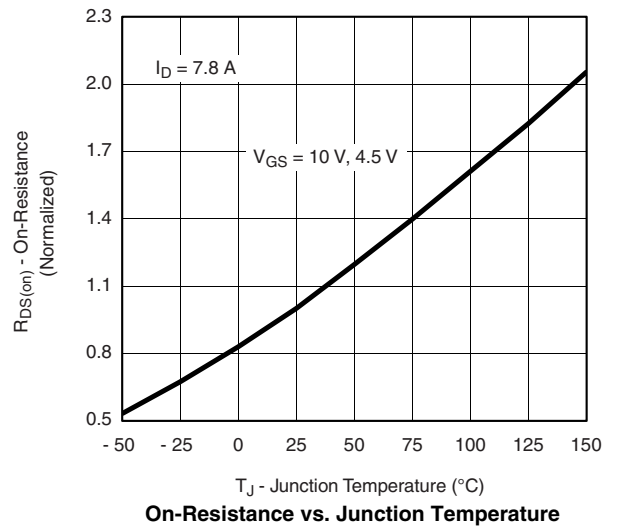
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

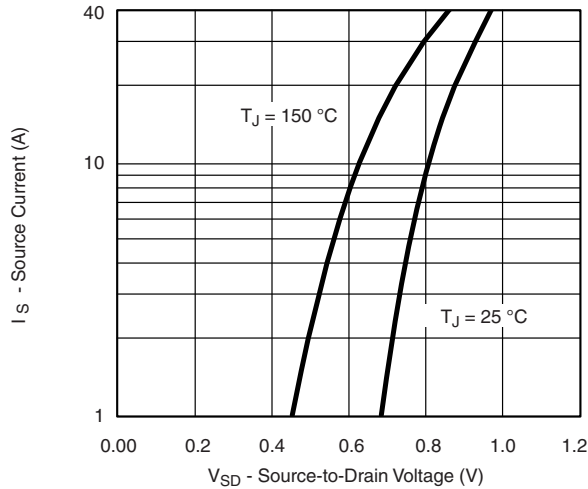


Gate Charge

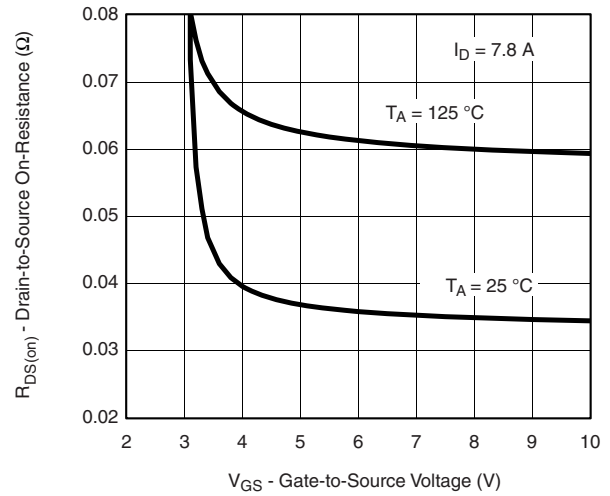


On-Resistance vs. Junction Temperature

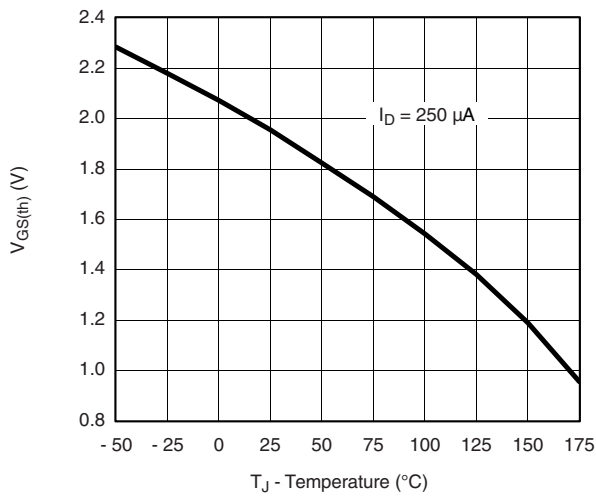
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



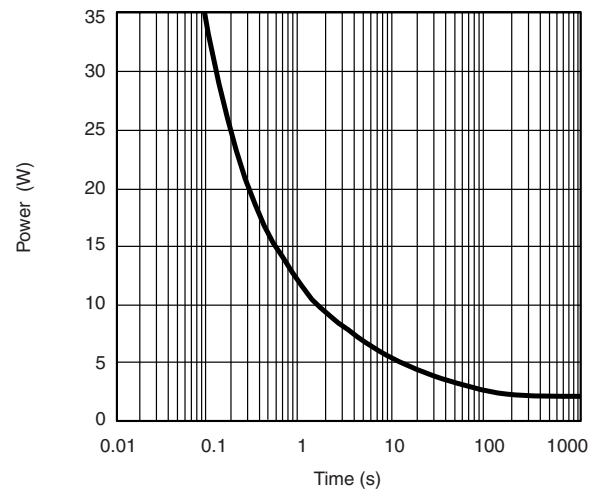
Source-Drain Diode Forward Voltage



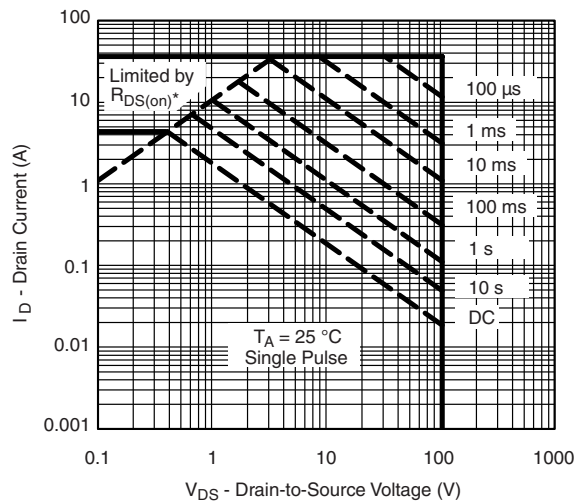
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



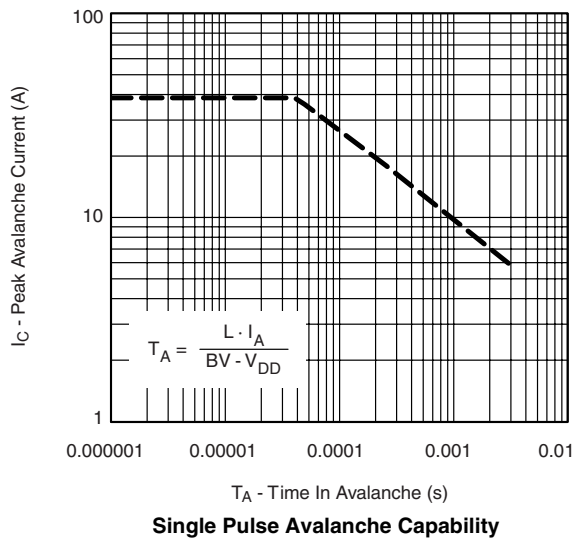
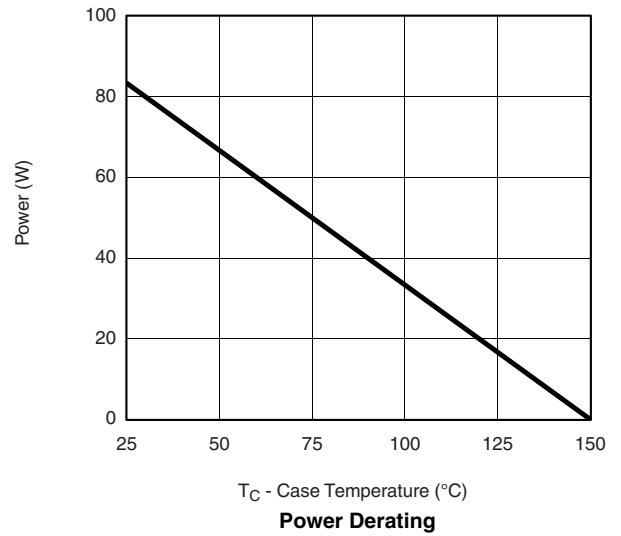
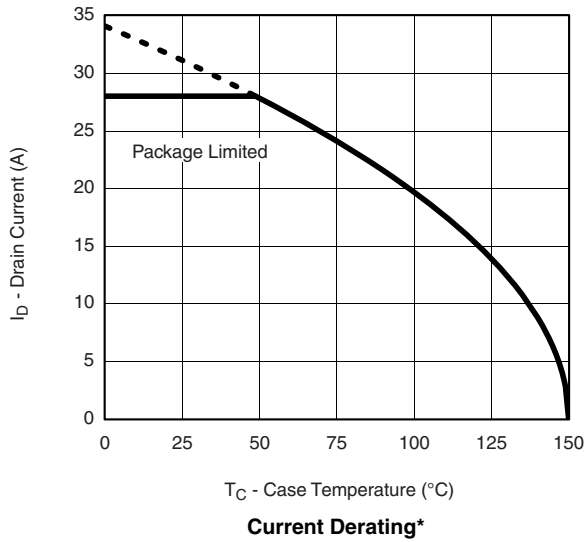
Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

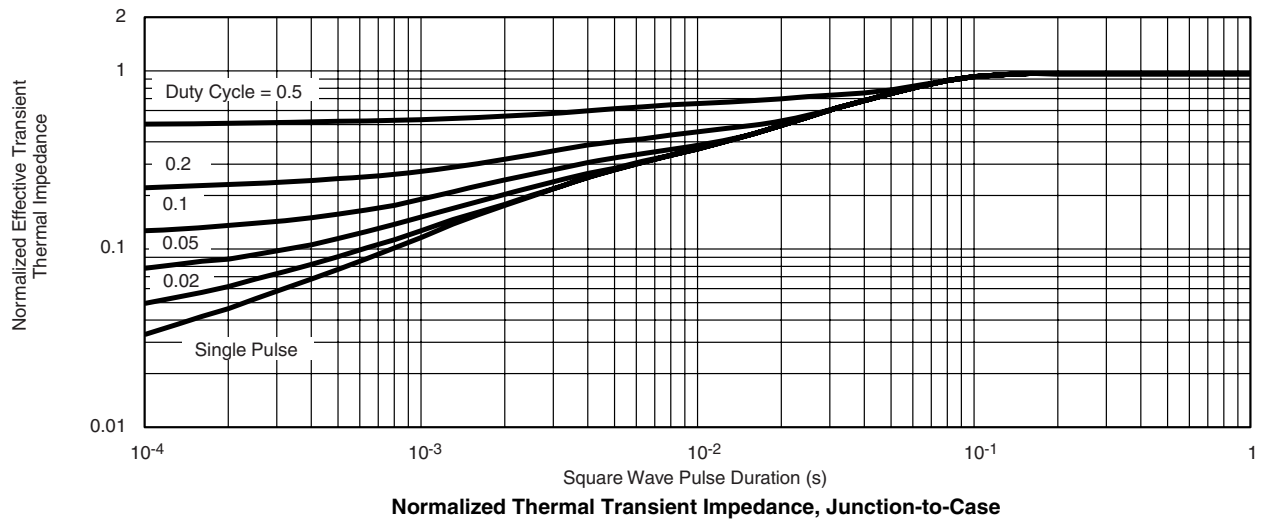
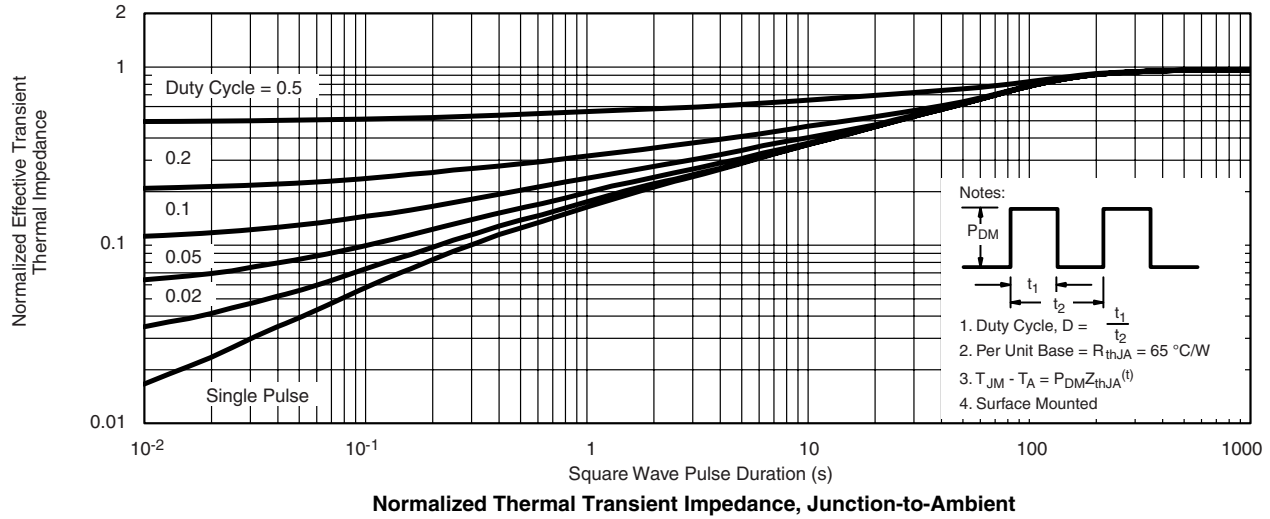
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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