FAIRCHILD SEMICONDUCTOR™

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# MM74HCU04
# Hex Inverter

## General Description

The MM74HCU04 inverters utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

The MM74HCU04 is an unbuffered inverter. It has high noise immunity and the ability to drive 15 LS-TTL loads. The 74HCU logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $V_{CC}$ and ground.

## Features

- Typical propagation delay: 7 ns
- Fanout of 15 LS-TTL loads
- Quiescent power consumption: 10 μA maximum at room temperature
- Low input current: 1 μA maximum

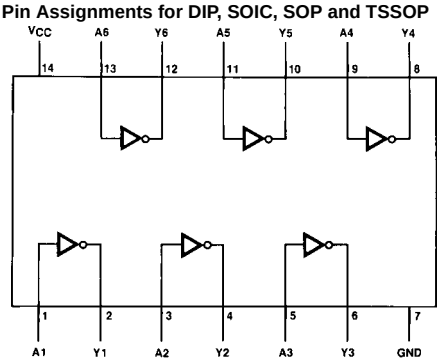
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| MM74HCU04M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow |
| MM74HCU04SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HCU04MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HCU04N | N14A | 14-Lead Plastic Dual-In-Lead Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

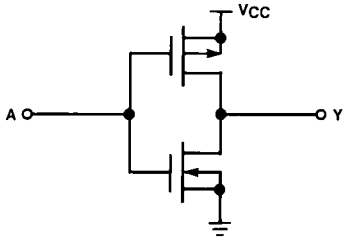
## Connection Diagram

**Pin Assignments for DIP, SOIC, SOP and TSSOP**




**Top View**

## Schematic Diagram



## Absolute Maximum Ratings(Note 1)

(Note 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5 to +7.0V |
| DC Input Voltage ($V_{IN}$) | −1.5 to $V_{CC}$ +1.5V |
| DC Output Voltage ($V_{OUT}$) | −0.5 to $V_{CC}$ +0.5V |
| Clamp Diode Current ($I_{IK}$, $I_{OK}$) | ±20 mA |
| DC Output Current, per pin ($I_{OUT}$) | ±25 mA |
| DC $V_{CC}$ or GND Current, per pin ($I_{CC}$) | ±50 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature ($T_L$) | |
| (Soldering 10 seconds) | 260°C |

## Recommended Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 2 | 6 | V |
| DC Input or Output Voltage ($V_{IN}$, $V_{OUT}$) | 0 | $V_{CC}$ | V |
| Operating Temperature Range ($T_A$) | −40 | +85 | °C |

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$ = 25°C | $T_A$ = −40 to 85°C | $T_A$ = −55 to 125°C | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | | 2.0V | | 1.7 | 1.7 | 1.7 | V |
| | | | 4.5V | | 3.6 | 3.6 | 3.6 | V |
| | | | 6.0V | | 4.8 | 4.8 | 4.8 | V |
| $V_{IL}$ | Maximum LOW Level Input Voltage | | 2.0V | | 0.3 | 0.3 | 0.3 | V |
| | | | 4.5V | | 0.8 | 0.8 | 0.8 | V |
| | | | 6.0V | | 1.1 | 1.1 | 1.1 | V |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | $V_{IN}$ = $V_{IL}$ | | | | | | |
| | | $\|I_{OUT}\| \leq 20$ µA | 2.0V | 2.0 | 1.8 | 1.8 | 1.8 | V |
| | | | 4.5V | 4.5 | 4.0 | 4.0 | 4.0 | V |
| | | | 6.0V | 6.0 | 5.5 | 5.5 | 5.5 | V |
| | | $V_{IN}$ = GND | | | | | | |
| | | $\|I_{OUT}\| \leq 4.0$ mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | $\|I_{OUT}\| \leq 5.2$ mA | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | V |
| $V_{OL}$ | Maximum LOW Level Output Voltage | $V_{IN}$ = $V_{IH}$ | | | | | | |
| | | $\|I_{OUT}\| \leq 20$ µA | 2.0V | 0 | 0.2 | 0.2 | 0.2 | V |
| | | | 4.5V | 0 | 0.5 | 0.5 | 0.5 | V |
| | | | 6.0V | 0 | 0.5 | 0.5 | 0.5 | V |
| | | $V_{IN}$ = $V_{CC}$ | | | | | | |
| | | $\|I_{OUT}\| \leq 6.0$ mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | $\|I_{OUT}\| \leq 7.8$ mA | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| $I_{IN}$ | Maximum Input Current | $V_{IN}$ = $V_{CC}$ or GND | 6.0V | | ±0.1 | ±1.0 | ±1.0 | µA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND | 6.0V | | 2.0 | 20 | 40 | µA |
| | | $I_{OUT}$ = 0 µA | | | | | | |

**Note 4:** For a power supply of 5V ±10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5V and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

## AC Electrical Characteristics

$V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 15 pF, $t_r$ = $t_f$ = 6 ns

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | | 7 | 13 | ns |

## AC Electrical Characteristics

$V_{CC}$ = 2.0V to 6.0V, $C_L$ = 50 pF, $t_r$ = $t_f$ = 6 ns (unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$=25°C | $T_A$=−40 to 85°C | $T_A$=−55 to 125°C | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | | |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | | 2.0V | 49 | 82 | 103 | 120 | ns |
| | | | 4.5V | 9.9 | 16 | 21 | 24 | ns |
| | | | 6.0V | 8.4 | 14 | 18 | 20 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Rise and Fall Time | | 2.0V | 30 | 75 | 95 | 110 | ns |
| | | | 4.5V | 8 | 15 | 19 | 22 | ns |
| | | | 6.0V | 7 | 13 | 16 | 19 | ns |
| $C_{PD}$ | Power Dissipation Capacitance (Note 5) | (per gate) | | 90 | | | | pF |
| $C_{IN}$ | Maximum Input Capacitance | | | 8 | 15 | 15 | 15 | pF |

**Note 5:** $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

## Typical Applications

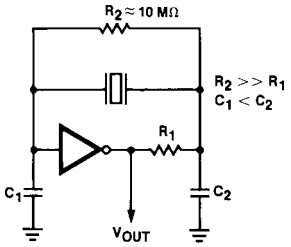



FIGURE 1. Crystal Oscillator

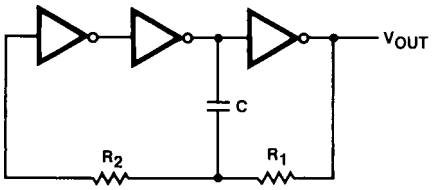



FIGURE 2. Stable RC Oscillator

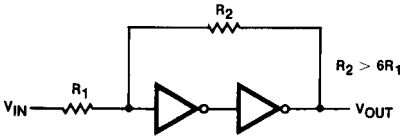
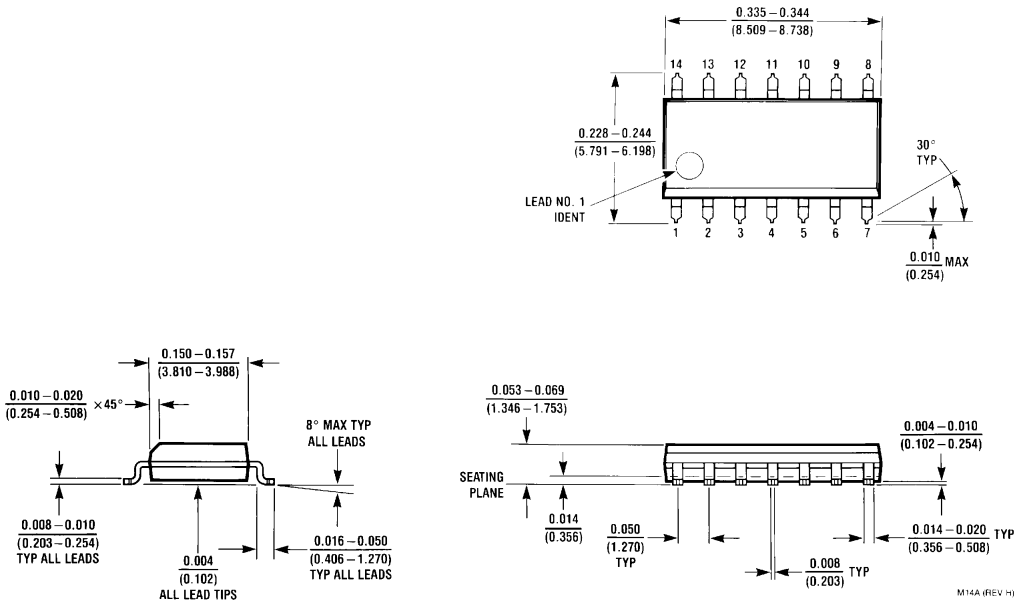
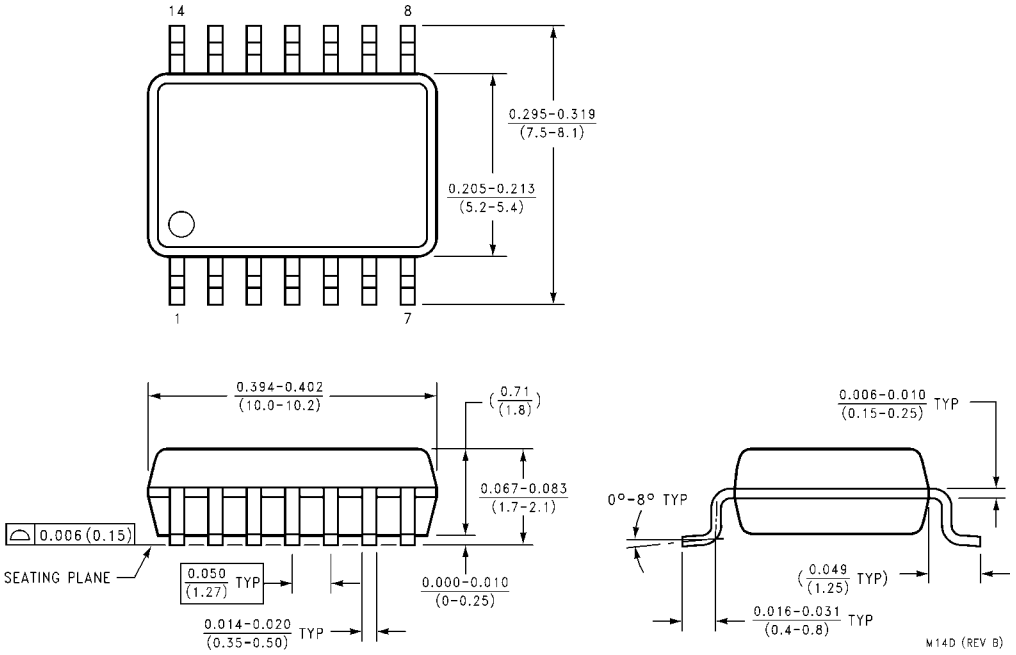



FIGURE 3. Schmitt Trigger

## Physical Dimensions inches (millimeters) unless otherwise noted



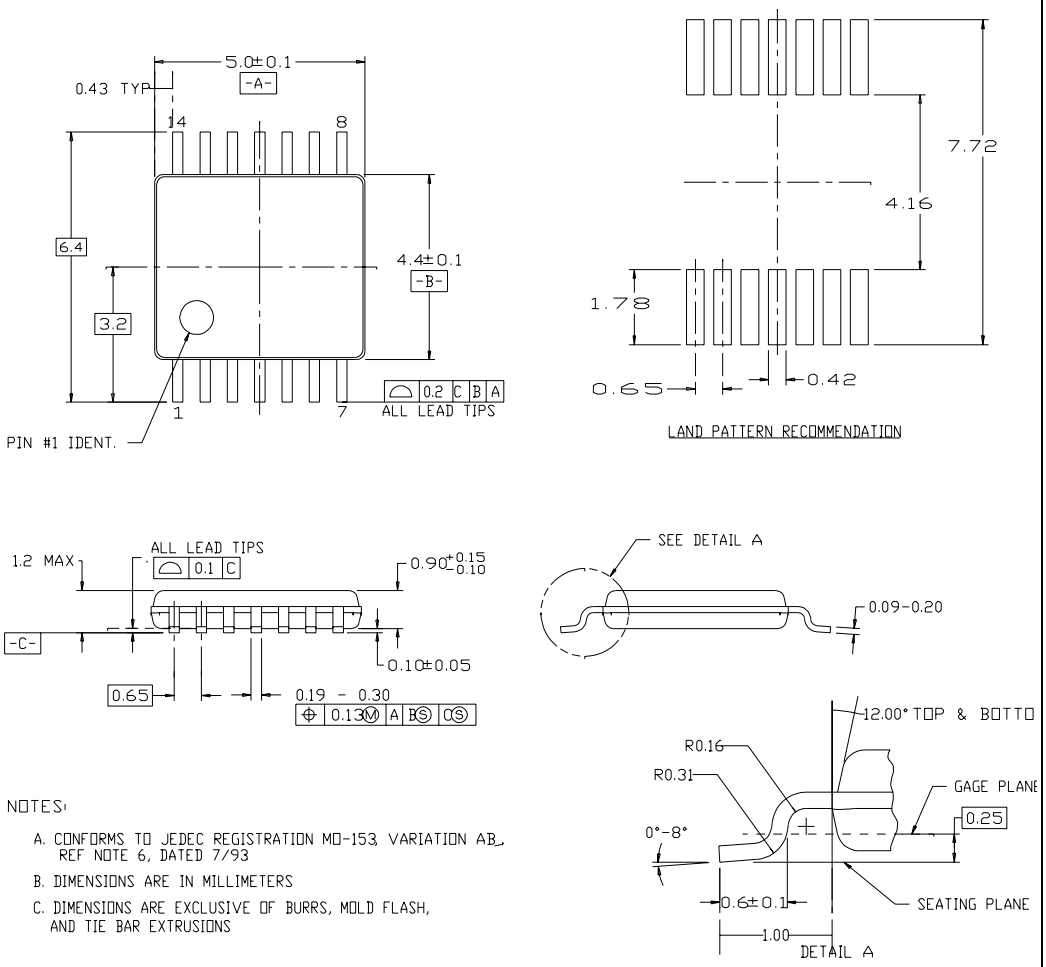

**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow**
**Package Number M14A**




**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M14D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

14LD, TSSOP, JEDEC MO-153, 4.4MM WIDE




NOTES:

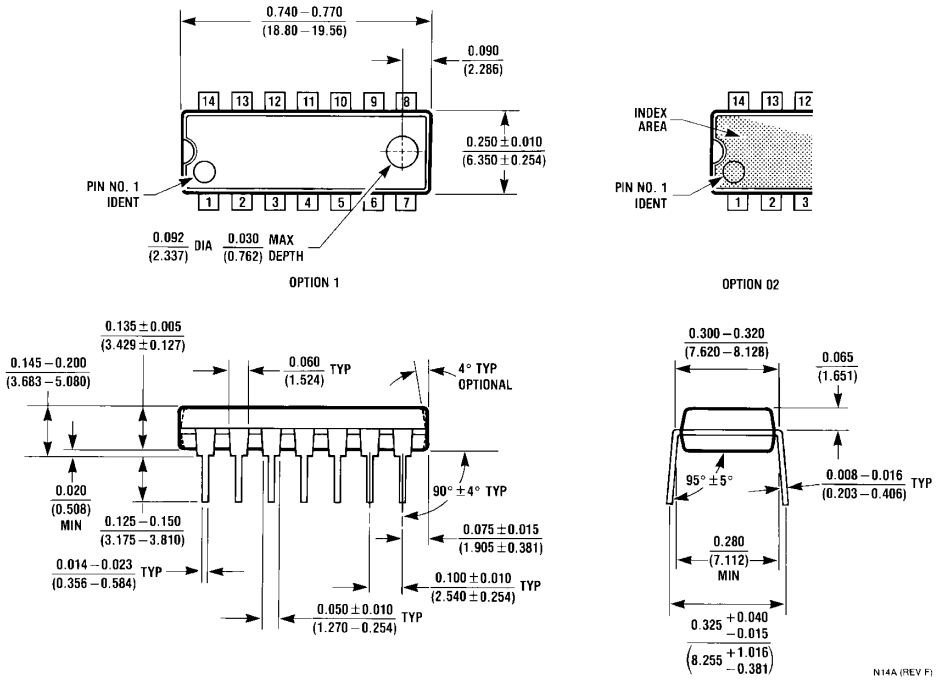
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC14**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N14A**