Rev 0; 10/08

MAXIM

XFP Laser Control and Digital Diagnostic IC

DS1862A

General Description

The DS1862A is a closed-loop laser-driver control IC with built-in digital diagnostics designed for XFP MSA. The laser control function incorporates automatic power control (APC) and allows extinction ratio control though a temperature-indexed lookup table (LUT). The DS1862A monitors up to seven analog inputs, including temperature and monitor diode (MD) current, which are used to regulate the laser bias current and extinction ratio. Warning and alarm thresholds can be programmed to generate an interrupt if monitored signals exceed tolerance. Calibration is also provided internally using independent gain and offset scaling registers for each of the monitored analog signals. Settings such as programmed calibration data are stored in password-protected EEPROM memory. Programming is accomplished through an I²C-compatible interface, which can also be used to access diagnostic functionality.

Applications

Laser Control and Monitoring 10Gbps Optical Transceiver Modules (XFP)

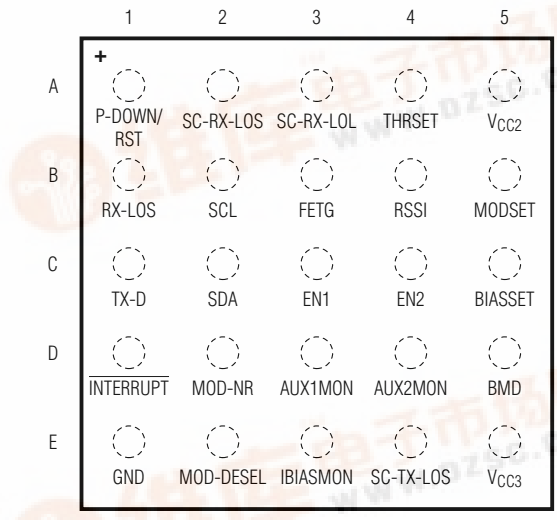
Laser Control and Monitoring

Digital Diagnostics in Optical Transmission

Features

- **Implements XFP MSA Requirements for Digital Diagnostics, Serial ID, and User Memory**
- **I²C-Compatible Serial Interface**
- **Automatic Power Control (APC)**
- **Extinction Ratio Control with Lookup Table**
- **Seven Monitored Channels for Digital Diagnostics (Five Basic Plus Two Auxiliary)**
- **Internal Calibration of Monitored Channels (Temp, $V_{CC2/3}$, Bias Current, Transmitted, and Received Power)**
- **Programmable Quick-Trip Logic for Turning Off Laser for Eye Safety**
- **Access to Monitoring and ID Information**
- **Programmable Alarm and Warning Thresholds**
- **Operates from 3.3V or 5V Supply**
- **25-Ball CSBGA, 5mm x 5mm Package**
- **Internal or External Temperature Sensor**
- **-40°C to +100°C Operating Temperature Range**
- **One 8-Bit Buffered DAC**

Pin Configuration



CSBGA (5mm x 5mm)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1862AB+	-40°C to +100°C	25 CSBGA
DS1862AB+T&R	-40°C to +100°C	25 CSBGA

+Denotes a lead-free/RoHS-compliant package.
T&R = Tape and reel.

Typical Operating Circuit appears at end of data sheet.

XFP Laser Control and Digital Diagnostic IC

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Open-Drain Pin Relative to Ground.....-0.5V to +6.0V
Voltage Range on MOD-DESEL, SDA, SCL, FETG, THRSET, TX-D, AUX1MON, AUX2MON, IBIASMON, RSSI, BIASSET, MODSET, EN1, EN2.....-0.5V to (V_{CC3} + 0.5V)*
Voltage Range on SC-RX-LOS, SC-RX-LOL, RX-LOS, SC-TX-LOS, MOD-NR, EN1, EN2.....-0.5V to (V_{CC2} + 0.5V)*
Operating Temperature Range .....-40°C to +100°C
EEPROM Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC JEDEC J-STD-020 Specification.

**Not to exceed +6.0V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(V_{CC3} = +2.9V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC3}	(Note 1)	+2.9		+5.5	V
Secondary Supply Voltage	V_{CC2}	V_{CC2} not to exceed V_{CC3} (Note 2)	+1.6		+3.6	V
High-Level Input Voltage (SDA, SCL)	V_{IH}	I_{IH} (max) = 10µA	0.7 x V_{CC3}		V_{CC3} + 0.5	V
Low-Level Input Voltage (SDA, SCL)	V_{IL}	I_{IL} (max) = -10µA	GND - 0.3		0.3 x V_{CC3}	V
High-Level Input Voltage (TX-D, MOD-DESEL, P-DOWN/RST) (Note 3)	V_{IH}	I_{IH} (max) = 10µA	2		V_{CC3} + 0.3	V
Low-Level Input Voltage (TX-D, MOD-DESEL, P-DOWN/RST) (Note 3)	V_{IL}	I_{IL} (max) = -10µA	-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC3} = +2.9V to +5.5V, V_{CC2} = +1.6V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC3}	P-DOWN/RST = 1		3	5	mA
High-Level Output Voltage (FETG)	V_{OH}	I_{OH} (max) = -2mA	V_{CC3} - 0.5			V
Low-Level Output Voltage (MOD-NR, $\overline{INTERRUPT}$, SDA, FETG)	V_{OL}	I_{OL} (max) = 3mA	0		0.4	V
Resistor (Pullup)	R_{PU}		9	12	15	kΩ
I/O Capacitance	$C_{I/O}$	(Note 4)			10	pF
Leakage Current	I_L		-10		+10	µA
Leakage Current (SCL, SDA)	I_L		-10		+10	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.0		2.6	V

DC ELECTRICAL CHARACTERISTICS—INTERFACE SIGNALS TO SIGNAL CONDITIONERS

(V_{CC2} = +1.6V to +3.6V, V_{CC3} = +2.9V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Level Input Voltage (SC-RX-LOS, SC-RX-LOL, SC-TX-LOS)	V_{IH}	I_{IH} (max) = 100µA	0.7 x V_{CC2}		V_{CC2} + 0.1	V
Low-Level Input Voltage (SC-RX-LOS, SC-RX-LOL, SC-TX-LOS)	V_{IL}	I_{IL} (max) = -100µA	0		0.3 x V_{CC2}	V
High-Level Output Voltage (EN1, EN2)	V_{OH}	I_{OH} (max) = -0.7mA	V_{CC2} - 0.2			V
	V_{OH2}	V_{CC2} = 2.5V to 3.6V, I_{OH} (max) = -2mA	V_{CC2} - 0.4			
	V_{OH3}	V_{CC2} = 1.6V, I_{OH} (max) = -0.7mA	V_{CC2} - 0.2			
Low-Level Output Voltage (EN1, EN2, RX-LOS)	V_{OL}	I_{OL} (max) = 0.7mA			0.20	V
	V_{OL2}	V_{CC2} = 2.5V to 3.6V, I_{OL} (max) = 2mA			0.40	
Leakage Current (SC-RX-LOS, SC-RX-LOL, SC-TX-LOS, RX-LOS)	I_L		-10		+10	µA

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I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC3} = +2.9V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:SDA}$		0.6			µs
START Setup Time	$t_{SU:SDA}$		0.6			µs
Data In Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data In Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 5)	20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 5)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
MOD-DESEL Setup Time	$t_{HOST\_SELECT\_SETUP}$		2			ms
MOD-DESEL Hold Time	$t_{HOST\_SELECT\_HOLD}$		10			µs
Aborted Sequence Bus Release	$t_{MOD-DESEL\_ABORT}$				2	ms
Capacitive Load for Each Bus	C_B	(Note 5)			400	pF
EEPROM Write Time	t_W	≤ 4-byte write (Note 6)			16	ms

ANALOG OUTPUT CHARACTERISTICS

(V_{CC3} = +2.9V to +5.5V, V_{CC2} = +1.6V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{BIASSET}$	$I_{BIASSET}$		0.01		1.50	mA
$I_{BIASSET}$ (Off-State Current)	$I_{BIASSET}$	Shutdown		±10	±100	nA
I_{MODSET}	I_{MODSET}		0.01		1.20	mA
I_{MODSET} (Off-State Current)	I_{MODSET}	Shutdown		±10	±100	nA
Voltage on $I_{BIASSET}$ and I_{MODSET}	V_{MAX}	(Note 7)	0.7		3.0	V
V_{THRSET}	V_{THRSET}	I_{MAX} = 100µA	50		1000	mV
V_{THRSET} Drift		Across temperature (Note 8)	-5		+5	%
V_{THRSET} Capacitance Load	C_{THRSET}				1	nF
APC Calibration Accuracy		+25°C			25	µA
APC Temp Drift		0.200mA to 1.5mA	-5		+5	%
		50µA to 200µA			12	µA
I_{BMD} DNL		Sink, SRC_SINK_B = 0	-0.9		+0.9	LSB
		Source, SRC_SINK_B = 1	-0.9		+0.9	
I_{BMD} INL		Sink, SRC_SINK_B = 0	-4.0		+4.0	LSB
		Source, SRC_SINK_B = 1	-4.0		+4.0	
I_{BMD} Voltage Drift					1.2	%/V
I_{BMD} FS Accuracy					1.5	%

ANALOG OUTPUT CHARACTERISTICS (continued)

(V_{CC3} = +2.9V to +5.5V, V_{CC2} = +1.6V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I_{MODSET} Accuracy		+25°C, I_{MODSET} = 0.04mA to 1.2mA	-1.5		+1.5	%
I_{MODSET} DNL		75µA range	-0.9		+0.9	LSB
		150µA range	-0.9		+0.9	
		300µA range	-0.9		+0.9	
		600µA range	-0.9		+0.9	
		1200µA range	-0.9		+0.9	
I_{MODSET} INL		75µA range	-1.5		+1.5	LSB
		150µA range	-1.5		+1.5	
		300µA range	-1.0		+1.0	
		600µA range	-1.0		+1.0	
		1200µA range	-1.0		+1.0	
I_{MODSET} Temp Drift					5	%
I_{MODSET} Voltage Drift					1.2	%/V
I_{MODSET} FS Accuracy					1.5	%
APC Bandwidth		I_{MD} / I_{APC} = 1 (Note 4)	6	10	30	kHz

AC ELECTRICAL CHARACTERISTICS—XFP CONTROLLER

(V_{CC3} = +2.9V to +5.5V, V_{CC2} = +1.6V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time to Initialize	t_{INIT}	V_{CC3} within ±5% of nominal	30		200	ms
TX-D Assert Time	t_{OFF}	I_{BIAS} and I_{MOD} below 10% of nominal			5	µs
TX-D Deassert Time	t_{ON}	I_{BIAS} and I_{MOD} above 90% of nominal			1	ms
P-DOWN/RST Assert Time	t_{PDR-ON}	I_{BIAS} and I_{MOD} below 10% of nominal			100	µs
P-DOWN/RST Deassert Time	$t_{PDR-OFF}$	I_{BIAS} and I_{MOD} above 90% of nominal			200	ms
MOD-DESEL Deassert Time	$t_{MOD-DESEL}$	Time until proper response to I^2C communication			2	ms
$\overline{INTERRUPT}$ Assert Delay	t_{INIT_ON}	Time from fault to interrupt assertion			100	ms
$\overline{INTERRUPT}$ Deassert Delay	t_{INIT_OFF}	Time from read (clear flags) to interrupt deassertion			500	µs
MOD-NR Assert Delay	$t_{MOD-NR-ON}$	Time from fault to MOD-NR assertion			0.5	ms
MOD-NR Deassert Delay	$t_{MOD-NR-OFF}$	Time from read (clear flags) to MOD-NR deassertion			0.5	ms
RX-LOS Assert Time	t_{LOS-ON}	Time from SC-RX-LOS assertion to RX-LOS assertion			100	ns
RX-LOS Deassert Time	$t_{LOS-OFF}$	Time from SC-RX-LOS deassertion to RX-LOS deassertion			100	ns
P-DOWN/RST Reset Time	t_{RESET}	Time from P-DOWN/RST assertion to initial reset	10			µs
Shutdown Time	t_{FAULT}	Time from fault to $I_{BIASSET}$, I_{MODSET}, and I_{BMD} below 10%			30	µs

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AC ELECTRICAL CHARACTERISTICS—SOFT* CONTROL AND STATUS

(V_{CC3} = +2.9V to +5.5V, V_{CC2} = +1.6V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT TX-D Assert Time	t_{OFF_SOFT}	I_{BIAS} and I_{MOD} below 10% of nominal			50	ms
SOFT TX-D Deassert Time	t_{ON_SOFT}	I_{BIAS} and I_{MOD} above 90% of nominal			50	ms
SOFT P-DOWN/RST Assert Time	t_{PDR-ON_SOFT}	I_{BIAS} and I_{MOD} below 10% of nominal			50	ms
SOFT P-DOWN/RST Deassert Time	$t_{PDR-OFF\_SOFT}$	I_{BIAS} and I_{MOD} above 90% of nominal			200	ms
Soft MOD-NR Assert Delay	$t_{MOD-NR-ON\_SOFT}$	Time from fault to MOD-NR assertion			50	ms
Soft MOD-NR Deassert Delay	$t_{MOD-NR-OFF\_SOFT}$	Time from read (clear flags) to MOD-NR deassertion			50	ms
Soft RX_LOS Assert Time	t_{LOS-ON_SOFT}	Time from SC-RX-LOS assertion to RX-LOS assertion			50	ms
Soft RX_LOS Deassert Time	$t_{LOS-OFF\_SOFT}$	Time from SC-RX-LOS deassertion to RX-LOS deassertion			50	ms
Analog Parameter Data Ready (DATA-NR)					500	ms

**All SOFT timing specifications are measured from the falling edge of STOP signal during I^2C communication.*

ANALOG INPUT CHARACTERISTICS

(V_{CC3} = +2.9V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I_{BMD} Configurable Source or Sink (+/-)				0.05		1.50	mA
I_{BMD} Voltage (I_{BMD} - 0µA)	V_{BMD}	Source mode	I_{BMD} range 0 to 1.5mA		2.0		V
		Sink mode			1.2		
I_{BMD} Input Resistance	R_{BMD}			400	550	700	Ω

A/D INPUT VOLTAGE MONITORING (IBIASMON, AUX2MON, AUX1MON, RSSI, BMD)

(V_{CC3} = +2.9V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Resolution	ΔV_{MON}			610		µV
Supply Resolution	$\Delta V_{CC2/3}$			1.6		mV
Input/Supply Accuracy	A_{CC}	At factory setting		0.25	0.5	%FS
Update Rate	t_{FRAME1}	AUX1MON and AUX2MON disabled		48	52	ms
	t_{FRAME2}	All channels enabled		64	75	
Input/Supply Offset	V_{OS}	(Note 4)		0	5	LSB
Full-Scale Input (IBIASMON and RSSI)		At factory setting	2.4875	2.5	2.5125	V
Full-Scale Input (AUX1MON, AUX2MON, V_{CC2}, V_{CC3})		At factory setting (Note 9)	6.5208	6.5536	6.5864	V
BMD (Monitor) (TX-P)		FS setting		1.5		mA

FAST ALARMS AND V_{CC} FAULT CHARACTERISTICS

(V_{CC3} = +2.9V to +5.5V, V_{CC2} = +1.6V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH BIAS and TX-P Threshold FS		(Note 10)	2.48	2.5	2.52	mA
$V_{CC2/3}$ Fault Asserted Falling Edge Delay		↓ $V_{CC2/3}$ (Note 11)			75	ms
QT Temperature Coefficient			-3		+3	%
QT Voltage Coefficient					0.5	%/V
QT FS Trim Accuracy (4.2V, +25°C)			2.480	2.500	2.520	mA
QT Accuracy (Trip) (INL)			-2	0	+2	LSB
QT Voltco					0.5	%/V
QT Tempco				1.5	3	%

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC3} = +2.9V to +5.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Endurance (Write Cycle)		+70°C	50k			Cycles
Endurance (Write Cycle)		+25°C	200k			Cycles

Note 1: All voltages are referenced to ground. Current into the IC is positive, and current out of the IC is negative.

Note 2: Secondary power supply is used to support optional variable power-supply feature of the XFP module. If V_{CC2} is not used (i.e., signal conditioners using 3.3V supply), V_{CC2} should be connected to the V_{CC3}.

Note 3: Input signals (i.e., TX-D, MOD-DESEL, and P-DOWN/RST) have internal pullup resistors.

Note 4: Guaranteed by design. Simulated over process and 50µA < I_{BMD} < 1500µA.

Note 5: C_B—total capacitance of one bus line in picofarads.

Note 6: EEPROM write begins after a STOP condition occurs.

Note 7: This is the maximum and minimum voltage on the MODSET and BIASSET pins required to meet accuracy and drift specifications.

Note 8: For V_{THRSET}, offset may be as much as 10mV.

Note 9: This is the uncalibrated offset provided by the factory; offset adjustment is available on this channel.

Note 10: %FS refers to calibrated FS in case of internal calibration, and uncalibrated FS in the case of external calibration. Uncalibrated FS is set in the factory and specified in this data sheet as FS (factory). Calibrated FS is set by the user, allowing a change in any monitored channel scale.

Note 11: See the *Monitor Channels* section for more detail or V_{CC2} and V_{CC3} selection.

XFP Laser Control and Digital Diagnostic IC

Timing Diagrams

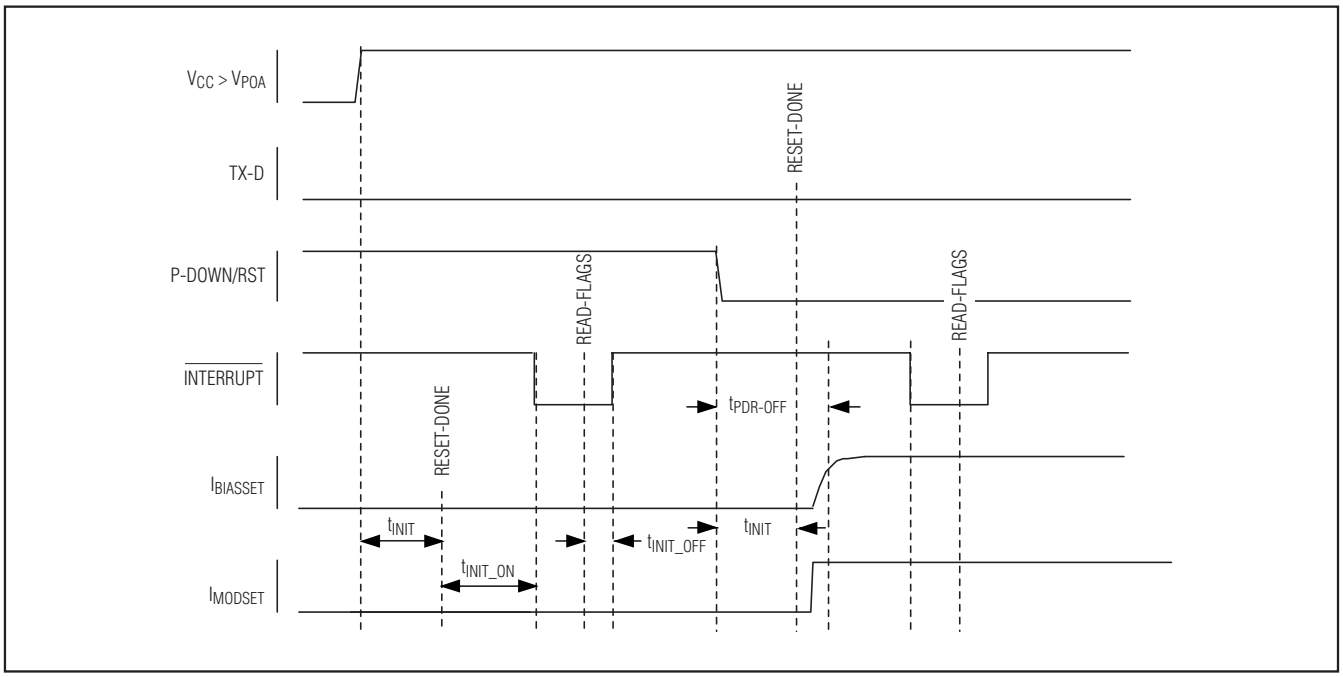

Figure 1. Power-On Initialization with P-DOWN/RST Asserted and TX-D/SOFT TX-D Not Asserted

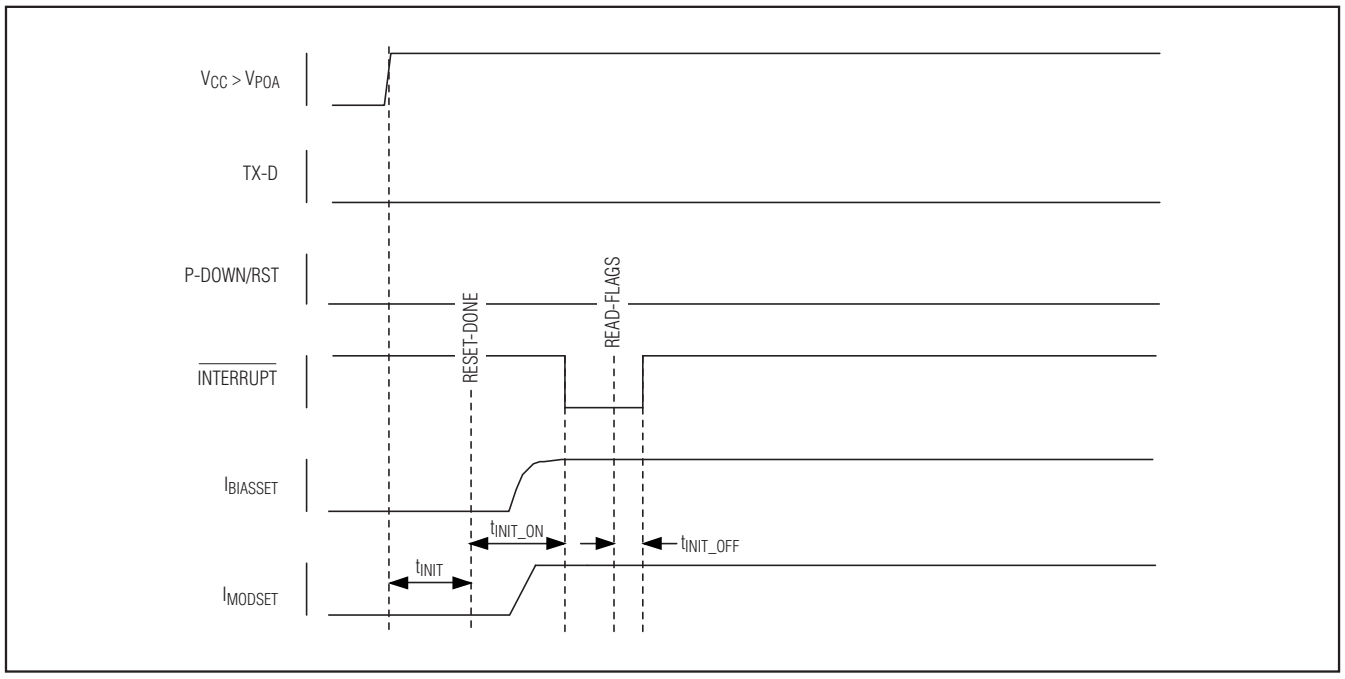

Figure 2. Power-On Initialization with P-DOWN/RST Not Asserted and TX-D/SOFT TX-D Not Asserted (Normal Operation)

Timing Diagrams (continued)

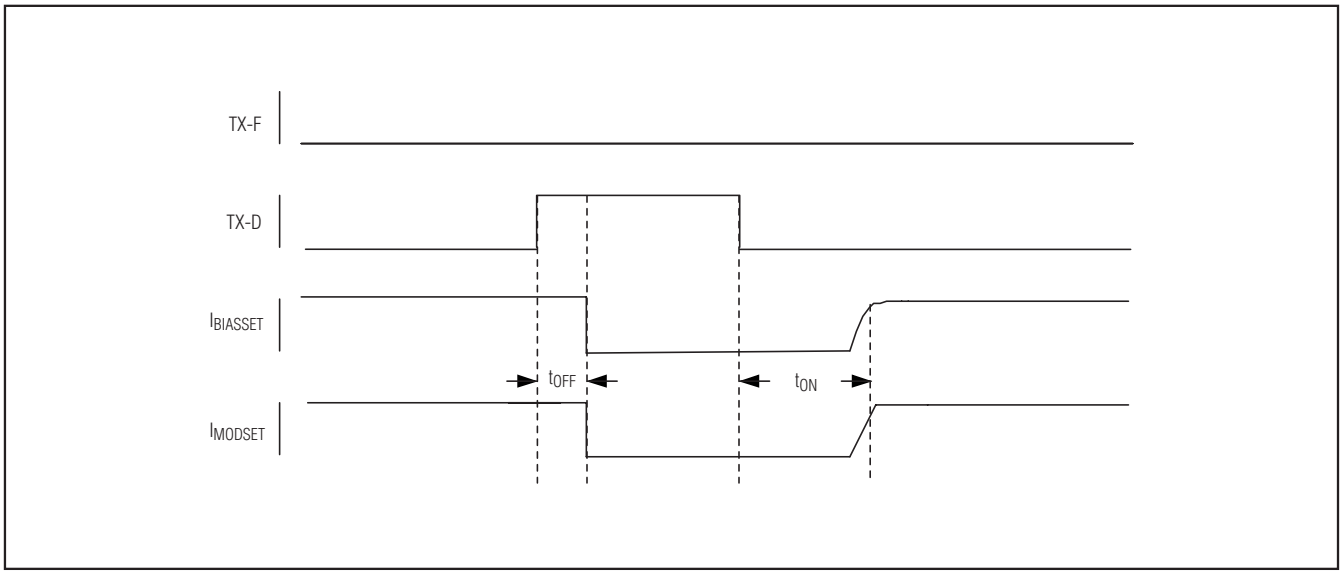

Figure 3. TX-D Timing During Normal Operation

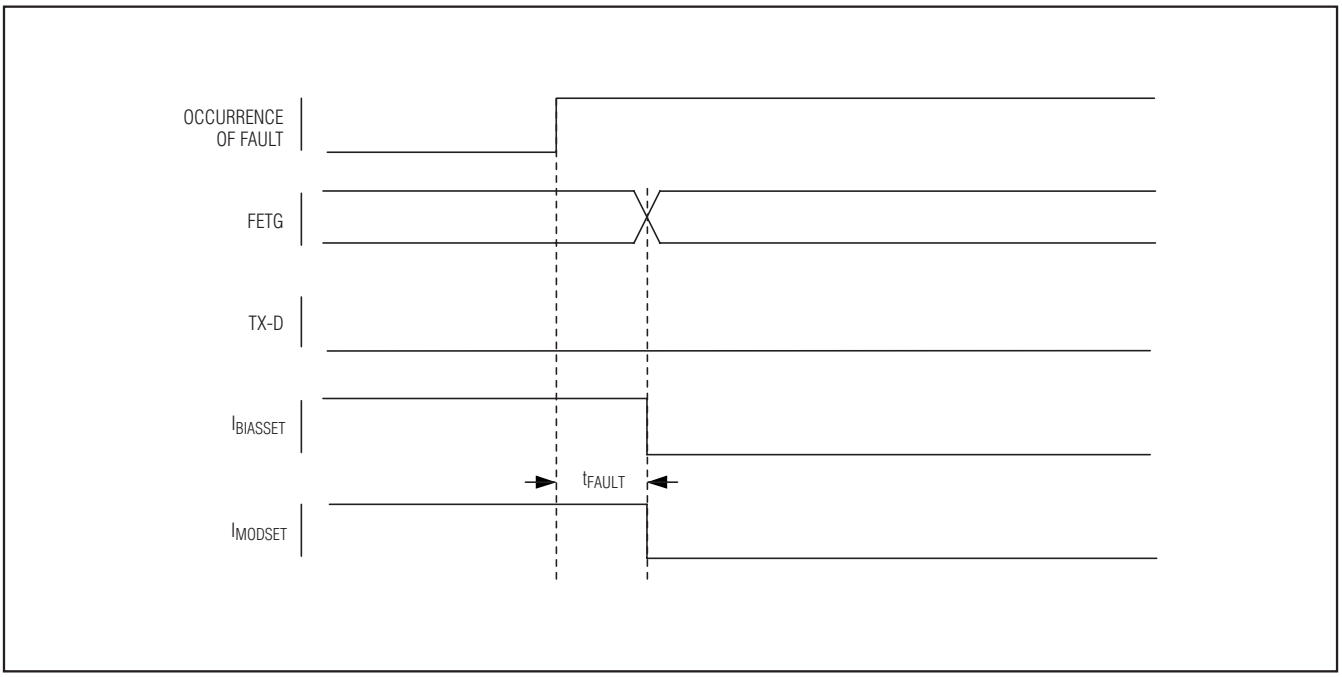

Figure 4. Detection of Safety Fault Condition

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Timing Diagrams (continued)

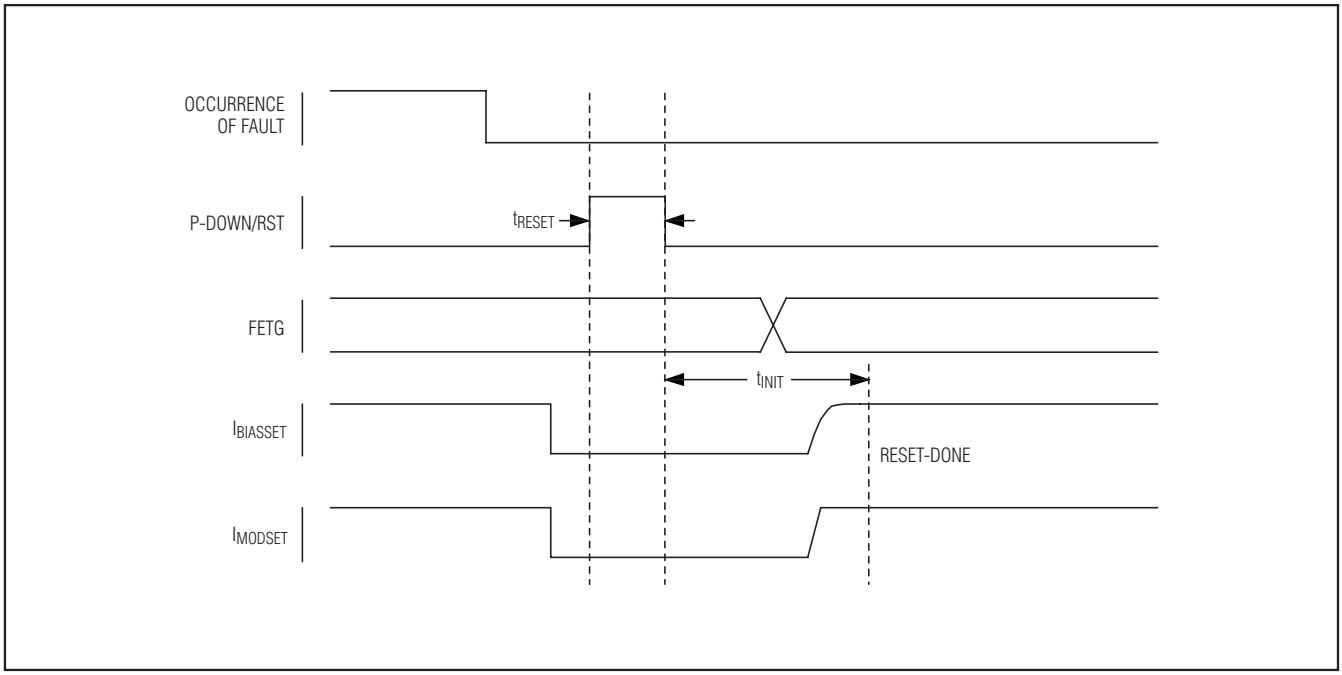


Figure 5. Successful Recovery from Transient Safety Fault Condition Using P-DOWN/RST

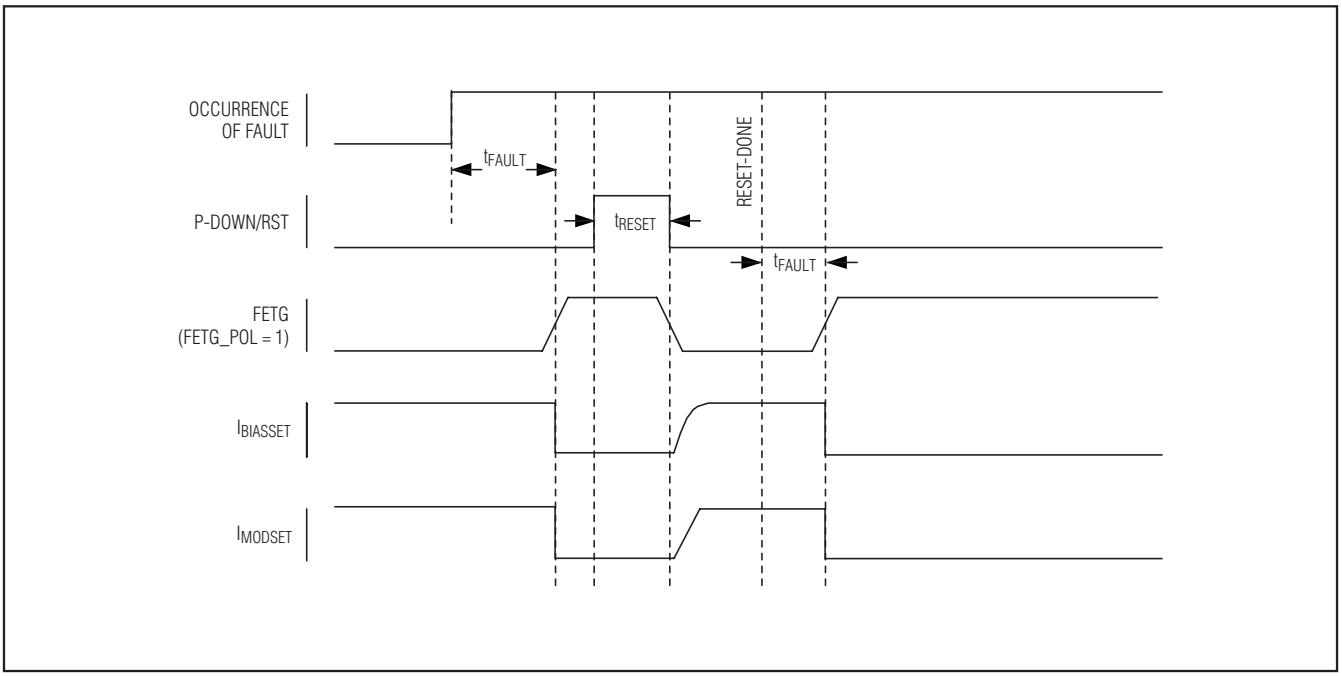


Figure 6. Unsuccessful Recovery from Transient Safety Fault Condition

Timing Diagrams (continued)

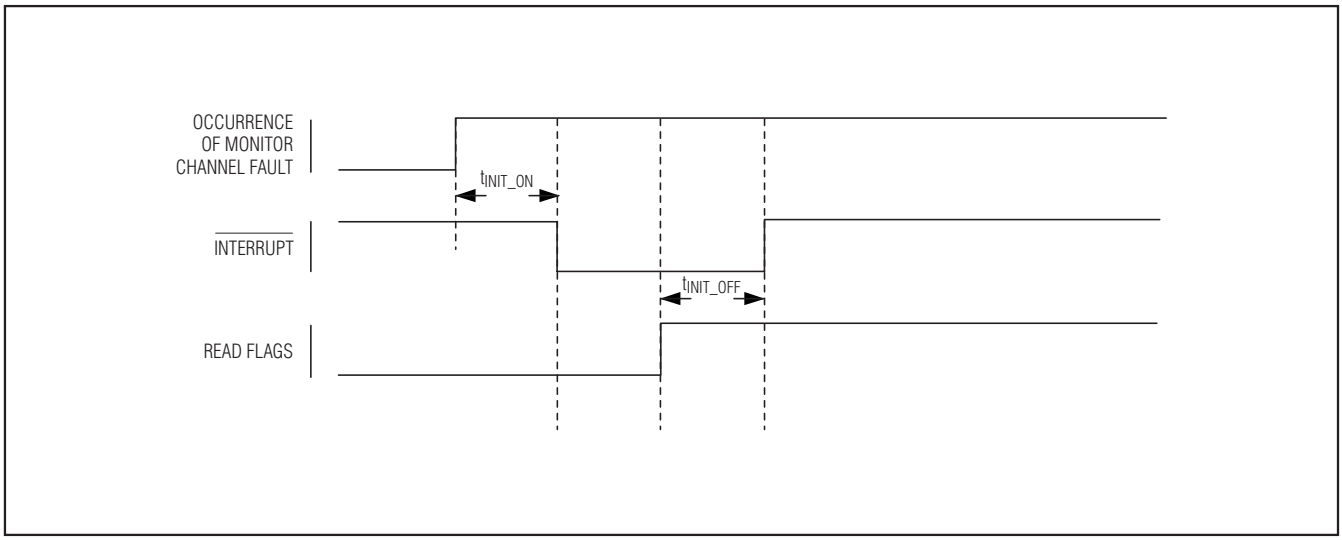


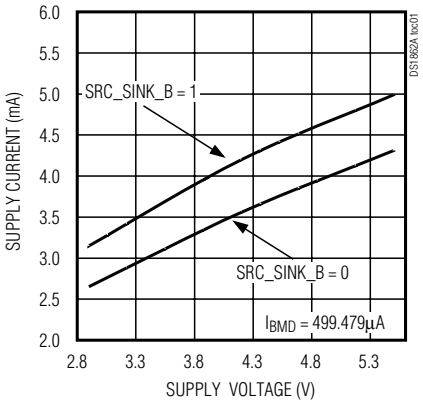
Figure 7. Monitor Channel Fault Timing

XFP Laser Control and Digital Diagnostic IC

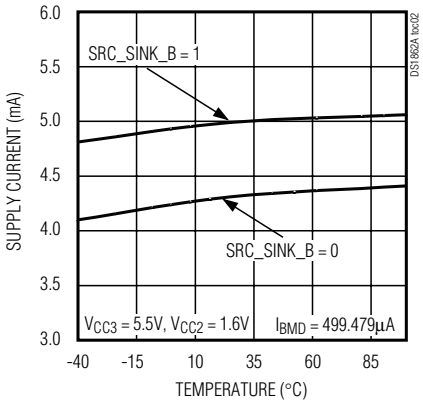
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

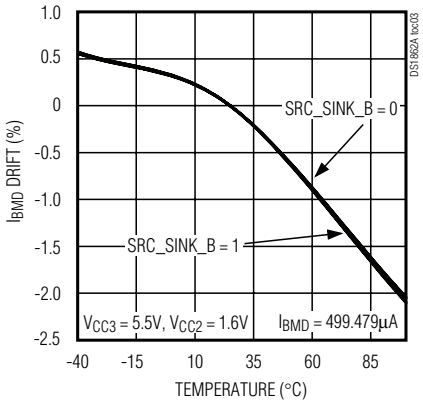
SUPPLY CURRENT vs. SUPPLY VOLTAGE



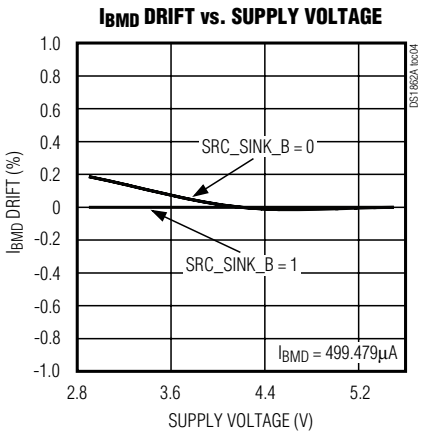
SUPPLY CURRENT vs. TEMPERATURE



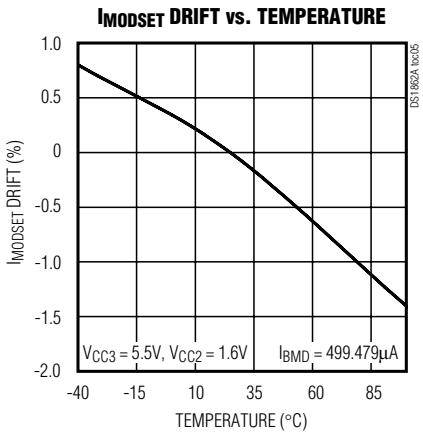
IBMD DRIFT vs. TEMPERATURE



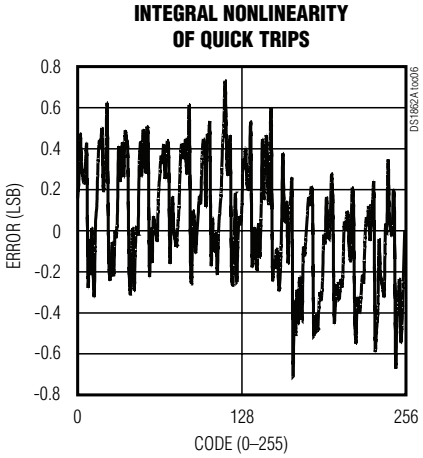
IBMD DRIFT vs. SUPPLY VOLTAGE



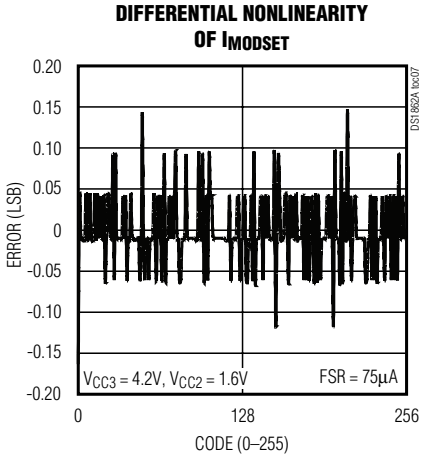
IMODSET DRIFT vs. TEMPERATURE



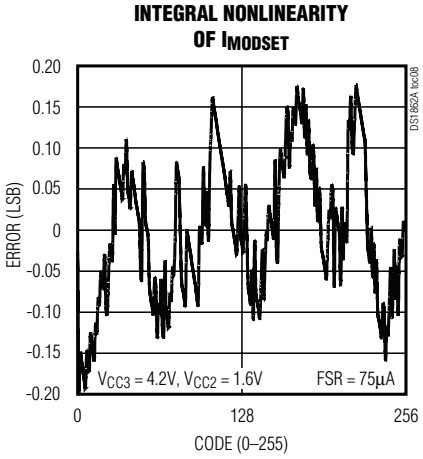
INTEGRAL NONLINEARITY OF QUICK TRIPS



DIFFERENTIAL NONLINEARITY OF IMODSET



INTEGRAL NONLINEARITY OF IMODSET



Pin Description

NAME	PIN	FUNCTION
P-DOWN/RST	A1	**Power-Down/Reset Input.** This multifunction pin is pulled high internally. See the *Power-Down/Reset Pin* section for additional information.
SC-RX-LOS	A2	**Signal Conditioner Receiver Loss-of-Signal Input.** This pin is an active-high input with LVCMOS/LVTTL voltage levels.
SC-RX-LOL	A3	**Signal Conditioner Receiver Loss-of-Lock Input.** This pin is an active-high input with LVCMOS/LVTTL voltage levels.
THRSET	A4	**Threshold Set Output.** This pin is a programmable voltage source that can be used for Rx signal conditioner.
V_{CC2}	A5	**1.8V Power-Supply Input**
RX-LOS	B1	**Receiver Loss of Signal.** This open-drain output indicates when there is insufficient optical power.
SCL	B2	**I^2C Serial-Clock Input**
FETG	B3	**FET Gate Output.** This pin can drive an external FET gate associated with safety fault disconnect.
RSSI	B4	**Received Power Signal Input**
MODSET	B5	**Modulation Current Output.** This pin is only capable of sinking current.
TX-D	C1	**Transmit Disable Input.** This pin has an internal pullup resistor.
SDA	C2	**I^2C Serial-Data Input/Output**
EN1	C3	**Enable 1 Output.** Functional control for signal conditioners.
EN2	C4	**Enable 2 Output.** Functional control for signal conditioners.
BIASSET	C5	**Bias Current Output.** This pin is only capable of sinking current.
$\overline{\text{INTERRUPT}}$	D1	**Interrupt.** This open-drain output pin indicates a possible operational fault or critical status condition to the host.
MOD-NR	D2	**Indicating Module Operational Fault.** Open-drain output. This pin indicates the status of the MOD-NR flag.
AUX1MON	D3	**Aux1 Monitor Input.** This pin can be used to measure any voltage quantity.
AUX2MON	D4	**Aux2 Monitor Input.** This pin can be used to measure any voltage quantity or external temperature
BMD	D5	**Monitor Diode Current Input.** This pin is capable of sourcing or sinking current.
GND	E1	**Ground**
MOD-DESEL	E2	**Module Deselect Input.** This pin must be pulled low to enable I^2C communication. This pin is pulled high internally.
IBIASMON	E3	**Bias Monitor Input.** This pin can be used to monitor the voltage across the laser.
SC-TX-LOS	E4	**Signal Conditioner Transmitter Loss of Signal.** This pin is an active-high input with LVCMOS/LVTTL voltage levels.
V_{CC3}	E5	**3.3V or 5V Power-Supply Input**

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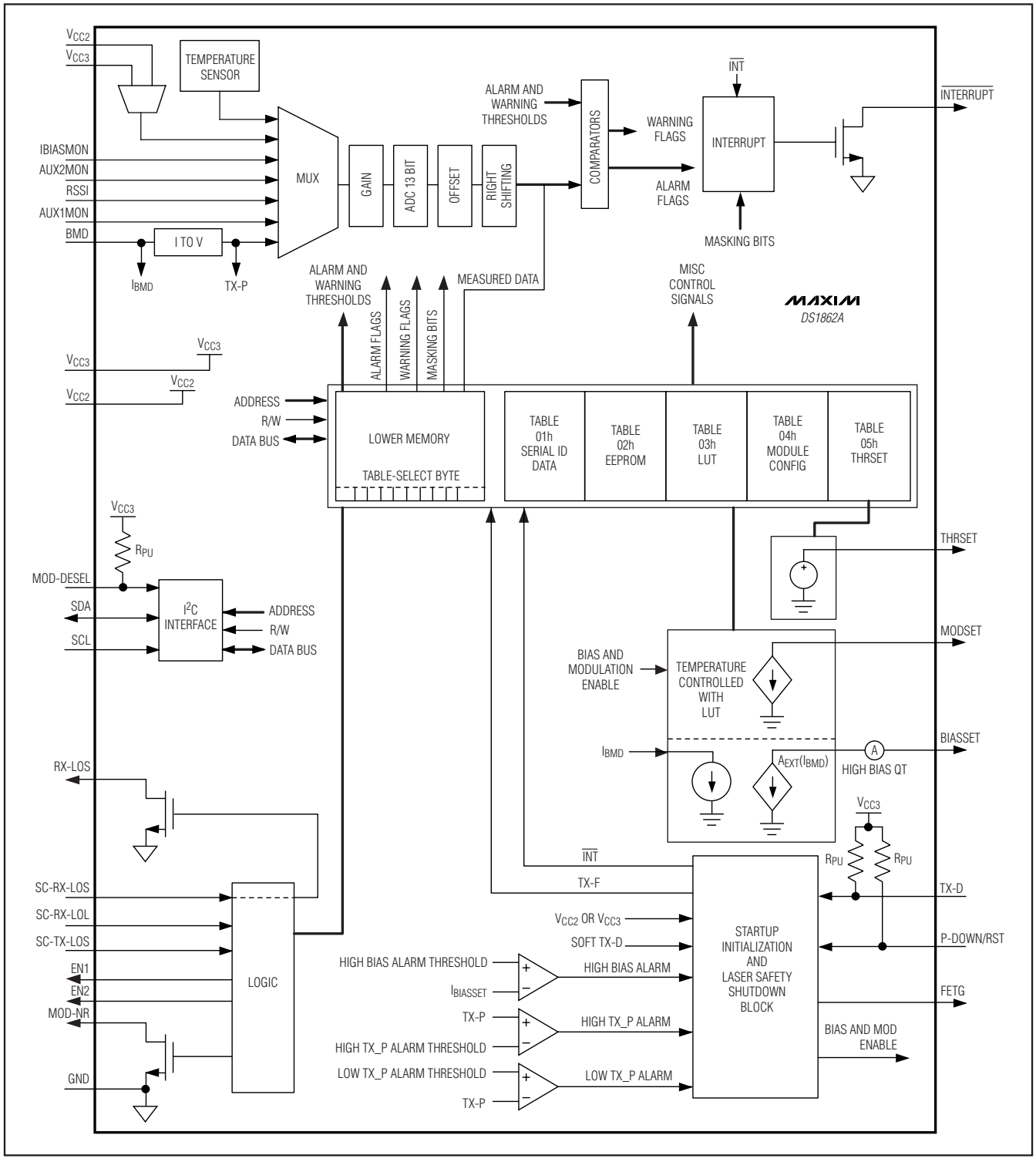
Block Diagram



Detailed Description

The DS1862A's block diagram is described in detail within the following sections and memory map/memory description.

Automatic Power Control (APC)

The DS1862A's APC is accomplished by closed-loop adjustment of the bias current (BIASSET) until the feedback current (BMD) from a photodiode matches the value determined by the APC registers. The relationship between the APC register and I_{BMD} is given by:

$$I_{BMD} = 5.859\mu A \times APC_C<7:0> + (1.464\mu A \times APC_F<1:0>)$$

where $APC_C<7:0>$ is the 8-bit value in Table 04h, Byte 84h that controls the coarse BMD current, and $APC_F<1:0>$ is the 2-bit value that controls the fine BMD current.

The BMD pin appears as a voltage source in series with two resistors. The overall equivalent resistance of the BMD input pin can be closely approximated by the plot in Figure 8. The voltage that appears on the BMD pin, assuming no external current load, is 1.2V if BMD is in sink-current mode (SRC_SINK_B = 0) or 2.0V if BMD is set to source current (SRC_SINK_B = 1). This allows the photodiode to be referenced to either V_{CC3} or GND. When the control loop is at steady state, the BMD current setting matches the current that is measured by the I_{BMD} voltage across the internal resistance. During a transient period, the DS1862A adjusts the current drive on the BIASSET pin to bring the loop into steady state. The DS1862A is designed to support loop gains of 1/20 to 10.

On power-up, the BMD current ramps up to the previously saved current setting in EEPROM APC registers. While operating, the DS1862A monitors the BMD current. If it begins to deviate from the desired (set) I_{BMD} value, the current on the BIASSET pin is again adjusted to compensate.

Extinction Ratio Control Lookup Table (LUT)

The DS1862A uses a temperature indexed lookup table (LUT) to control the extinction ratio. The MODSET pin is capable of sinking current based on the 8-bit binary value that is controlling it. The DS1862A also features a user-configurable current range to increase extinction ratio resolution. Five current ranges, as described in Table 1, are available to control the current entering MODSET.

Table 1. Selectable Current Ranges for MODSET

LUT CURRENT RANGE TABLE 04h, BYTE 86h<2:0>	CURRENT RANGE (µA)
000	0 to 75
001	0 to 150
010	0 to 300
011	0 to 600
100	0 to 1200

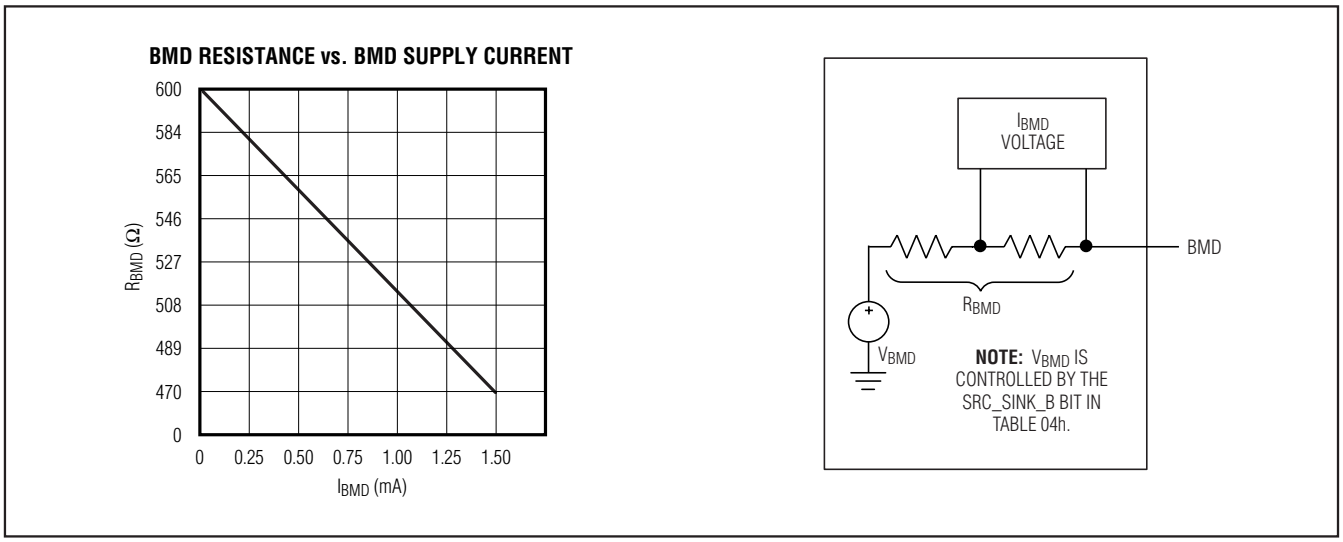


Figure 8. Approximate Model of the BMD Input

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If the largest current range is selected, the maximum value of FFh (from LUT) corresponds to a 1200µA sink current. Regardless of the current range, the MODSET value always consists of 256 steps, including zero.

I_{MODSET} can be controlled automatically with the temperature-based lookup table, or by three other manual methods.

Automatic temperature addressed lookup is accomplished by an internal or external temperature sensor controlling an address pointer. This pointer indexes through 127 previously loaded 8-bit current values stored in the LUT. Each one of the 127 temperature slot locations corresponds to a 2°C increment over the -40°C to +102°C temperature range. Any temperature above or below these points causes the code in the first or last temperature slot to be indexed. Both the internal temperature sensor and an external sensor connected to AUX2MON are capable of providing a signal to control the extinction ratio automatically with an indexed LUT. Table 2 illustrates the relationship between the temperature and the memory locations in the LUT.

Table 2. Temperature Lookup Table

TEMPERATURE (°C)	CORRESPONDING LOOKUP TABLE ADDRESS
< -40	80h
-40	80h
-38	81h
-36	82h
…	…
+96	C4h
+98	C5h
+100	C6h
+102	C7h
> +102	C7h

Automatic and manual control of MODSET is controlled by two bits, TEN and AEN, that reside in Table 04h, Byte B2h. By default (from factory) TEN and AEN are both set, causing complete automatic temperature-based lookup. If TEN and/or AEN are altered, the DS1862A is set to one of the manual modes. Table 3 describes manual mode functionality.

Table 3. Truth Table for TEN and AEN Bits

TEN	AEN	DS1862A LUT FUNCTIONALITY
0	0	Manual mode that allows users to write a value directly to the LUT VALUE register (Table 04h, Byte B1h) to drive MODSET. While in this mode, the LUT INDEX POINTER register is not being updated, and no longer drives the LUT VALUE register.
0	1	Manual mode that allows users to write a value directly to the LUT VALUE register (Table 04h, Byte B1h) to drive MODSET. While in this mode, the LUT INDEX POINTER register is still being updated; however, it no longer drives the LUT VALUE register.
1	0	Manual mode that allows users to write a value to the LUT INDEX POINTER register (Table 04h, Byte B0), then the DS1862A updates the LUT VALUE register (Table 04h, Byte B1h) based on the user's index pointer.
1	1	Automatic mode (factory default). This mode automatically indexes the LUT based on temperature, placing the resulting LUT address in the LUT INDEX POINTER register (Table 04h, Byte B0h). Then the MODSET setting is transferred from that LUT address to the LUT VALUE register (Table 04h, Byte B1h). Lastly, the I_{MODSET} is set to the new MODSET code.

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Monitor Channels

The DS1862A has seven monitored voltage signals that are polled in a round-robin multiplexed sequence and are updated with the frame rate, t_{FRAME}. All channels are read as 16-bit values, but have 13-bit resolution, and with the exception of temperature measurements, all channels are stored as unsigned values. The resulting 16-bit value for all monitored channels, except internal temperature, is calculated by internally averaging the analog-to-digital result eight times. The resulting internal temperature monitor channel is averaged 16 times. See the *Internal Calibration* section for a complete description of each channel's method(s) of internal calibration.

The AUX1MON, AUX2MON, and $V_{CC2/3}$ monitor channels are optional and can be disabled. This feature allows for shorter frame rate for the essential monitor channels. Channels that cannot be disabled are internal temperature, BMD, RSSI, and IBIASMON. A table of full-scale (FS) signal values (using factory internal calibration without right shifting) and the resulting FS code values for all seven channels is provided in Table 4.

Measuring Temperature—Internal or External

The DS1862A is capable of measuring temperature on three different monitor channels: internal temperature sensor, AUX1MON, and AUX2MON. Only the internal temperature and AUX2MON channels are capable of indexing the LUT to control the extinction ratio. To use an external temperature sensor on AUX2MON, the TEMP_INT/EXT bit in Table 04h, Byte 8Bh, must be set. While AUX2MON controls the extinction ratio, the internal temperature sensor does not stop running; despite extinction ratio control by AUX2MON, it is this internal temperature signal that continues to control the status of temperature flags. Also, when TEMP_INT/EXT = 1, the internal temperature clamps at -40°C and +103.9375°C, and when TEMP_INT/EXT = 0 it clamps at -120°C and +127.984°C. AUX2MON, however, does have its own flag to indicate an out-of-tolerance condition and assert the $\overline{\text{INTERRUPT}}$ pin.

Both AUX1MON and AUX2MON can be used to measure temperature as a function of voltage on their respective pins. They can be enabled by selecting either 0h or 4h from Table 5. Internal (or external) calibration may be required to transmute the input voltage to the desired two's-complement digital code, readable from the result registers in lower memory, Bytes 6Ah, 6Bh, 6Ch, 6Dh.

Measuring $V_{CC2/3}$

The DS1862A has the flexibility to internally measure either V_{CC2} or V_{CC3} to monitor supply voltage. V_{CC2} or V_{CC3} is user selectable by the $V_{CC2/3}$_SEL bit in Table 01h, Byte DCh. To remove $V_{CC2/3}$ from the round-robin monitor update scheme, despite having V_{CC2} or V_{CC3} selected to be monitored, the Reserve_EN bit in Table 04h, Byte 8Bh can be programmed to a 0. The analog power-on-reset flag, POA, indicates the status of V_{CC3} power supply. Even though POA seems to behave similarly to $V_{CC2/3}$ monitor channel, it is completely separate and has no connection.

RESERVE_EN	$V_{CC2/3}$_SEL	RESULT
0	0	$V_{CC2/3}$ result not enabled.
0	1	$V_{CC2/3}$ result not enabled.
1	0	V_{CC3} is being measured.
1	1	V_{CC2} is being measured.

Measuring APC and Laser Parameters—BMD, IBIASMON, RSSI

BMD and BIASSET are used to control and monitor the laser functionality. Regardless of the set BMD current in the APC register, the DS1862A measures BMD pin current and uses this value not only to adjust the current on the BIASSET pin, but also to monitor TX-P as well. The IBIASMON pin is used to input a voltage signal to the DS1862A that can be used to monitor the bias current through the laser. This monitor channel does not drive the HIGH BIAS quick-trip (QT) alarms for safety

Table 4. Monitor Channel FS and LSB Detail

SIGNAL	+FS SIGNAL	+FS (hex)	-FS SIGNAL	-FS (hex)	LSB
Temperature	127.984°C	7FF8	-120°C	8800	0.0625°C
$V_{CC2/3}$	6.5528V	FFF8	0V	0000	100µV
IBIASMON	2.4997V	FFF8	0V	0000	38.147µV
RSSI	2.4997V	FFF8	0V	0000	38.147µV
AUX1MON	6.5528V	FFF8	0V	0000	38.147µV
AUX2MON	6.5528V	FFF8	0V	0000	38.147µV
BMD (TX-P)	1.5mA	FFF8	0mA	0000	22.888nA

fault functionality, current on the BIASSET pin is monitored by the DS1862A to control the HIGH BIAS quick-trip alarm. Similar to TX-P, the RSSI pin is used to measure the received power, RX-P.

Measuring Voltage Quantities using AUX1MON and AUX2MON

AUX1MON and AUX2MON are auxiliary monitor inputs that may be used to measure additional parameters. AUX1/2MON feature a user-selectable register that determines the measured value's units (i.e., voltage, current, or temperature). In addition to indicating units, some of the 4-bit op codes, in Table 5, also place the part in special modes used for alarms and faults internally. Whichever units' scale is selected, the DS1862A is only capable of measuring a positive voltage quantity, therefore internal or external calibration may be required to get the binary value to match the measured quantity. A table of acceptable units and/or their corresponding user-programmable 4-bit op code is provided below.

Table 5. AUX1/2MON Functionality Selection (Unit Selection)

VALUE	DESCRIPTION OF AUX1/2MON INTENDED USE (UNITS OF MEASURE)
0000b	Auxiliary monitoring not implemented
0001b	APD bias voltage (16-bit value is voltage in units of 10mV)
0010b	Reserved
0011b	TEC current (mA) (16-bit value is current in units of 0.1mA)
0100b	Laser temperature (same encoding as module temperature)
0101b	Laser wavelength
0110b	+5V supply voltage (encoded as primary voltage monitor)
0111b	+3.3V supply voltage (encoded as primary voltage monitor)
1000b	+1.8V supply voltage (encoded as primary voltage monitor) (V_{CC2})
1001b	-5.2V supply voltage (encoded as primary voltage monitor)
1010b	+5V supply current (16-bit value is current in 0.1mA)
1101b	+3.3V supply current (16-bit value is current in 0.1mA)
1110b	+1.8V supply current (16-bit value is current in 0.1mA)
1111b	-5.2V supply current (16-bit value is current in 0.1mA)

Alarms and Warning Flags Based on Monitor Channels

All of the monitor channels feature alarm and warning flags that are asserted automatically as user-programmed thresholds are internally compared with monitor channel results. Flags may be set, which, if not masked, will generate an interrupt on the $\overline{\text{INTERRUPT}}$ pin or generate a safety fault. Whenever $V_{CC2/3}$, AUX2MON, AUX1MON, RSSI, and internal temperature go beyond their threshold trip points and the corresponding mask bit is 0, an interrupt is generated on the $\overline{\text{INTERRUPT}}$ pin and a corresponding warning or alarm flag is set. Similarly, a safety fault occurs whenever BMD or BIASSET go beyond threshold trip points. When this happens, the FETG pin immediately asserts and BIASSET and MODSET currents are shut down.

Monitor Channel Conversion Example

Table 6 provides an example of how a 16-bit ADC code corresponds to a real life measured voltage using the factory-set calibration on either RSSI or IBIASMON. By factory default, the LSB is set to 38.147µV.

Table 6. A/D Conversion Example

MSB (BIN)	LSB (BIN)	VOLTAGE (V)
11000000	00000000	1.875
10000000	10000000	1.255

To calculate V_{CC2}, V_{CC3}, AUX1MON, or AUX2MON, convert the unsigned 16-bit value to decimal and multiply by 100µV.

To calculate the temperature (internal), treat the two's-complement value binary number as an unsigned binary number, then convert it to decimal and divide by 256. If the result is grater than or equal to 128, subtract 256 from the result.

Temperature: high byte = -128°C to +127°C signed; low byte = 1/256°C.

Table 7. Temperature Bit Weights

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	—	—	—

Table 8. Temperature Conversion Examples

MSB (BIN)	LSB (BIN)	TEMPERATURE (°C)
01000000	00000000	+64
01000000	00001000	+64.03215
01011111	00000000	+95
11110110	00000000	-10
11011000	00000000	-40

Internal Calibration

The DS1862A has two means for scaling an analog input to a digital result. The two devices alter the gain and offset of the signal to be calibrated. All of the inputs except internal temperature have unique registers for both the gain and the offset that can be found in Table 04h. See the table below for a complete description of internal calibration capabilities including right-shifting for all monitor channels.

Table 9. Internal Calibration Capabilities

SIGNAL	INTERNAL SCALING	INTERNAL OFFSET	RIGHT-SHIFTING
Temperature	—	x	—
$V_{CC2/3}$	x	x	—
IBIASMON	x	x	x
RSSI (RX-P)	x	x	x
AUX1MON	x	x	x
AUX2MON	x	x	x
BMD (TX-P)	x	x	x

To scale a specific input's gain and offset, the relationship between the analog input and the expected digital result must be known. The input that would produce a corresponding digital result of all zeroes is the null value (normally this input is GND). The input that would produce a corresponding digital result of all ones is the full-scale (FS) value minus one LSB. The FS value is also found by multiplying an all ones digital value by the weighted LSB. For example, a digital reading is 16 bits long, assume that the LSB is known to be 50µV, then the FS value would be 2^{16} x 50µV = 3.2768V.

A binary search can be used to find the appropriate gain value to achieve the desired FS of the converter. Once the gain value is determined, then it can be loaded into the appropriate channels' Gain register. This requires forcing two known voltages on to the monitor input pin. For best results, one of the forced voltages should be the NULL input and the other should be 90% of FS. Since the LSB of the least significant byte in the digital reading register is known, the expected digital results are also known for both the null and FS value inputs. Figure 9 describes the hysteresis built into the DS1862A's LUT functionality.

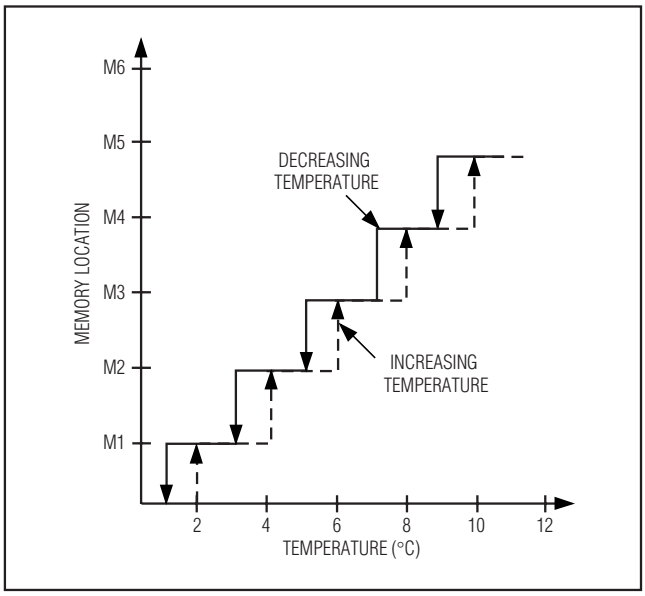

Figure 9. Lookup Table Hysteresis

With the exception of BMD, which can source or sink current, all monitored channels are high impedance and are only capable of directly measuring a voltage. If other measured quantities are desired, such as light, frequency, power, current, etc., they must be converted to a voltage. In this situation the user is not interested in voltage measurement on the monitored channel, but the measurement of the desired parameter. Only the relationship between the indirect measured quantity (light, frequency, power, current, etc.) to the expected digital result must be known.

An example of gain scaling using the recommended binary search procedure is provided with the following pseudo code.

To help will the computation, two integers need to be defined: count 1 and count 2. CNT1 = NULL / LSB and CNT2 = 90%FS / LSB. CLAMP is the largest result that can be accommodated.

```
/* Assume that the Null input is 0.5V. */
/* In addition, the requirement for LSB is 50µV. */
    FS = 65536 * 50e-6;          /* 3.2768 */
    CNT1 = 0.5 / 50e-6;          /* 10000 */
    CNT2 = 0.90*FS / 50e-6;      /* 58982 */
/* Thus the NULL input of 0.5V and the 90% of FS input
is 2.94912V. */
    set the trim-offset-register to zero;
    set Right-Shift register to zero (Typically zero.
    See the Right-Shifting section);
    gain_result = 0h;
    CLAMP = FFF8h/2^(Right_Shift_Register);
    For n = 15 down to 0
    begin
        gain_result = gain_result + 2^n;
        Force the 90% FS input (2.94912V);
        Meas2 = read the digital result from the part;
    If Meas2 >= CLAMP then
        gain_result = gain_result - 2^n;
    Else
        Force the NULL input (0.5V);
        Meas1 = read the digital result from the part;
        if (Meas2 - Meas1) > (CNT2 - CNT1) then
        gain_result = gain_result - 2^n;
    end;
    Set the gain register to gain_result;
```

The gain register is now set and the resolution of the conversion will best match the expected LSB. The next step is to calibrate the offset of the DS1862A. With the correct gain value written to the gain register, again force the NULL input to the monitor pin. Read the digital result from the part (Meas1). The offset value is equal to negative value of Meas1.

$$OFFSET\_REGISTER = \left[\frac{(-1)Meas1}{4}\right]$$

The calculated offset is now written to the DS1862A and the gain and offset-scaling procedure is complete.

Right-Shifting A/D Conversion Result (Scalable Dynamic Ranging)

Right-shifting is a digital method used to regain some of the lost ADC range of a calibrated system. If right-shifting is enabled, by simply loading a non-zero value into the appropriate Right-Shifting Register, then the DS1862A shifts the calibrated result just before it is stored into the monitor channels' register. If a system is calibrated so the maximum expected input results in a digital output value of less than 7FFFh (50% of FS), then it is a candidate for using the right-shifting method.

If the maximum desired digital output is less than 7FFFh, then the calibrated system is using less than 1/2 the ADC's range. Similarly, if the maximum desired digital output is less than 1FFFh, then the calibrated system is only using 1/8th the ADC's range. For example, if an applied maximum analog signal yields a maximum digital output less than 1FFCh, then only 1/8th of the ADC's range is used. Right-shifting improves the resolution of the measured signal as part of internal calibration. Without right-shifting, the 3 MS bits of the ADC will never be used. In this example, a value of 3 for the right-shifting maximizes the ADC range and a larger gain setting must be loaded to achieve optimal conversion. No resolution is lost since this is a 13-bit converter that is left justified. The value can be right-shifted 3 times without losing any resolution. The following table describes when the right-shifting method can be effectively used.

Table 10. Right-Shifting Selection

OUTPUT RANGE USED WITH ZERO RIGHT-SHIFTS	NUMBER OF RIGHT-SHIFTS NEEDED
0h .. FFFFh	0
0h .. 7FFFh	1
0h .. 3FFFh	2
0h .. 1FFFh	3
0h .. 0FFFh	4

Warning and Alarm Logic Based on AUX1/2MON, $V_{CC2/3}$, Temp, RX-P, and IBIASMON

The DS1862A is capable of generating an alarm and/or warning whenever an analog monitored channel goes out of a user-defined tolerance. Temperature, bias current (based on IBIASMON), receive power (based on RSSI), AUX1MON, AUX2MON, and $V_{CC2/3}$, are monitored channels that generate latched flags. See the figure below for more detail pertaining to AUX1MON and AUX2MON. Flags are latched into a high state the first time a monitored channel goes out of the defined operating window and for each monitored signal there is a Mask bit that can be set to prevent the corresponding alarm or warning flag from being set. Once a flag is set, it is cleared by simply reading its memory location.

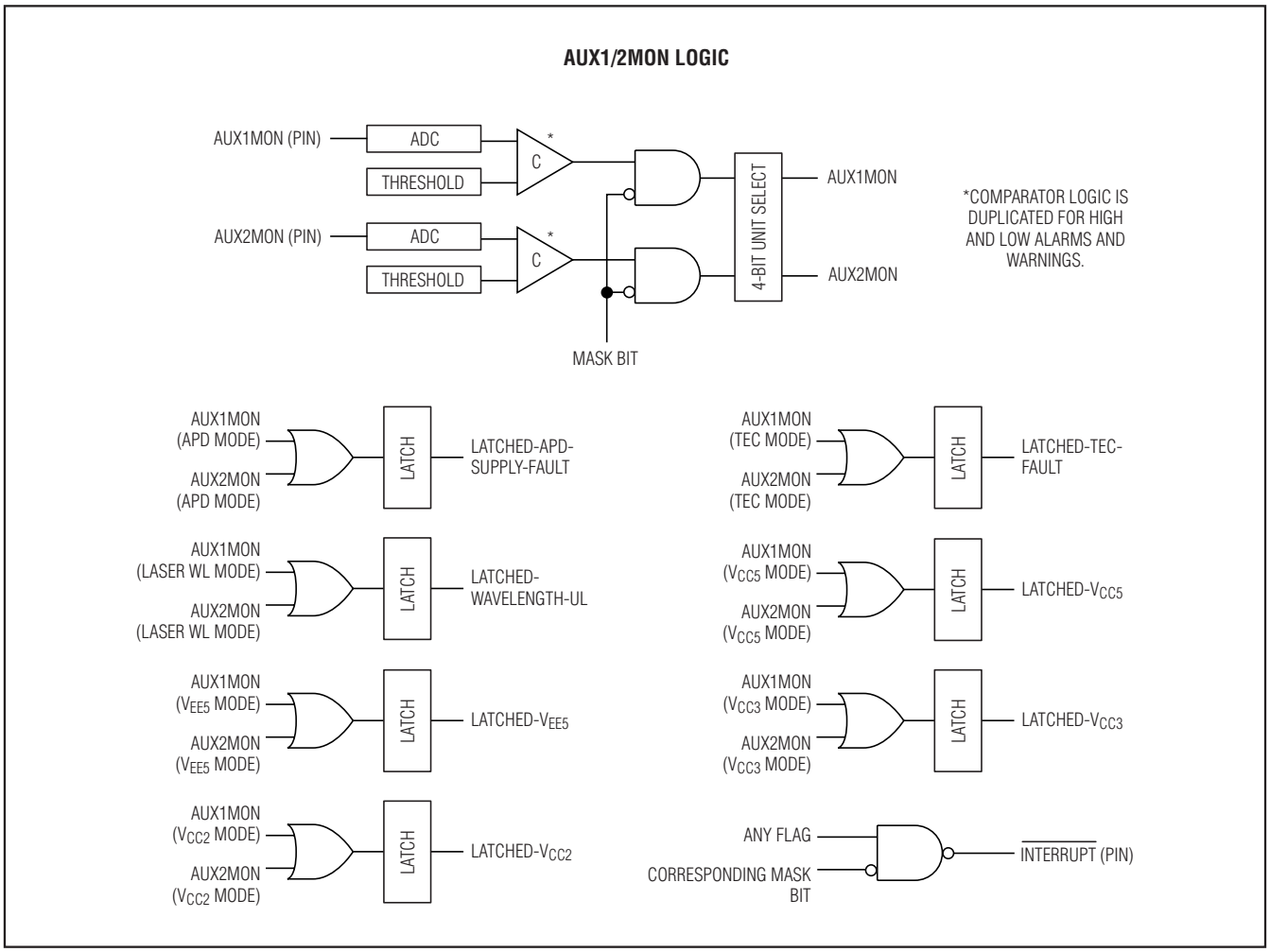

Figure 10. AUX1/2MON Monitor Logic

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Warning and Alarm Logic Based on Signal Conditioners

The DS1862A also has flags that are set by certain logical conditions on signal conditioner (SC) pins: SC-RX-LOL, SC-RX-LOS, SC-TX-LOS. Similarly, for each latched signal conditioner flag there are also mask bits that are capable of preventing the alarm or warning flag from causing an $\overline{\text{INTERRUPT}}$ pin to assert. Again, flags are cleared automatically whenever their memory address is read. See Figure 11 for more detail.

Quick-Trip Logic and FETG Shutdown Functionality

In addition to alarms and warnings, the DS1862A also has quick-trip (QT) functionality (sometimes referred to as fast alarms) that is capable of shutting down the LASER with the FETG pin in conjunction with shutting down I_{MODSET} and $I_{BIASSET}$. I_{BMD} and $I_{BIASSET}$ currents are measured and are compared with user-defined trip points to set the quick-trip flags: QT LOW TX-P, QT HIGH TX-P, and QT HIGH BIAS. These flags are also capable of being masked to prevent FETG from being asserted when an out-of-tolerance condition is detected. FETG is not asserted by setting the TX-D pin, SOFT TX-D, or P-DOWN/RST pin to a high state, however, I_{MODSET}, and $I_{BIASSET}$ will shut down. See Figure 12 for more detail.

The polarity of the FETG pin can also be reversed by setting the FETG_POL bit. Once a safety fault has occurred, the FETG pin and all of the attendant flags

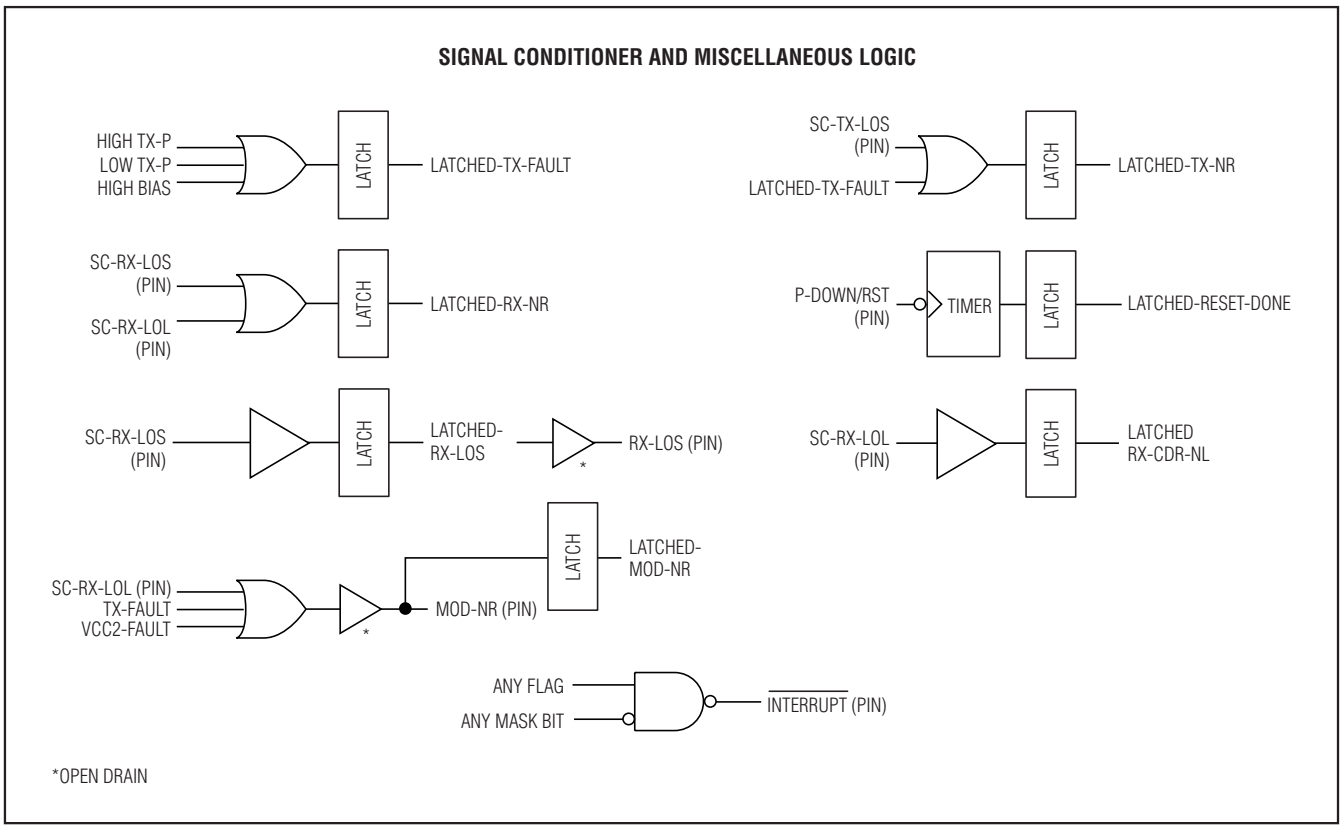

Figure 11. Signal Conditioner and Other Logic

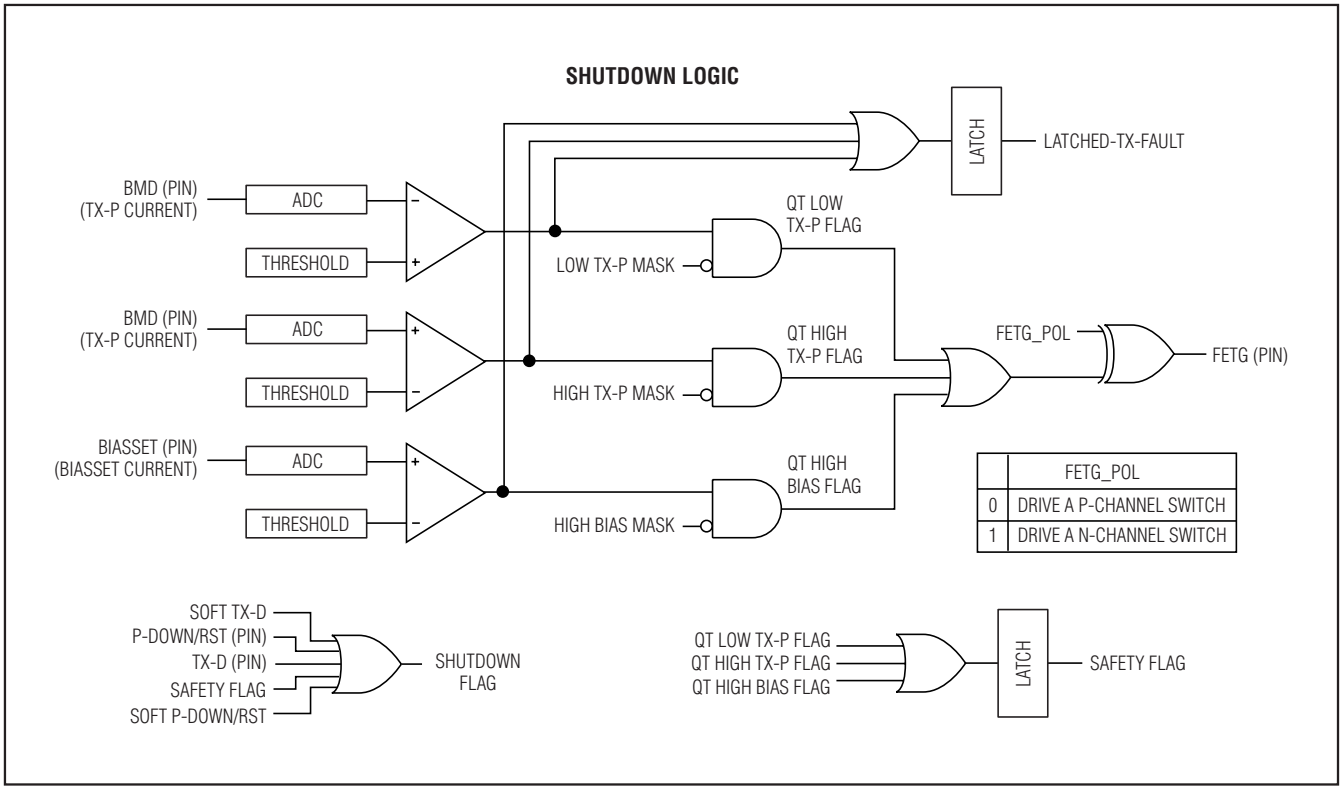

Figure 12. Safety Fault and Shutdown Logic

can only be reset by pulsing the P-DOWN/RST pin high for the reset time, t_{RESET}, or by toggling the SOFT P-DOWN/RST bit in Byte 6Eh, bit 3. See the *Power-Down/Reset Pin* section for more details.

Power-Down/Reset Pin

The P-DOWN/RST pin is a multifunction input pin that resets and/or powers down the DS1862A. Since the pin is internally pulled up, its normal state is released, which corresponds to power-down mode. If the P-DOWN/RST pin is released, or driven high, the DS1862A responds by shutting down the MODSET and BIASSET currents. Once the pin is pulled low, operation continues (if not inhibited by a safety fault). Besides powering down the DS1862A, a high-going pulse with minimum reset time, t_{RESET}, can be applied to the P-DOWN/RST pin. This is necessary to restart the DS1862A, especially if it is in a safety shutdown condition and needs to be restarted after the safety condition has been rectified. See the timing diagrams for proper pin timing.

Power-Down Functionality

During power-down mode $I_{BIASSET}$ and I_{MODSET} drop below 10µA, effectively shutting down the laser. FETG is not asserted and safety faults do not occur during this period. During power-down, I^2C communication is still active, but the signal conditioner pins EN1 and EN2 are noncontrollable and automatically change to the states: EN1 = 1 and EN2 = 0. Other internal flags/signals that are based on the signal conditioner inputs still reflect the status on the signal conditioner pins during power-down. For example, RX-LOS still reflects the status of SC-RX-LOS, and MOD-NR still reflects the logical states for the signal conditioner pins. Similarly, it is possible for FETG to be asserted, even though the BIASSET and MODSET currents are shut down. However, during power-down and a short period, $t_{PDR-OFF}$, during power-up, TX-P Low flag is ignored (internally automatically masked out) and does not contribute to FETG's logic.

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During an asserted period of P-DOWN/RST (DS1862A in power-down), and V_{CC3} is cycled, the DS1862A remains in power-down mode upon power-up. While in power-down mode the $\overline{\text{INTERRUPT}}$ pin does not assert. Once V_{CC3} has returned, the reset done flag asserts after the interrupt assert delay, t_{INIT_ON}.

Reset Functionality

Besides powering down the DS1862A, the P-DOWN/RST pin also functions to reset the DS1862A. After a high-going pulse of time t_{RESET}, several events occur within the DS1862A. First, MODSET and BIASSET currents shut down and are then reinstated. Second, between the rising edge of the reset pulse and the assertion of the reset-done flag (t_{INIT}), the low TX-P flag is ignored and does not cause FETG to trip. After time t_{INIT}, the low TX-P flag becomes functional. Also, at this time, the reset-done flag is asserted, causing an interrupt to be generated. If there are no faults before t_{INIT}, then no interrupts are asserted on the $\overline{\text{INTERRUPT}}$ pin.

If V_{CC3} is powered up while P-DOWN/RST is high, then the reset-done flag must be cleared twice. The first time the reset-done flag is generated by V_{CC3} powering up, the second time reset-done is generated by a falling edge on P-DOWN/RST. If V_{CC3} is continuously powered while P-DOWN/RST is low then only one reset-done flag needs to be cleared. See the timing diagrams for graphical detail.

Memory Map

Memory Organization

The DS1862A features six separate memory tables that are internally organized into 4-word rows. The Lower Memory is addressed from 00h to 7Fh and contains alarm and warning thresholds, flags, masks, several control registers, password entry area (PE), and the table select byte. Table 01h primarily contains user EEPROM as well as several control bytes for various functions. Table 02h is strictly user EEPROM that is protected by a host password. Table 03h is strictly used for controlling the extinction ratio with an LUT. Table 04h is a multifunction space that contains internal calibration values for monitored channels, LUT index pointers, and miscellaneous control bytes. Table 05h is factory programmed and stores SCALE values for use with suggested external temperature sensors. Also, one byte in Table 05h controls the THRSET voltage source and is completely accessible without any password protection. See the *Detailed Register Description* section for a more complete detail of each byte's function, as well as Table 11 for read/write permissions for each byte. Many nonvolatile memory locations are actually SRAM-shadowed EEPROM, which are controlled by the SEEB bit in Table 04h, Byte B2h.

The DS1862A incorporates SRAM-shadowed EEPROM memory locations for key memory addresses that may be rewritten many times. By default the shadowed-EEPROM bit, SEEB, is not set and these locations act as ordinary EEPROM. By setting SEEB, these locations begin to function like SRAM cells, which allow an infinite number of write cycles without concern of wearing out the EEPROM. This also eliminates the requirement for the EEPROM write time, t_{WR}. Because changes made with SEEB enabled do not affect the EEPROM, these changes are not retained through power cycles. The power-up value is the last value written with SEEB disabled. This function can be used to limit the number of EEPROM writes during calibration or to change the monitor thresholds periodically during normal operation helping to reduce the number of times EEPROM is written. The following information describes which locations are shadowed-EEPROM.

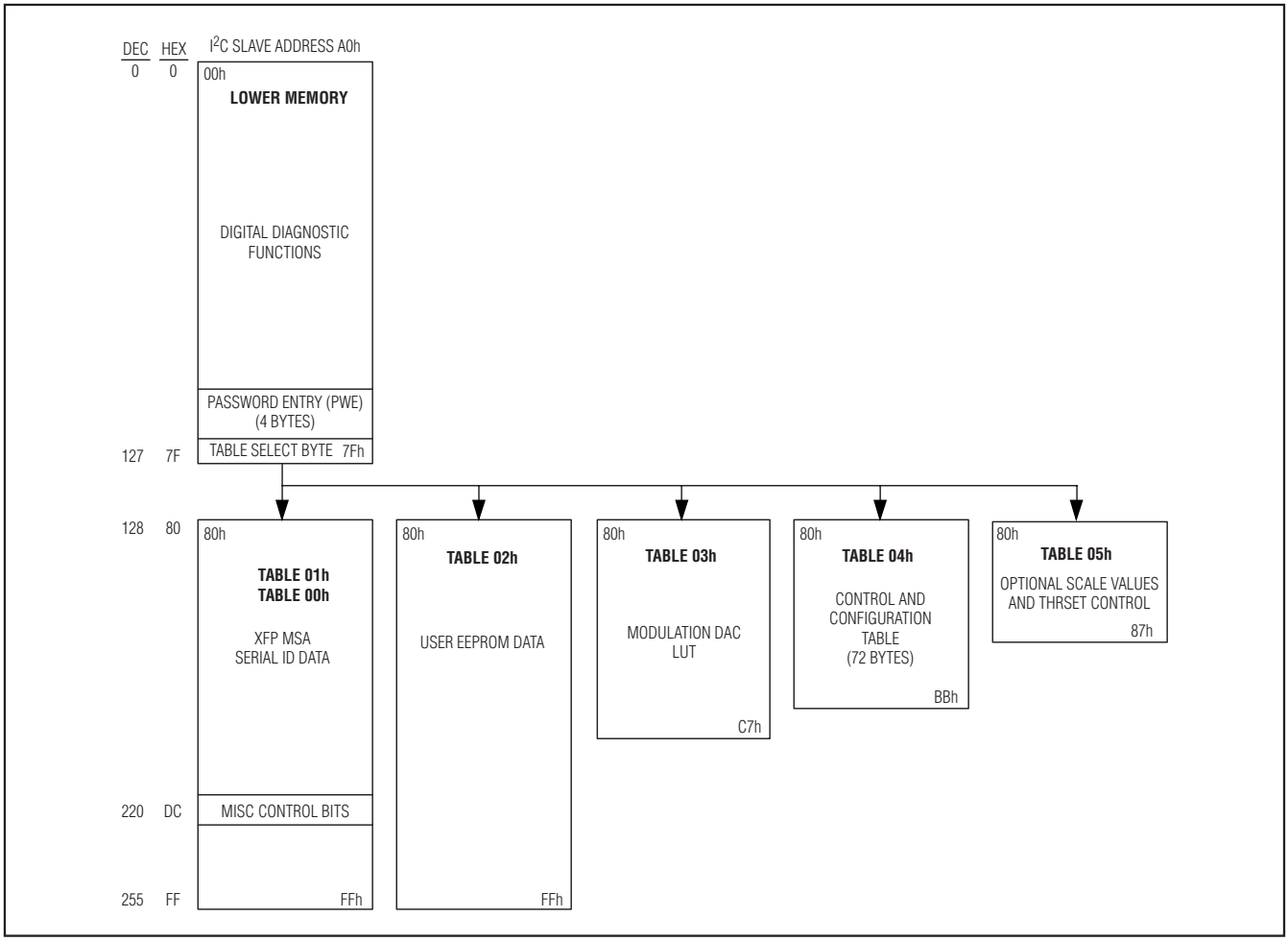

Figure 13. General View of DS1862A Memory Organization

Register Map

Table 11. Permission Table

PERMISSION	READ	WRITE
<0>	At least one byte in this row is different than the rest of the bytes, so look at each byte separately for permissions.	
<1>	ALL	ALL
<2>	ALL	MODULE
<3>	ALL	HOST
<4>	MODULE	MODULE
<5>	ALL	FACTORY
<6>	NEVER	HOST
<7>	NEVER	MODULE

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LOWER MEMORY (00h–7Fh)								
ADDRESS (hex)	WORD 0		WORD 1		WORD 2		WORD 3	
	BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
00<0,2>	USER EE	Signal Cond*	Temp Alarm Hi		Temp Alarm Lo		Temp Warn Hi	
08<2>	Temp Warn Lo		V_{CC3} Alarm Hi**		V_{CC3} Alarm Lo**		V_{CC3} Warn Hi**	
10<2>	V_{CC3} Warn Lo**		Bias Alarm Hi		Bias Alarm Lo		Bias Warn Hi	
18<2>	Bias Warn Lo		TX-P Alarm Hi		TX-P Alarm Lo		TX-P Warn Hi	
20<2>	TX-P Warn Lo		RX-P Alarm Hi		RX-P Alarm Lo		RX-P Warn Hi	
28<2>	RX-P Warn Lo		AUX1 Alarm Hi		AUX1 Alarm Lo		AUX1 Warn Hi	
30<2>	AUX1 Warn Lo		AUX2 Alarm Hi		AUX2 Alarm Lo		AUX2 Warn Hi	
38<0,2>	AUX2 Warn Lo		USER EE	USER EE	*Reserved*	*Reserved*	*Reserved*	*Reserved*
40<1>	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	USER SRAM	USER SRAM
48<1>	USER SRAM	USER SRAM	USER SRAM	USER SRAM	USER SRAM	USER SRAM	USER SRAM	USER SRAM
50<1>	Temp/Res/Bias/ TxP Alarm	RxP/AUX1/AUX2/ Res Alarm	Temp/Res/Bias/ TxP Warn	RxP/AUX1/ AUX2/Res Warn	Tx/Rx Misc Flags	Apd/Tec/ Wave/Res Flags	$V_{CC5/3/2}$/Vee Alarm Flags	$V_{CC5/3/2}$/Vee Warn Flags
58<1>	Temp/Res/Bias/ TxP Mask	RxP/AUX1/AUX2/ Res Mask	Temp/Res/Bias/ TxP Mask	RxP/AUX1/ AUX2/Res Mask	Rx/Rx Misc Mask	Apd/Tec/Wave/ Res Mask	$V_{CC5/3/2}$/Vee Alarm Mask	$V_{CC5/3/2}$/Vee Warn Mask
60<1>	Temp Value		$V_{CC2/3}$ Value**		Bias Value		TX-P Value	
68<1>	RX-P Value		AUX1 Value		AUX2 Value		GCS1	GCS0
70<0,1>	*Reserved*	*Reserved*	*Reserved*	*Reserved*	POA	*Reserved*	PEC_EN	Host PW
78<0,1>	Host PW	Host PW	Host PW	PWE (MSB)		PWE (LSB)		Table Select

EXPANDED BYTES

BYTE (hex)	BYTE/WORD NAME	Bit7		Bit6*		Bit5		Bit4		Bit3		Bit2		Bit1		Bit0	
		bit_{15}	bit_{14}	bit_{13}	bit_{12}	bit_{11}	bit_{10}	bit_9	bit_8	bit_7	bit_6	bit_5	bit_4	bit_3	bit_2	bit_1	bit_0
01	Signal Cond<1>*	USER EE		USER EE		USER EE		USER EE		USER EE		EN2 Value		EN1 Value		Lock-T1-221	
50	<1>	L-HI-TEMP-AL		L-LO-TEMP-AL		*Reserved*		*Reserved*		L-HI-BIAS-AL		L-LO-BIAS-AL		L-HI-TX-P-AL		L-LO-TX-P-AL	
51	<1>	L-HI-RX-P-AL		L-LO-RX-P-AL		L-HI-AUX1-AL		L-LO-AUX1-AL		L-HI-AUX2-AL		L-LO-AUX2-AL		*Reserved*		*Reserved*	
52	<1>	L-HI-TEMP-W		L-LO-TEMP-W		*Reserved*		*Reserved*		L-HI-BIAS-W		L-LO-BIAS-W		L-HI-TX-P-W		L-LO-TX-P-W	
53	<1>	L-HI-RX-P-W		L-LO-RX-P-W		L-HI-AUX1-W		L-LO-AUX1-W		L-HI-AUX2-W		L-LO-AUX2-W		*Reserved*		*Reserved*	
54	<1>	L-TX-NR		L-TX-F		L-TX-CDR-NL		L-RX-NR		L-RX-LOS		L-RX-CDR-NL		L-MOD-NR		L-RESET-DONE	
55	<1>	L-APD-SUP-F		L-TEC-F		L-WAVE-NL		*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*	
56	<1>	L-HI-V_{CC5}-AL		L-LO–V_{CC5}-AL		L-HI-V_{CC3}-AL		L-LO–V_{CC3}-AL		L-HI-V_{CC2}-AL		L-LO–V_{CC2}-AL		L-HI-V_{EE5}-AL		L-LO-V_{EE5}-AL	

**Bit 0 of Address 01h can be written only if bit 0 of Byte DDh in Table 01h is set.*

***$V_{CC2/3}$ are in reserved locations.*

EXPANDED BYTES (CONTINUED)															
BYTE (hex)	BYTE/WORD NAME	Bit7		Bit6		Bit5		Bit4		Bit3		Bit2		Bit1		Bit0	
		bit_{15}	bit_{14}	bit_{13}	bit_{12}	bit_{11}	bit_{10}	bit_{9}	bit_{8}	bit_{7}	bit_{6}	bit_{5}	bit_{4}	bit_{3}	bit_{2}	bit_{1}	bit_{0}
57	<1>	L-HI-V_{CC5}-W		L-LO-V_{CC5}-W		L-HI-V_{CC3}-W		L-LO-V_{CC3}-W		L-HI-V_{CC2}-W		L-LO-V_{CC2}-W		L-HI-V_{EE5}-W		L-LO-V_{EE5}-W	
58	<1>	HI-TEMP-AL MASK		LO-TEMP-AL MASK		*Reserved*		*Reserved*		HI-BIAS-AL MASK		LO-BIAS-AL MASK		HI-TX-P-AL MASK		LO-TX-P-AL MASK	
59	<1>	HI-RX-P-AL MASK		LO-RX-P-AL MASK		HI-AUX1-AL MASK		LO-AUX1-AL MASK		HI-AUX2-AL MASK		LO-AUX2-AL MASK		*Reserved*		*Reserved*	
5A	<1>	HI-TEMP-W MASK		LO-TEMP-W MASK		*Reserved*		*Reserved*		HI-BIAS-W MASK		LO-BIAS-W MASK		HI-TX-P-W MASK		LO-TX-P-W MASK	
5B	<1>	HI-RX-P-W MASK		LO-RX-P-W MASK		HI-AUX1-W MASK		LO-AUX1-W MASK		HI-AUX2-W MASK		LO-AUX2-W MASK		*Reserved*		*Reserved*	
5C	<1>	TX-NR MASK		TX-F MASK		TX-CDR-NL MASK		RX-NR MASK		RX-LOL MASK		RX-CDR-NL MASK		MOD-NR MASK		RESET-DONE MASK	
5D	<1>	APD-SUP-F MASK		TEC-F MASK		WAVE-NL MASK		*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*	
5E	<1>	HI-V_{CC5}-AL MASK		LO-V_{CC5}-AL MASK		HI-V_{CC3}-AL MASK		LO-V_{CC3}-AL MASK		HI-V_{CC2}-AL MASK		LO-V_{CC2}-AL MASK		HI-V_{EE5}-AL MASK		LO-V_{EE5}-AL MASK	
5F	<1>	HI-V_{CC5}-W MASK		LO-V_{CC5}-W MASK		HI-V_{CC3}-W MASK		LO-V_{CC3}-W MASK		HI-V_{CC2}-W MASK		LO-V_{CC2}-W MASK		HI-V_{EE5}-W MASK		LO-V_{EE5}-W MASK	
6E	<1>	TX-D		SOFT TX-D†		MOD-NR		P-DOWN/RST		SOFT P-DOWN/RST†		$\overline{\text{INTERRUPT}}$		RX-LOS		DATA-NR	
6F	<1>	TX-NR		TX-F		*Reserved*		RX-NR		RX-CDR-NL		*Reserved*		*Reserved*		*Reserved*	
74	POA <1>	POA		*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*	
77	Host PW<6>	2^{31}		2^{30}		2^{29}		2^{28}		2^{27}		2^{26}		2^{25}		2^{24}	
78	Host PW<6>	2^{23}		2^{22}		2^{21}		2^{20}		2^{19}		2^{18}		2^{17}		2^{16}	
79	Host PW<6>	2^{15}		2^{14}		2^{13}		2^{12}		2^{11}		2^{10}		2^{9}		2^{8}	
7A	Host PW<6>	2^{7}		2^{6}		2^{5}		2^{4}		2^{3}		2^{2}		2^{1}		2^{0}	
7B	PWE<6>	2^{31}		2^{30}		2^{29}		2^{28}		2^{27}		2^{26}		2^{25}		2^{24}	
7C	PWE<6>	2^{23}		2^{22}		2^{21}		2^{20}		2^{19}		2^{18}		2^{17}		2^{16}	
7D	PWE<6>	2^{15}		2^{14}		2^{13}		2^{12}		2^{11}		2^{10}		2^{9}		2^{8}	
7E	PWE<6>	2^{7}		2^{6}		2^{5}		2^{4}		2^{3}		2^{2}		2^{1}		2^{0}	
7F	Table Select<1>	2^{7}		2^{6}		2^{5}		2^{4}		2^{3}		2^{2}		2^{1}		2^{0}	

†Bit 6 and Bit 3 of Byte 6Eh are masked by Bit 6 and Bit 5 of Byte DDh in Table 01h, respectively.

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TABLE 01h (SERIAL ID MEMORY)								
ADDRESS (hex)	WORD 0		WORD 1		WORD 2		WORD 3	
	Byte 0/8	Byte 1/9	Byte 2/A	Byte 3/B	Byte 4/C	Byte 5/D	Byte 6/E	Byte 7/F
80<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
88<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
90<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
98<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
A0<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
A8<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
B0<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
B8<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
C0<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
C8<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
D0<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
D8<2>	USER EE	USER EE	USER EE	USER EE	$V_{CC2/3}$_SEL	LO MEM 6Eh EN	AUX1/2 UNIT SEL	USER EE
E0<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
E8<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
F0<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE
F8<2>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE

EXPANDED BYTES															
BYTE (hex)	BYTE/WORD NAME	Bit7		Bit6		Bit5		Bit4		Bit3		Bit2		Bit1		Bit0	
		bit_{15}	bit_{14}	bit_{13}	bit_{12}	bit_{11}	bit_{10}	bit_9	bit_8	bit_7	bit_6	bit_5	bit_4	bit_3	bit_2	bit_1	bit_0
	USER EE	USER EE		USER EE		USER EE		USER EE		USER EE		USER EE		USER EE		USER EE	
DC<2>	$V_{CC2/3}$_SEL	*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		$V_{CC2/3}$_SEL	
DD<2>	LO MEM 6Eh EN	*Reserved*		Enable 6Eh, bit 6		Enable 6Eh, bit 3		*Reserved*		*Reserved*		*Reserved*		*Reserved*		Lock-Bit	
DE<2>	AUX1/2 UNIT SEL	AUX1-SEL 2^3		AUX1-SEL 2^2		AUX1-SEL 2^1		AUX1-SEL 2^0		AUX2-SEL 2^3		AUX2-SEL 2^2		AUX2-SEL 2^1		AUX2-SEL 2^0	

Note: *Byte DDh<6:5> of Table 01h enables bit 6 and bit 3 of Byte 6Eh in the lower memory.*

TABLE 02h (HOST USER MEMORY)								
ADDRESS (hex)	WORD 0		WORD 1		WORD 2		WORD 3	
	Byte 0/8	Byte 1/9	Byte 2/A	Byte 3/B	Byte 4/C	Byte 5/D	Byte 6/E	Byte 7/F
80–FF<3>	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE	USER EE

TABLE 03h (MODSET LOOKUP TABLE)								
ADDRESS (hex)	WORD 0		WORD 1		WORD 2		WORD 3	
	Byte 0/8	Byte 1/9	Byte 2/A	Byte 3/B	Byte 4/C	Byte 5/D	Byte 6/E	Byte 7/F
80–87<4>	USER EE, < -40°C	USER EE, -40°C	USER EE, -38°C	USER EE, -36°C	USER EE, -34°C	USER EE, -32°C	USER EE, -30°C	USER EE, -28°C
88–BF<4>	—	—	—	—	—	—	—	—
C0–C7<4>	USER EE, +88°C	USER EE, +90°C	USER EE, +92°C	USER EE, +94°C	USER EE, +96°C	USER EE, +98°C	USER EE, +100°C	USER EE, > +102°C

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TABLE 04h (CONTROL AND CONFIG) (80h–BBh)

ADDRESS (hex)	WORD 0		WORD 1		WORD 2		WORD 3	
	Byte 0/8	Byte 1/9	Byte 2/A	Byte 3/B	Byte 4/C	Byte 5/D	Byte 6/E	Byte 7/F
80<4>	*Reserved*	BIAS SHIFT, TX-P SHIFT	RX-P SHIFT, AUX1 SHIFT	AUX2 SHIFT, *Reserved*	APC REF COARSE	APC REF FINE	LUT RANGE	Control Register 1
88<4>	QT TX-P HI	QT TX-P LO	QT HIGH BIAS	Control Register 2	*Reserved*	*Reserved*	*Reserved*	*Reserved*
90<4>	*Reserved*	*Reserved*	MSB $V_{CC2/3}$ SCALE	LSB $V_{CC2/3}$ SCALE	MSB BIAS SCALE	LSB BIAS SCALE	MSB TX-P SCALE	LSB TX-P SCALE
98<4>	MSB RX-P SCALE	LSB RX-P SCALE	MSB AUX1 SCALE	LSB AUX1 SCALE	MSB AUX2 SCALE	LSB AUX2 SCALE	*Reserved*	*Reserved*
A0<4>	MSB TEMP OFFSET	LSB TEMP OFFSET	MSB $V_{CC2/3}$ OFFSET	LSB $V_{CC2/3}$ OFFSET	MSB BIAS OFFSET	LSB BIAS OFFSET	MSB TX-P OFFSET	LSB TX-P OFFSET
A8<4>	MSB RX-P OFFSET	LSB RX-P OFFSET	MSB AUX1 OFFSET	LSB AUX1 OFFSET	MSB AUX2 OFFSET	LSB AUX2 OFFSET	*Reserved*	*Reserved*
B0<4>	LUT INDEX POINTER	LUT VALUE	LUT_CONF	*Reserved*	DAC STATUS	*Reserved*	*Reserved*	*Reserved*
B8<7>	MOD_PW_CHNG	MOD_PW_CHNG	MOD_PW_CHNG	MOD_PW_CHNG				

EXPANDED BYTES

BYTE (hex)	BYTE WORD NAME	Bit7		Bit6		Bit5		Bit4		Bit3		Bit2		Bit1		Bit0	
		bit_{15}	bit_{14}	bit_{13}	bit_{12}	bit_{11}	bit_{10}	bit_9	bit_8	bit_7	bit_6	bit_5	bit_4	bit_3	bit_2	bit_1	bit_0
81	<4>	BIAS SHIFT 2^3		BIAS SHIFT 2^2		BIAS SHIFT 2^1		BIAS SHIFT 2^0		TX-P SHIFT 2^3		TX-P SHIFT 2^2		TX-P SHIFT 2^1		TX-P SHIFT 2^0	
82	<4>	RX-P SHIFT 2^3		RX-P SHIFT 2^2		RX-P SHIFT 2^1		RX-P SHIFT 2^0		AUX1 SHIFT 2^3		AUX1 SHIFT 2^2		AUX1 SHIFT 2^1		AUX1 SHIFT 2^0	
83	<4>	AUX2 SHIFT 2^3		AUX2 SHIFT 2^2		AUX2 SHIFT 2^1		AUX2 SHIFT 2^0		*Reserved*		*Reserved*		*Reserved*		*Reserved*	
84	<4>	APC 2^9		APC 2^8		APC 2^7		APC 2^6		APC 2^5		APC 2^4		APC 2^3		APC 2^2	
85	<4>	*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		APC 2^1		APC 2^0	
86	<4>	*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		LUT RANGE 2^2		LUT RANGE 2^1		LUT RANGE 2^0	
87	<4>	FETG_POL		QT TX-P HI Mask		QT HIGH BIAS Mask		QT TX-P LO Mask		*Reserved*		*Reserved*		SRC_SINK_B		*Reserved*	
8B	<4>	*Reserved*		*Reserved*		*Reserve_EN*		TEMP_INT/EXT		*Reserved*		*Reserved*		*Reserved*		*Reserved*	
B2	LUT_CONF<4>	*Reserved*		*Reserved*		*Reserved*		*Reserved*		*Reserved*		SEEB		TEN		AEN	
B4	DAC STATUS <4>	SAFETY Flag		SHUTDOWN Flag		*Reserved*		QT LOW TX-P Flag		QT HIGH TX-P Flag		QT HIGH BIAS Flag		*Reserved*		*Reserved*	
B8	Module PW<7>	2^{31}		2^{30}		2^{29}		2^{28}		2^{27}		2^{26}		2^{25}		2^{24}	
B9	Module PW<7>	2^{23}		2^{22}		2^{21}		2^{20}		2^{19}		2^{18}		2^{17}		2^{16}	
BA	Module PW<7>	2^{15}		2^{14}		2^{13}		2^{12}		2^{11}		2^{10}		2^9		2^8	
BB	Module PW<7>	2^7		2^6		2^5		2^4		2^3		2^2		2^1		2^0	

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TABLE 05h (OPTIONAL OFFSETS AND THRSET)																	
ADDRESS (hex)	WORD 0				WORD 1				WORD 2				WORD 3				
	Byte 0/8		Byte 1/9		Byte 2/A		Byte 3/B		Byte 4/C		Byte 5/D		Byte 6/E		Byte 7/F		
80–87	DS60 SCALE				LM50 SCALE				*Reserved*		*Reserved*		*Reserved*		V_{THRSET_VALUE} <1>		
EXPANDED BYTES																	
BYTE (hex)	BYTE/WORD NAME	Bit7		Bit6		Bit5		Bit4		Bit3		Bit2		Bit1		Bit0	
		bit_{15}	bit_{14}	bit_{13}	bit_{12}	bit_{11}	bit_{10}	bit_9	bit_8	bit_7	bit_6	bit_5	bit_4	bit_3	bit_2	bit_1	bit_0
80	DS60 SCALE <5>	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
82	LM50 SCALE <5>	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
87	V_{THRSET_VALUE}	2^7		2^6		2^5		2^4		2^3		2^2		2^1		2^0	

Detailed Register Description

Conventions

Name of Row

- *Name of Byte* .....<Read/Write><Volatile><Power-On Value>
- *Name of Byte* .....<Read/Write><Nonvolatile><Factory-Default Setting>
- *Name of Byte* .....<Read/Write><Shadowed Nonvolatile><Factory-Default Setting>
- *Name of Byte* .....<Read/Write><Status><Power-On Value>

Lower Memory

00h

- *USER EE* .....<R-all/W-all><Shadowed Nonvolatile><00>

01h

- *Signal Condition*.....<R-all/W-all><Volatile><00> Bit 0 can only be written if Table 01h, Byte DDh, bit <0> is high. Bits <2:1> control EN2 and EN1, respectively.

02h → 39h

- *Alarms and Warnings* .....<R-all/W-Module><Shadowed Nonvolatile><Note*> These registers set the 16-bit threshold level for corresponding monitor channels. *Note: High alarm and warnings factory default to FFFFh, and low alarm shut warnings default to 0000h.

3Ah, 3Bh

- *USER EE* .....<R-all/W-all><Shadowed Nonvolatile><00>

46h → 4Fh

- *USER SRAM*.....<R-all/W-all><Volatile><00>

50h → 57h

- *Latched Flags* .....<R-all/clear-all><Volatile><00> These are latched flags for corresponding signals. Any flag is cleared by simply reading it.

58h → 5Fh

- *Masks*.....<R-all/W-all><Volatile><00> These mask bits internally block the signals that drive the $\overline{\text{INTERRUPT}}$ pin. A low setting causes the corresponding monitor channel to drive the $\overline{\text{INTERRUPT}}$ pin.

60h → 6Dh

- *Monitor Values* .....<R-all/W-all><Volatile><xxxx> These registers are internally updated with the monitor channel's digital result. They can be read as left-justified 16-bit values.

6Eh

- *GCS1* .....<R-all/W-all><Volatile><xx> These are nonlatched flags, indicating the real-time digital state of a corresponding signal as well as control bits for particular functions.

Bit 0: DATA-NR. Bit is high until DS1862A has achieved power-up. Bit goes low, signaling that monitor channel data is ready to be read.

Bit 1: RX-LOS. Indicates optical loss of the signal and is updated within t_{LOS-ON}.

Bit 2: $\overline{\text{INTERRUPT}}$. Indicates the state of the $\overline{\text{INTERRUPT}}$ pin and is updated within t_{INIT_ON}.

Bit 3: SOFT P-DOWN/RST. Read/Write bit that places the DS1862A in power-down mode. Toggle to reset. Masked by Bit 5 of Byte DDh in Table 01h.

Bit 4: P-DOWN/RST. Indicates the digital state of the P-DOWN/RST pin and is updated within t_{PDR-ON}.

Bit 5: MOD-NR State. Indicates the state of MOD-NR pin and is updated within t_{PDR-ON}.

Bit 6: SOFT TX-D. Read/Write bit that disables (shuts down) $I_{BIASSET}$ and I_{MODSET}. Masked by Bit 6 of Byte DDh in Table 01h.

Bit 7: TX-D. Indicates the digital state of the TX-D pin and is updated within t_{OFF}.

6Fh

- *GCS0* ..... <R-all/W-all><Status><xx> These are nonlatched flags, indicating the real-time digital state of a corresponding signal.

Bit 0: Reserved.

Bit 1: Reserved.

Bit 2: Reserved.

Bit 3: RX-CDR-NL not locked. Indicates LOL in Rx path CDR.

Bit 4: RX-NR State. Indicates a NOT READY condition in the Rx path.

Bit 5: Reserved.

Bit 6: TX-F State. Indicates a laser safety fault condition.

Bit 7: TX-NR State. Indicates a NOT READY condition on the Tx path.

74h

- *POA*..... <R-all/W-all><Volatile><00> A high on bit 7 indicates that V_{CC3} is below the power-on analog trip point, POA.

76h

- *PEC_EN*..... <R-all/W-all><Volatile><00> Bit 0 is used to enable PEC. A value of 1 enables PEC.

77h → 7Ah

- *Host PW Change* ..... <R-never/W-Host><Shadowed Nonvolatile P><00> This is the 32-bit location that the DS1862A uses to compare with the PWE to grant host password access. A Read result is always <FFh>.

7Bh → 7Eh

- *PWE*..... <R-never/W-all><Volatile><00> This is the 32-bit location that is used to enter the host and module password to gain access to the DS1862A. A Read result is always <FFh>.

7Fh

- *Table Select*..... <R-all/W-all><Volatile><01> This is the 8-bit register that controls which section of upper memory (table) is being addressed by I^2C. A value of 00h and 01h results in addressing Table 01h. Values above 05h are accepted, but do not correspond to any physical memory.

Table 01h

80h → DBh

- *USER EE* ..... <R-all/W-Module><Nonvolatile><00>

DCh

- $V_{CC2/3}$*_SEL*..... <R-all/W-Module><Shadowed Nonvolatile><00> Bit 0 of this register controls whether V_{CC2} or V_{CC3} is internally measured by the $V_{CC2/3}$ monitor channel. A '1' selects V_{CC2} to be measured.

DDh

- *LO MEM 6Eh EN*.....<R-all/W-Module><Shadowed Nonvolatile><00> If bit 5 is high, then bit 3 of 6Eh is not masked. If bit 6 is high, then bit 6 of 6Eh is not masked. Bit 0 is the Lock_Bit. If set, Lower Memory address 01h, bit 0 is writable.

DEh

- *AUX1/2 UNIT SEL* .....<R-all/W-Module><Shadowed Nonvolatile><00> These two 4-bit values define what is being measured on AUX1MON and AUX2MON. MSB is AUX1MON unit select and LSB is AUX2MON unit select. See Table 5 for more details.

DFh

- *USER EE* .....<R-all/W-Module><Shadowed Nonvolatile><00>

E0h → FFh

- *USER EE* .....<R-all/W-Module><Nonvolatile><00>

Table 02h

80h → FFh

- *USER EE* .....<R-all/W-Host><Nonvolatile><00>

Table 03h

80h →C7h

- *LUT* .....<R-Module/W-Module><Nonvolatile><00> These registers control the output current on MODSET as a function of temperature.

Table 04h

80h →B8h

81h

- *BIAS SHIFT* .....<R-Module/W-Module><Shadowed Nonvolatile><0> This 4-bit value in <7:4> defines how many right-shifts IBIASMON monitor channel receives. The MSB is bit 7.
- *TX-P SHIFT*.....<R-Module/W-Module><Shadowed Nonvolatile><0> This 4-bit value in <3:0> defines how many right-shifts TX-P (BMD) monitor channel receives. The MSB is bit 3.

82h

- *RX-P SHIFT* .....<R-Module/W-Module><Shadowed Nonvolatile><0> This 4-bit value in <7:4> defines how many right-shifts RX-P (RSSI) monitor channel receives. The MSB is bit 7.
- *AUX1 SHIFT*.....<R-Module/W-Module><Shadowed Nonvolatile><0> This 4-bit value in <3:0> defines how many right-shifts AUX1MON monitor channel receives. The MSB is bit 3.

83h

- *AUX2 SHIFT*.....<R-Module/W-Module><Shadowed Nonvolatile><0> This 4-bit value in <7:4> defines how many right-shifts AUX2MON monitor channel receives. The MSB is bit 7.

84h

- *APC REF COARSE*.....<R-Module/W-Module><Shadowed Nonvolatile><00> This 8-bit value sets the coarse APC current on BMD.

85h

- *APC REF FINE* ..... <R-Module/W-Module><Shadowed Nonvolatile><00> This 2-bit value in <1:0> sets the fine APC current on BMD. The MSB is bit 1.

86h

- *LUT RANGE* ..... <R-Module/W-Module><Shadowed Nonvolatile><00> This 3-bit register in <2:0> sets the current range on MODSET. The MSB is bit 2.

87h

- *Control Register 1* ..... <R-Module/W-Module><Shadowed Nonvolatile><00>

Bit 0: Reserved.

Bit 1: SRC_SINK_B. If set, then BMD sources current; otherwise, BMD sinks current.

Bit 2: Reserved.

Bit 3: Reserved.

Bit 4: QT TX-P LO Mask. If set, then TX-P low does not have the ability to cause a safety fault.

Bit 5: QT HIGH BIAS Mask. If set, then HIGH BIAS does not have the ability to cause a safety fault.

Bit 6: QT TX-P HI Mask. If set, then TX-P high does not have the ability to cause a safety fault.

Bit 7: FETG_POL. If set, then FETG asserts with a high logic level; otherwise, it asserts with a low logic level.

88h

- *QT TX-P HI* ..... <R-Module/W-Module><Shadowed Nonvolatile><FF> This is the TX-P quick-trip threshold setting that is used as a comparison to generate a TX-P high safety fault.

89h

- *QT TX-P LO* ..... <R-Module/W-Module><Shadowed Nonvolatile><00> This is the TX-P quick-trip threshold setting that is used as a comparison to generate a TX-P low safety fault.

8Ah

- *QT HIGH BIAS* ..... <R-Module/W-Module><Shadowed Nonvolatile><FF> This is the TX-P quick-trip threshold setting that is used as a comparison to generate a HIGH BIAS safety fault.

8Bh

- *Control Register 2* ..... <R-Module/W-Module><Shadowed Nonvolatile><00>

Bit 0: Reserved.

Bit 1: Reserved.

Bit 2: Reserved.

Bit 3: Reserved.

Bit 4: TEMP_INT/EXT. If set, then the LUT INDEX POINTER register is controlled by AUX2MON. Otherwise, the internal temperature sensor controls the LUT.

Bit 5: Reserve_EN. If set, then $V_{CC2/3}$ is actively updated in the monitor loop.

Bit 6: Reserved.

Bit 7: Reserved.

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92h

- $V_{CC2/3}$ *SCALE* ..... <R-Module/W-Module><Shadowed Nonvolatile><Factory Trimmed> This 16-bit register controls the scale value for the $V_{CC2/3}$ monitor channel.

94h

- *BIAS SCALE*..... <R-Module/W-Module><Shadowed Nonvolatile><Factory Trimmed> This 16-bit register controls the scale value for the BIAS monitor channel.

96h

- *TX-P SCALE*..... <R-Module/W-Module><Shadowed Nonvolatile><Factory Trimmed> This 16-bit register controls the scale value for the TX-P (BMD) monitor channel.

98h

- *RX-P SCALE*..... <R-Module/W-Module><Shadowed Nonvolatile><Factory Trimmed> This 16-bit register controls the scale value for the RX-P (RSSI) monitor channel.

9Ah

- *AUX1 SCALE* ..... <R-Module/W-Module><Shadowed Nonvolatile><Factory Trimmed> This 16-bit register controls the scale value for the AUX1MON monitor channel.

9Ch

- *AUX2 SCALE* ..... <R-Module/W-Module><Shadowed Nonvolatile><Factory Trimmed> This 16-bit register controls the scale value for the AUX2MON monitor channel.

A0h

- *TEMP OFFSET* ..... <R-Module/W-Module><Shadowed Nonvolatile><Factory Trimmed> This 16-bit register controls the offset value for the internal temperature monitor channel.

A2h

- $V_{CC2/3}$ *OFFSET*..... <R-Module/W-Module><Shadowed Nonvolatile><0000> This 16-bit register controls the offset value for the $V_{CC2/3}$ monitor channel.

A4h

- *BIAS OFFSET*..... <R-Module/W-Module><Shadowed Nonvolatile><0000> This 16-bit register controls the offset value for the BIAS monitor channel.

A6h

- *TX-P OFFSET* ..... <R-Module/W-Module><Shadowed Nonvolatile><0000> This 16-bit register controls the offset value for the TX-P (BMD) monitor channel.

A8h

- *RX-P OFFSET*..... <R-Module/W-Module><Shadowed Nonvolatile><0000> This 16-bit register controls the offset value for the RX-P (RSSI) monitor channel.

AAh

- *AUX1 OFFSET*..... <R-Module/W-Module><Shadowed Nonvolatile><0000> This 16-bit register controls the offset value for the AUX1MON monitor channel.

ACh

- *AUX2 OFFSET*..... <R-Module/W-Module><Shadowed Nonvolatile><0000> This 16-bit register controls the offset value for the AUX2MON monitor channel.

B0h

- *LUT INDEX POINTER*..... <R-Module/W-Module><Volatile><xx> This register controls the index pointer value for the LUT. It is automatically updated (in normal operating mode) and can be read or overwritten using the TEN and AEN bits.

B1h

- *LUT VALUE*.....<R-Module/W-Module><Shadowed Nonvolatile><00> This register contains the fetched LUT value that drives the MODSET current. It can be read or overwritten to directly control the MODSET current (manual mode).

B2h

- *LUT_CONF*.....<R-Module/W-Module><Shadowed Nonvolatile><03>

Bit 0: AEN. A high on AEN enables data placed in the LUT VALUE register to drive MODSET.

Bit 1: TEN. A high on TEN enables the LUT INDEX POINTER to fetch data from the LUT.

Bit 2: SEEB. A high on SEEB disables EEPROM writes of Shadowed EEPROM locations.

Bit 3: Reserved.

Bit 4: Reserved.

Bit 5: Reserved.

Bit 6: Reserved.

Bit 7: Reserved.

B4h

- *DAC STATUS*.....<R-Module/W-Module><Status><xx0xxx00b>

Bit 0: Reserved.

Bit 1: Reserved.

Bit 2: QT HIGH BIAS Flag. This flag indicates that the current entering BIASSET is above the threshold.

Bit 3: QT HIGH TX-P Flag. This flag indicates that TX-P is above the threshold.

Bit 4: QT LOW TX-P Flag. This flag indicates that TX-P is below the threshold.

Bit 5: Reserved.

Bit 6: SHUTDOWN Flag. A high indicates that the DS1862A is in shutdown mode and that FETG is asserted.

Bit 7: SAFETY Flag. A high indicates that a safety fault (quick trip) has occurred.

B8h

- *MOD_PW_CHNG*.....<R-never/W-Module><Shadowed Nonvolatile><00h> This is the 32-bit location that the DS1862A uses to compare with the PWE to grant module password access. A Read result is always <FFh>.

Table 05h

80h

- *DS60 SCALE*.....<R-all/W-Factory><Nonvolatile><Factory Trimmed> This unique 16-bit value sets the SCALE register for use with a DS60 temperature sensor on AUX2MON.

82h

- *LM50 SCALE*.....<R-all/W-Factory><Nonvolatile><Factory Trimmed> This unique 16-bit value sets the SCALE register for use with a LM50 temperature sensor on AUX2MON.

87h

- V_{THRSET_VALUE}.....<R-all/W-all><Shadowed Nonvolatile><80> This 8-bit value sets the voltage on the signal conditioner voltage source, THRSET.

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Security/Password Protection

The DS1862A features two separate and independent 32-bit passwords for important memory locations. The host password and the module password allow their own allocated memory locations to be locked to prevent write and/or read access. To enhance the security of the DS1862A, the password entry and setting bytes can never be read.

To gain access to host-protected or module-protected memory locations, the correct 32-bit value must be entered into the password entry bytes (PWE) in either a single 4-byte write, or 4 single-byte writes. To reprogram either password, simply enter the appropriate current password to gain memory access, write the new Host or module PW with one 4-byte write, and finally re-enter the new password into the PWE to regain memory access.

Power-Up Sequence

The DS1862A does require a particular power-up sequence to ensure proper functionality. V_{CC3} should always be applied first or at the same time as V_{CC2}. If this power-up sequence is not followed, then current can be sourced out of V_{CC2} as if it was connected to V_{CC3} with a resistor internal to the DS1862A. If V_{CC2} is not used then it should be externally connected to V_{CC3}.

Signal Conditioners—EN1 and EN2 and THRSET

Signal Conditioners—EN1 and EN2

The EN1 and EN2 output pins are controlled by the bits at address 01h, bits 2 and 1. The logic state of the pins is directly analogous to the logical state of the register. EN1 and EN2 automatically change to a high and low state, respectively, during power-down mode as described in the *Power-Down Functionality* section.

Signal Conditioners—THRSET

A programmable voltage source, THRSET, is also provided for use with signal conditioners. This source is programmable from 0 to 1V in 256 increments.

I²C and Packet Error Checking (PEC) Information

The DS1862A supports I²C data transfers as well as data transfers with PEC. The slave address is unalterable and is set to A0h. The DS1862A, however, does have an additional dedicated pin, MOD-DESEL, which acts as an active-low chip select to enable communication. See the *I²C Serial Interface* and the *I²C Operation Using Packet Error Checking* sections for details.

Precision SCALE Register Settings for AUX2MON

The DS1862A features a factory-trimmed SCALE value for use with DS60 or LM50 temperature sensors. If external temperature measurement on AUX2MON is used with one of these two sensors, the 16-bit SCALE value can be read from Table 05h and written into the SCALE register in Table 04h, Byte 9Ch and 9Dh. This option allows for the most precise setting for SCALE without requiring additional trimming. Since the SCALE register value is precisely trimmed at the factory, the OFFSET register will always be a nonunique value and can simply be written into the OFFSET register. For the DS60, the value of EF0Ah in OFFSET completes the internal calibration. For the LM50, the value of F380h in OFFSET completes the internal calibration.

I²C Serial Interface

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave devices: Slave devices send and receive data at the master's request.

Bus idle or not busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 14 for applicable timing.

STOP condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 14 for applicable timing.

REPEATED START condition: The master can use a REPEATED START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. REPEATED STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A REPEATED START condition is issued identically to a normal START condition. See Figure 14 for applicable timing.

Bit write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (Figure 14). Data is shifted into the device during the rising edge of the SCL.

Bit read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (Figure 14) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 14) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave address byte: Each slave on the I²C bus responds to a slave addressing byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS1862A's slave address is 1010000Xb. The MOD-DESEL pin is used as a chip select, and allows the device to respond or ignore I²C communication that has A0h as the device address. By writing the correct slave address with R/$\overline{W}$ = 0, the master indicates it will write data to the slave. If R/$\overline{W}$ = 1, the master will read data from the slave. If an incorrect slave address is written, the DS1862A assumes the master is communicating with another I²C device and ignores the communications until the next START condition is sent.

Memory address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data.

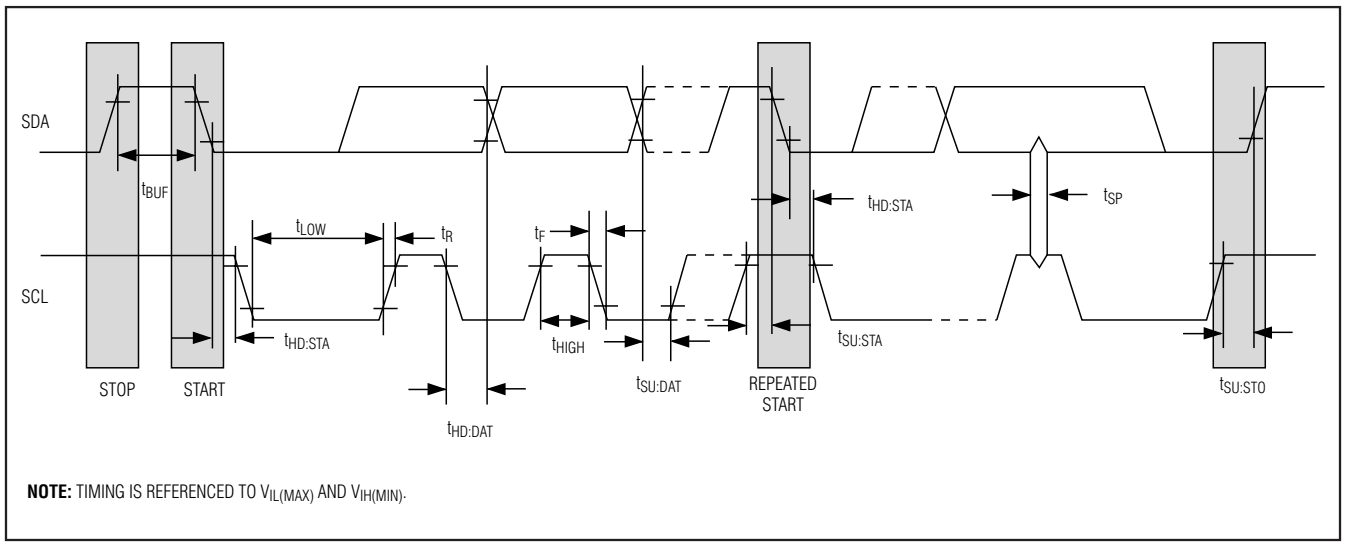

Figure 14. I²C Timing Diagram

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The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

Writing a single byte to a slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgement during all byte write operations.

Writing multiple bytes to a slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 4 data bytes, and generates a STOP condition.

The DS1862A is capable of writing 1 to 4 bytes (referred to as one row or page) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one row of the memory map. Attempts to write to additional memory rows without sending a STOP condition between rows results in the address counter wrapping around to the beginning address of the present row.

To prevent address wrapping from occurring, the master must send a STOP condition at the end of the row, and then wait for the bus free or EEPROM write time to elapse. Then the master can generate a new START condition, and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge polling: Any time EEPROM is written, the DS1862A requires the EEPROM write time (t_W) after the STOP condition to write the contents of the row to EEPROM. During the EEPROM write time, the DS1862A does not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the DS1862A, which allows the next row to be written as soon as the DS1862A is ready to receive the data. The alternative to acknowledge polling is to wait for the maximum period of t_W to elapse before attempting to write again to the DS1862A.

EEPROM write cycles: When EEPROM writes occur, the DS1862A writes the whole EEPROM memory 4-byte row even if only a single byte on the row was modified. Writes that do not modify all 4 bytes on the row are allowed and do not corrupt the remaining bytes of memory on the same row. Because the whole row is written, bytes on the row that were not modified during the transaction are still subject to a write cycle. This can result in a whole row being worn out over time by writing a single byte repeatedly. Writing a row one byte at a time wears out the EEPROM four times faster than writing the entire row at once. The DS1862A's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table.

Reading a single byte from a slave: Unlike the write operation that uses the memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave at the location currently in the address counter, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

Manipulating the address counter for reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a REPEATED START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

See Figure 15 for a read example using the REPEATED START condition to specify the starting memory location.

Reading multiple bytes from a slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it NACKs to indicate the end of the transfer and generates a STOP condition. This can be done with or without modifying the address counter's location before the read cycle. If the address counter reaches the last physical address, the internal index pointer loops back to the first memory location in a given memory table. For example, if address FFh in Table 02h is read, the next byte of data to be returned to the master is address 80h in Table 02h, not 00h in lower memory.

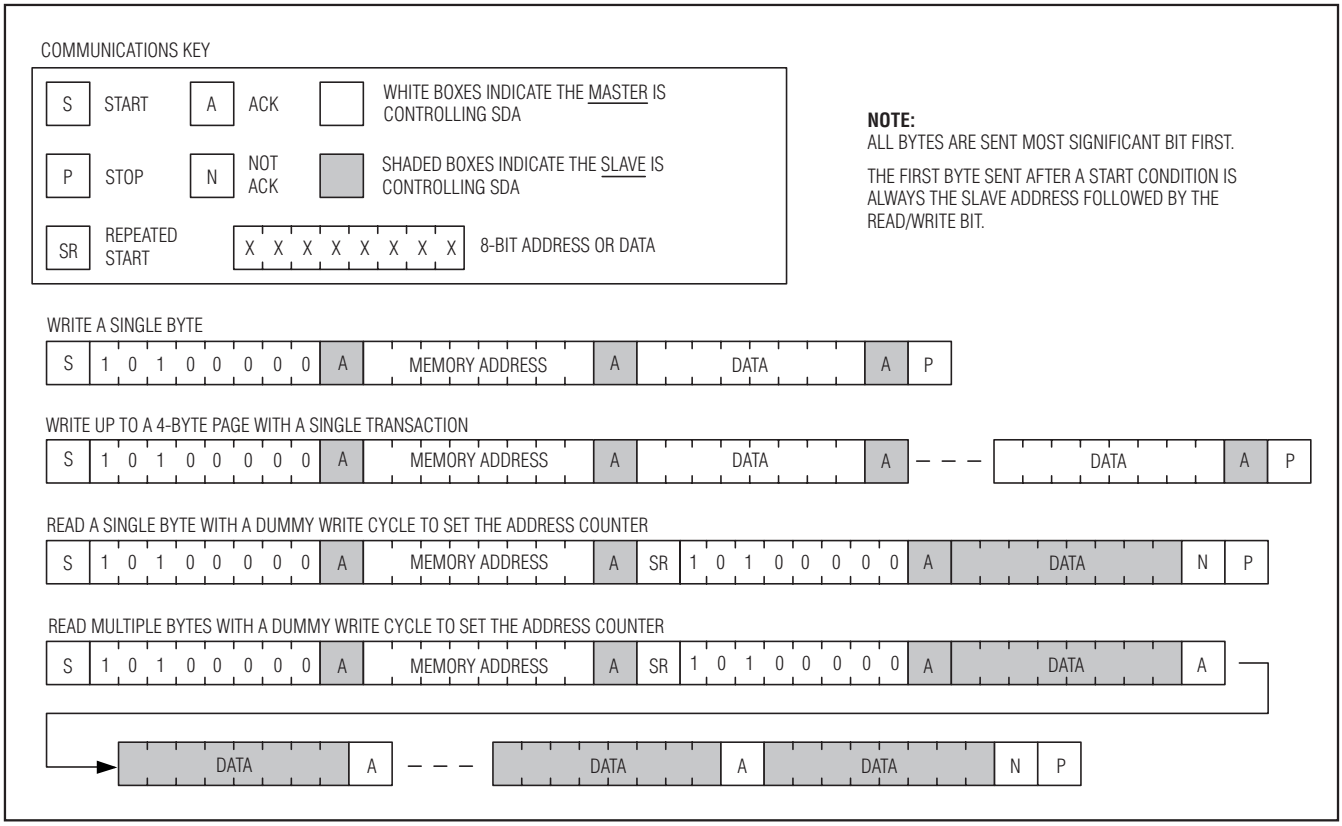

Figure 15. I²C Communications Examples

I²C Operation Using Packet Error Checking

Read Operation with Packet Error Checking

Packet error checking during reads is supported by the DS1862A. Information is transferred form the DS1862A in much the same way as conventional I²C protocol, however, an extra CRC field is added and checked. The master still begins by sending the device address (A0h for DS1862A), then the index pointer to the memory address of interest. The next byte transferred, however, is the value of the intended number of bytes to be read. The calculation of the CRC-8 includes and requires the explicit starting memory address to be included as the second transferred byte (dummy write byte). Next, the slave transfers the data back as the master acknowledges. Only 1 to 128 bytes can be sequentially read during one transmission while using PEC. After the master reads the intended number of bytes, the CRC-8 value is transmitted by the DS1862A. The master ends the communication with a NACK and a STOP. See Figure 16 for a graphical representation. The CRC-8 is calculated starting with the MSB of the memory address pointer, number of bytes to read, and the read data. The master can then verify the CRC-8 value and reject the read data if the CRC-8 value does not correspond to the received CRC value. The CRC-8 must be calculated by using the following polynomial for both reads and writes:

$$C(x) = X^8 + X^2 + X + 1$$

Write Operation with Packet Error Checking

Packet error checking during writes is also supported by the DS1862A. Information is written to the DS1862A in much the same way as conventional I²C protocol, however, an extra CRC field is added and checked. The master still begins by sending the device address, then the index pointer to the memory address of interest. The next byte, however, is the value of the intended number of bytes to be written. The calculation of the

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CRC-8 includes and requires the explicit starting memory address to be included as the second transferred byte. Next, the master transfers the data as the DS1862A acknowledges. Only 4 bytes can be sequentially written during one transmission while using PEC. After the master writes the intended number of bytes, the CRC-8 value should be transmitted. Following the CRC-8 byte, the master should transmit the CAB byte (CRC Add-on Byte). At this point, the DS1862A sends an ACK if the CRC-8 matches its internal calculated value or a NACK if not. Finally, the master should end the communication and send a STOP. See Figure 16 for a graphical representation. The CRC-8 is calculated starting with the MSB of the memory address pointer, number of bytes to be written, and the written data. The master can then poll the last ACK or NACK for successful transfer of written data.

For more information on I²C PEC communications, refer to the XFP and/or SMBus 2.0 standard.

Applications Information

Calibrating APC and Extinction Ratio

Before calibrating, the APC register should be set to a low value to ensure the laser's maximum power level is not exceeded before the power level is calibrated. Additionally, the ER should be set to a minimum value to ensure that a data test pattern does not cause the laser to shut off. Once the APC and ER registers are at minimal values, enable a data pattern and calibrate the average power level.

Calibrating the Average Power Level

While sending data through the laser diode, increase the value in the APC register until the light output matches the desired *average* power level. The average power level is the arithmetic average of the '1' and '0' power levels.

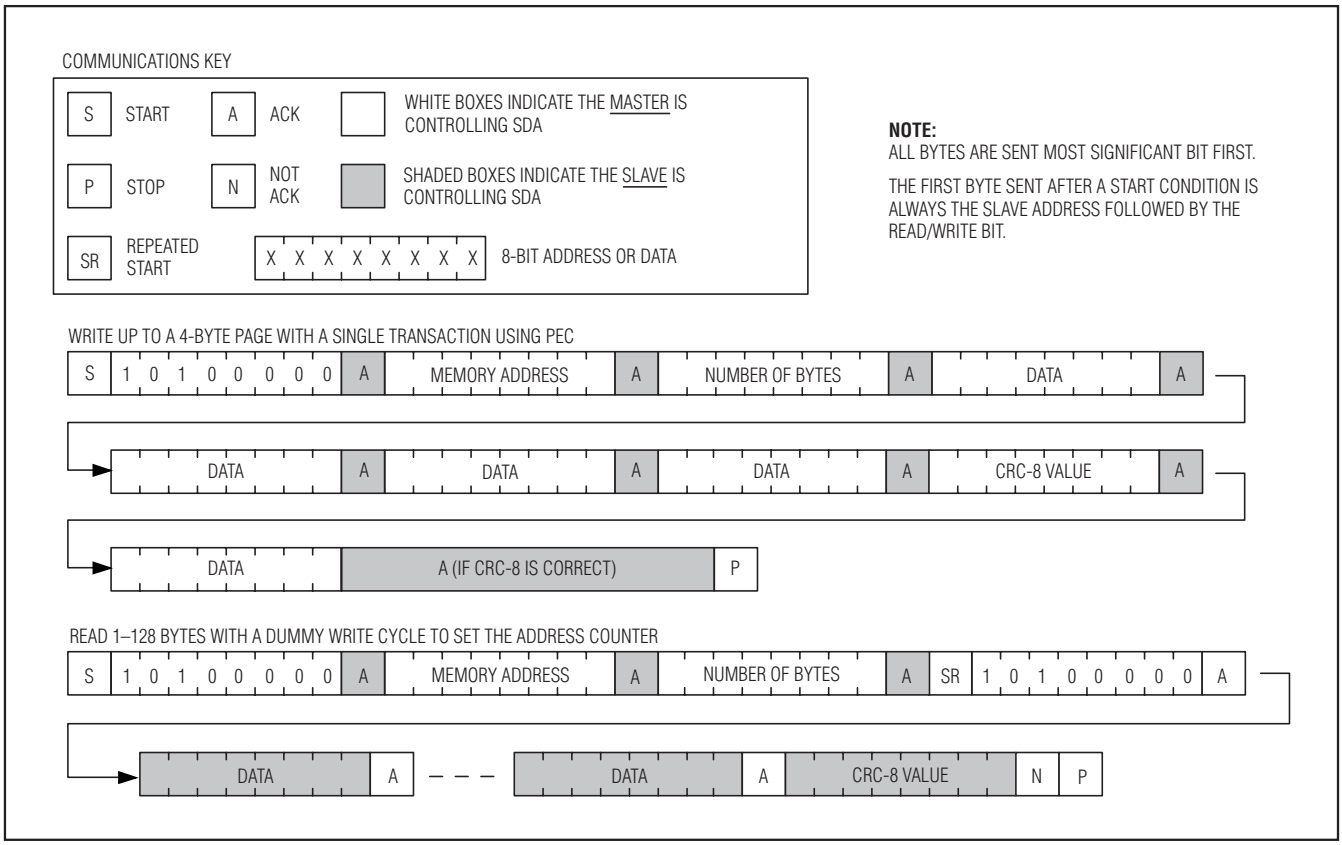

Figure 16. I²C PEC Communications Examples

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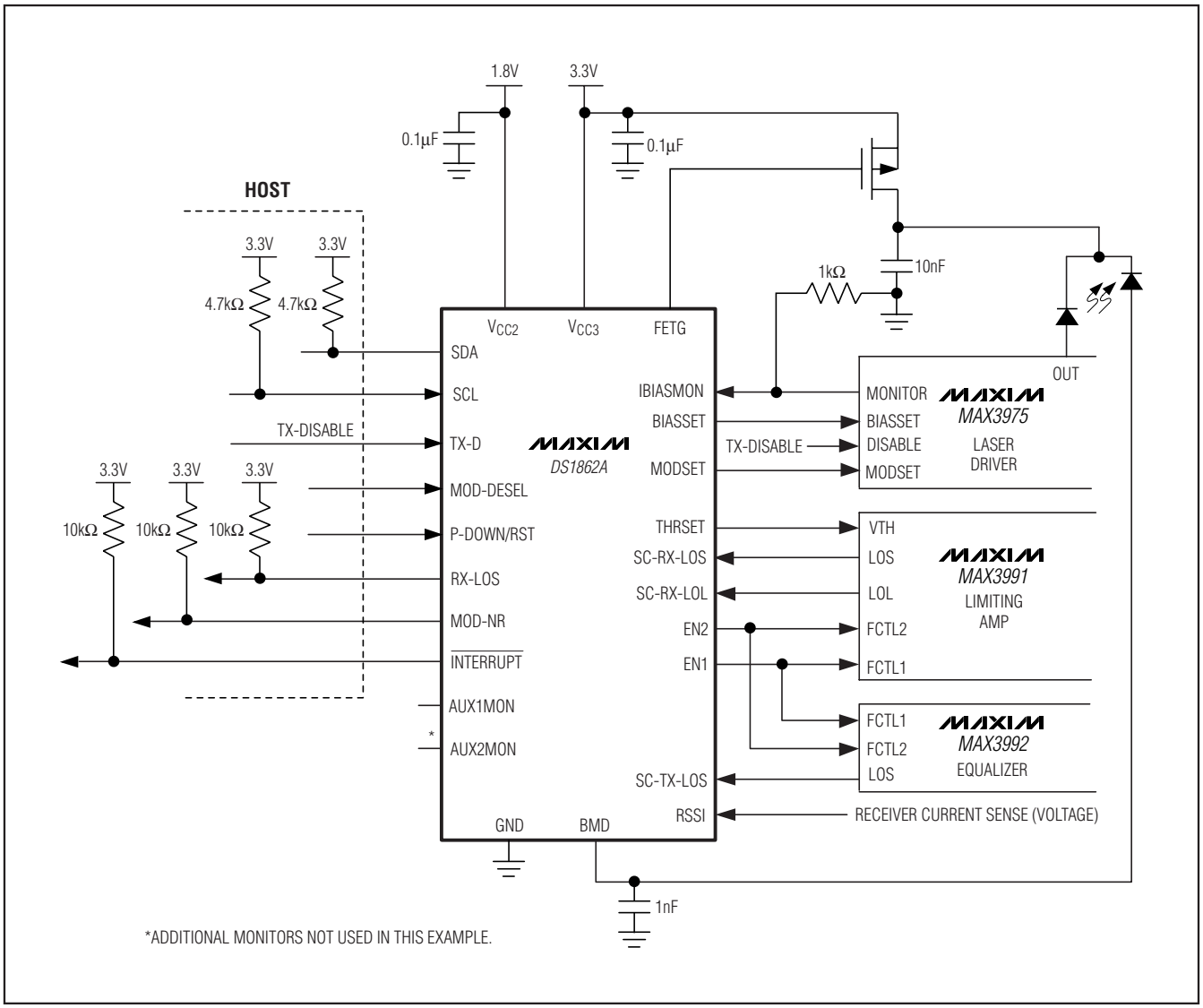
Power-Supply Decoupling

To achieve best results, it is recommended that the power supply is decoupled with a 0.01µF or a 0.1µF capacitor. Use high-quality, ceramic, surface-mount capacitors, and mount the capacitors as close as possible to the V_{CC2}/V_{CC3} and GND pins to minimize lead inductance.

SDA and SCL Pullup Resistors

SDA is an open-collector bidirectional data pin on the DS1862A that requires a pullup resistor to realize high logic levels. Either an open-collector output with a pullup resistor or a push-pull output driver can be utilized for the SCL input. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *I^2C AC Electrical Characteristics* are within specification.

Typical Operating Circuit



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Chip Information

TRANSISTOR COUNT: 75,457

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
25 CSBGA	X25+1	**21-0361**