4.5 Ω R_{ON}, 4-/8-Channel ±5 V,+12 V, +5 V, and +3.3 V Multiplexers

ADG1608/ADG1609

FEATURES

- 4.5 Ω typical on resistance
- 1 Ω on-resistance flatness
- Up to 470 mA continuous current
- ±3.3 V to ±8 V dual-supply operation
- 3.3 V to 16 V single-supply operation
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 16-lead TSSOP and 16-lead, 3 mm × 3 mm LFCSP

APPLICATIONS

- Communication systems
- Medical systems
- Audio signal routing
- Video signal routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Relay replacements

FUNCTIONAL BLOCK DIAGRAMS

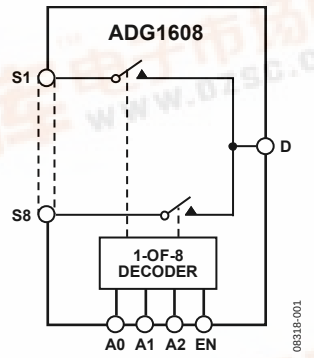

Figure 1.

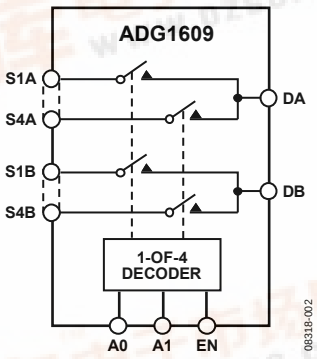

Figure 2.

GENERAL DESCRIPTION

The ADG1608/ADG1609 are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The ADG1608 switches one of eight inputs to a common output, as determined by the 3-bit binary address lines, A0, A1, and A2. The ADG1609 switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines, A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched off.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

The low on resistance of these switches make them ideal solutions for data acquisition and gain switching applications where low on resistance and distortion is critical. The on-resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals.

CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 8 Ω maximum on resistance over temperature.
2. Minimum distortion: THD + N = 0.04%
3. 3 V logic-compatible digital inputs: V_{INH} = 2.0 V, V_{INL} = 0.8 V.
4. No V_L logic power supply required.
5. Ultralow power dissipation: <8 nW.
6. 16-lead TSSOP and 16-lead, 3 mm × 3 mm LFCSP.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

7/09—Revision 0: Initial Version

SPECIFICATIONS

±5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	4.5			Ω typ	V_S = ±4.5 V, I_S = −10 mA; see Figure 25
	5	7	8	Ω max	V_{DD} = ±4.5 V, V_{SS} = ±4.5 V
On-Resistance Match Between Channels (ΔR_{ON})	0.12			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.25	0.3	0.35	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	1			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	1.3	1.7	2	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 26
	±0.1	±0.5	±3	nA max	
Drain Off Leakage, I_D (Off)	±0.03			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 26
ADG1608	±0.15	±2	±14	nA max	
ADG1609	±0.15	±1	±7	nA max	
Channel On Leakage, I_D, I_S (On)	±0.03			nA typ	V_S = V_D = ±4.5 V; see Figure 27
	±0.15	±2	±14	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±1			nA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	150			ns typ	R_L = 300 Ω, C_L = 35 pF
	182	230	258	ns max	V_S = 2.5 V; see Figure 28
t_{ON} (EN)	106			ns typ	R_L = 300 Ω, C_L = 35 pF
	132	150	160	ns max	V_S = 2.5 V; see Figure 30
t_{OFF} (EN)	113			ns typ	R_L = 300 Ω, C_L = 35 pF
	144	178	202	ns max	V_S = 2.5 V; see Figure 30
Break-Before-Make Time Delay, t_D	47			ns typ	R_L = 300 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 2.5 V; see Figure 29
Charge Injection	24			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 31
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 32
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34
Total Harmonic Distortion + Noise (THD + N)	0.04			% typ	R_L = 110 Ω, V_S = 5 V p-p, f = 20 Hz to 20 kHz; see Figure 35
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 33
ADG1608	40			MHz typ	
ADG1609	71			MHz typ	
C_S (Off)	20			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)					
ADG1608	120			pF typ	V_S = 0 V, f = 1 MHz
ADG1609	61			pF typ	V_S = 0 V, f = 1 MHz
C_D, C_S (On)					
ADG1608	153			pF typ	V_S = 0 V, f = 1 MHz
ADG1609	85			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			±3.3/±8	V min/max	

[1] Guaranteed by design, but not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	4			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 25
	4.5	6.5	7.5	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels (ΔR_{ON})	0.12			Ω typ	V_S = 10 V, I_S = −10 mA
	0.25	0.3	0.35	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.9			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	1.2	1.6	1.9	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 26
	±0.1	±0.5	±3	nA max	
Drain Off Leakage, I_D (Off)	±0.03			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 26
ADG1608	±0.15	±2	±14	nA max	
ADG1609	±0.15	±1	±7	nA max	
Channel On Leakage, I_D, I_S (On)	±0.03			nA typ	V_S = V_D = 1 V or 10 V; see Figure 27
	±0.15	±2	±14	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±1			nA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	113			ns typ	R_L = 300 Ω, C_L = 35 pF
	141	172	196	ns max	V_S = 8 V; see Figure 28
t_{ON} (EN)	80			ns typ	R_L = 300 Ω, C_L = 35 pF
	94	101	110	ns max	V_S = 8 V; see Figure 30
t_{OFF} (EN)	77			ns typ	R_L = 300 Ω, C_L = 35 pF
	93	117	140	ns max	V_S = 8 V; see Figure 30
Break-Before-Make Time Delay, t_D	47			ns typ	R_L = 300 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 8 V; see Figure 29
Charge Injection	29			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 31
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 32
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34
Total Harmonic Distortion + Noise (THD + N)	0.04			% typ	R_L = 110 Ω, V_S = 5 V p-p, f = 20 Hz to 20 kHz; see Figure 35
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 33
ADG1608	40			MHz typ	
ADG1609	78			MHz typ	
C_S (Off)	19			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)					
ADG1608	117			pF typ	V_S = 6 V, f = 1 MHz
ADG1609	59			pF typ	V_S = 6 V, f = 1 MHz
C_D, C_S (On)					
ADG1608	149			pF typ	V_S = 6 V, f = 1 MHz
ADG1609	84			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 12 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
ADG1608	300			μA typ	Digital inputs = 5 V
			480	μA max	
ADG1609	225			μA typ	Digital inputs = 5 V
			360	μA max	
V_{DD}			3.3/16	V min/max	

[1] Guaranteed by design, but not subject to production test.

5 V SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°Cto +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	8.5			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA; see Figure 25
	10	12.5	14	Ω max	V_{DD} = 4.5 V, V_{SS} = 0 V
On-Resistance Match Between Channels (ΔR_{ON})	0.15			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	0.3	0.35	0.4	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	1.7			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	2.3	2.7	3	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 26
	±0.1	±0.5	±3	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 26
ADG1608	±0.15	±2	±14	nA max	
ADG1609	±0.15	±1	±7	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 1 V or 4.5 V; see Figure 27
	±0.15	±2	±14	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±1			nA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	193			ns typ	R_L = 300 Ω, C_L = 35 pF
	251	301	339	ns max	V_S = 2.5 V; see Figure 28
t_{ON} (EN)	115			ns typ	R_L = 300 Ω, C_L = 35 pF
	152	171	184	ns max	V_S = 2.5 V; see Figure 30
t_{OFF} (EN)	140			ns typ	R_L = 300 Ω, C_L = 35 pF
	184	225	259	ns max	V_S = 2.5 V; see Figure 30
Break-Before-Make Time Delay, t_D	66			ns typ	R_L = 300 Ω, C_L = 35 pF
			37	ns min	V_{S1} = V_{S2} = 2.5 V; see Figure 29
Charge Injection	11			pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 31
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 32
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 34
Total Harmonic Distortion + Noise (THD + N)	0.3			% typ	R_L = 110 Ω, f = 20 Hz to 20 kHz, V_S = 3.5 V p-p; see Figure 35
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 33
ADG1608	37			MHz typ	
ADG1609	72			MHz typ	
C_S (Off)	22			pF typ	V_S = 2.5 V, f = 1 MHz
C_D (Off)					V_S = 2.5 V, f = 1 MHz
ADG1608	136			pF typ	
ADG1609	68			pF typ	
C_D, C_S (On)					V_S = 2.5 V, f = 1 MHz
ADG1608	168			pF typ	
ADG1609	94			pF typ	
POWER REQUIREMENTS					V_{DD} = 5.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
V_{DD}			3.3/16	V min/max	

[1] Guaranteed by design, but not subject to production test.

3.3 V SINGLE SUPPLY

V_{DD} = 3.3 V, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	13.5	15	16.5	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA; see Figure 25, V_{DD} = 3.3 V, V_{SS} = 0 V
On-Resistance Match Between Channels (ΔR_{ON})	0.25	0.28	0.3	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
On-Resistance Flatness ($R_{FLAT(ON)}$)	5	5.5	6.5	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = 3.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 0.6 V/3 V, V_D = 3 V/0.6 V; see Figure 26
	±0.1	±0.5	±3	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = 0.6 V/3 V, V_D = 3 V/0.6 V; see Figure 26
ADG1608	±0.15	±2	±14	nA max	
ADG1609	±0.15	±1	±7	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 0.6 V or 3 V; see Figure 27
	±0.15	±2	±14	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±1			nA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	312			ns typ	R_L = 300 Ω, C_L = 35 pF
	437	498	542	ns max	V_S = 1.5 V; see Figure 28
t_{ON} (EN)	216			ns typ	R_L = 300 Ω, C_L = 35 pF
	309	331	344	ns max	V_S = 1.5 V; see Figure 30
t_{OFF} (EN)	236			ns typ	R_L = 300 Ω, C_L = 35 pF
	316	367	411	ns max	V_S = 1.5 V; see Figure 30
Break-Before-Make Time Delay, t_D	104			ns typ	R_L = 300 Ω, C_L = 35 pF
			48	ns min	V_{S1} = V_{S2} = 1.5 V; see Figure 29
Charge Injection	6			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 31
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 32
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 34
Total Harmonic Distortion + Noise (THD + N)	0.5			% typ	R_L = 110 Ω, f = 20 Hz to 20 kHz, V_S = 2 V p-p; see Figure 35
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 33
ADG1608	34			MHz typ	
ADG1609	72			MHz typ	
C_S (Off)	23			pF typ	V_S = 1.5 V, f = 1 MHz
C_D (Off)					V_S = 1.5 V, f = 1 MHz
ADG1608	145			pF typ	
ADG1609	72			pF typ	
C_D, C_S (On)					V_S = 1.5 V, f = 1 MHz
ADG1608	173			pF typ	
ADG1609	95			pF typ	
POWER REQUIREMENTS					V_{DD} = 3.6 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
V_{DD}			3.3/16	V min/max	

[1] Guaranteed by design, but not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 5. ADG1608

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
V_{DD} = +5 V, V_{SS} = −5 V				
TSSOP (θ_{JA} = 112.6°C/W)	290	180	100	mA max
LFCSP (θ_{JA} = 48.7°C/W)	470	255	120	mA max
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	213	129	73	mA max
LFCSP (θ_{JA} = 48.7°C/W)	346	185	84	mA max
V_{DD} = 5 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	157	101	63	mA max
LFCSP (θ_{JA} = 48.7°C/W)	252	150	77	mA max
V_{DD} = 3.3 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	126	87	56	mA max
LFCSP (θ_{JA} = 48.7°C/W)	206	129	73.5	mA max

Table 6. ADG1609

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
V_{DD} = +5 V, V_{SS} = −5 V				
TSSOP (θ_{JA} = 112.6°C/W)	147	98	63	mA max
LFCSP (θ_{JA} = 48.7°C/W)	245	147	77	mA max
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	157	101	63	mA max
LFCSP (θ_{JA} = 48.7°C/W)	255	150	77	mA max
V_{DD} = 5 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	115	80	52	mA max
LFCSP (θ_{JA} = 48.7°C/W)	189	119	70	mA max
V_{DD} = 3.3 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	94	66	45	mA max
LFCSP (θ_{JA} = 48.7°C/W)	154	101	63	mA max

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	18 V
V_{DD} to GND	−0.3 V to +18 V
V_{SS} to GND	+0.3 V to −18 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	710 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D[2]	Data + 15%
Operating Temperature Range	
Industrial (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board)	112.6°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board)	48.7°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.
[2] See Table 5 and Table 6.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

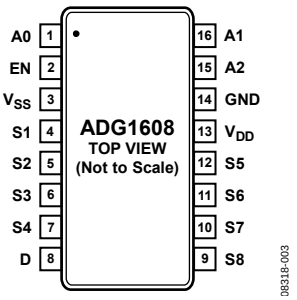

Figure 3. ADG1608 Pin Configuration (TSSOP)

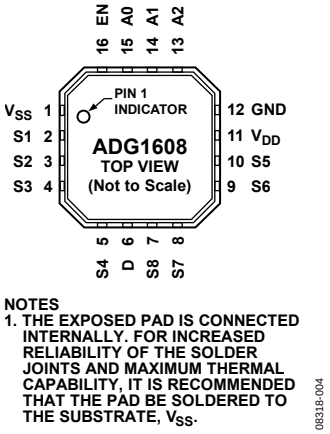

Figure 4. ADG1608 Pin Configuration (LFCSP)

Table 8. ADG1608 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, Ax logic inputs determine on switches.
3	1	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	2	S1	Source Terminal 1. Can be an input or an output.
5	3	S2	Source Terminal 2. Can be an input or an output.
6	4	S3	Source Terminal 3. Can be an input or an output.
7	5	S4	Source Terminal 4. Can be an input or an output.
8	6	D	Drain Terminal. Can be an input or an output.
9	7	S8	Source Terminal 8. Can be an input or an output.
10	8	S7	Source Terminal 7. Can be an input or an output.
11	9	S6	Source Terminal 6. Can be an input or an output.
12	10	S5	Source Terminal 5. Can be an input or an output.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	GND	Ground (0 V) Reference.
15	13	A2	Logic Control Input.
16	14	A1	Logic Control Input.
N/A	EP	EP	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 9. ADG1608 Truth Table

A2	A1	A0	EN	On Switch
X[1]	X[1]	X[1]	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

[1] X = don't care.

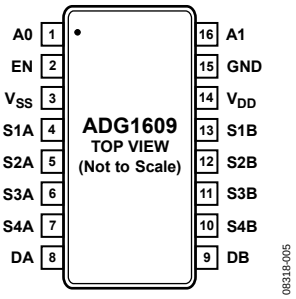

Figure 5. ADG1609 Pin Configuration (TSSOP)

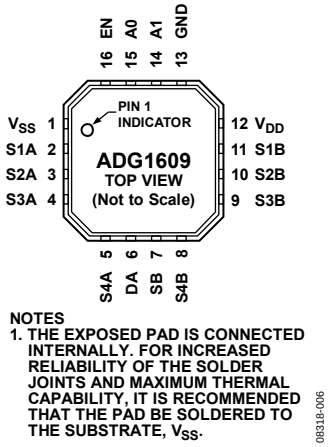

Figure 6. ADG1609 Pin Configuration (LFCSP)

Table 10. ADG1609 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, Ax logic inputs determine on switches.
3	1	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	2	S1A	Source Terminal 1A. Can be an input or an output.
5	3	S2A	Source Terminal 2A. Can be an input or an output.
6	4	S3A	Source Terminal 3A. Can be an input or an output.
7	5	S4A	Source Terminal 4A. Can be an input or an output.
8	6	DA	Drain Terminal A. Can be an input or an output.
9	7	DB	Drain Terminal B. Can be an input or an output.
10	8	S4B	Source Terminal 4B. Can be an input or an output.
11	9	S3B	Source Terminal 3B. Can be an input or an output.
12	10	S2B	Source Terminal 2B. Can be an input or an output.
13	11	S1B	Source Terminal 1B. Can be an input or an output.
14	12	V_{DD}	Most Positive Power Supply Potential.
15	13	GND	Ground (0 V) Reference.
16	14	A1	Logic Control Input.
N/A	EP	EP	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 11. ADG1609 Truth Table

A1	A0	EN	On Switch Pair
X[1]	X[1]	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

[1] X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

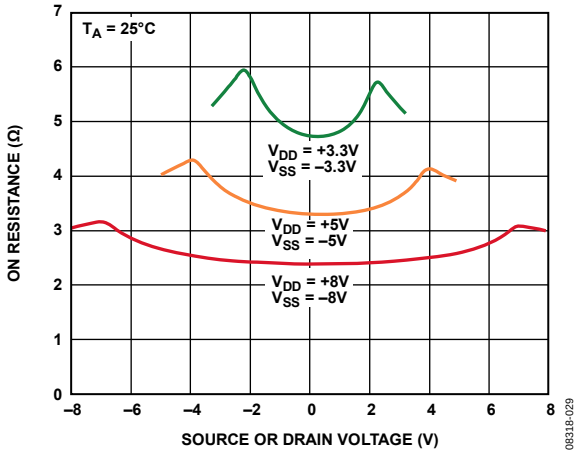

Figure 7. On Resistance vs. V_D (V_S) for Dual Supply

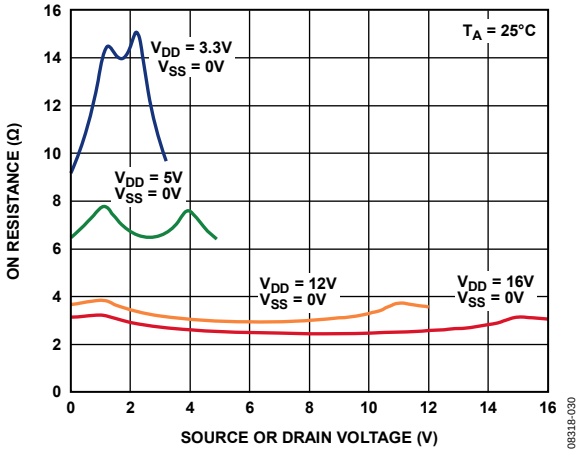

Figure 8. On Resistance vs. V_D (V_S) for Single Supply

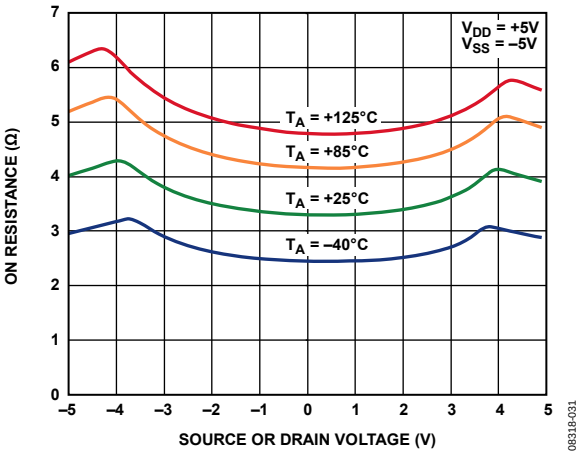

Figure 9. On Resistance vs. V_D (V_S) for Different Temperatures, ±5 V Dual Supply

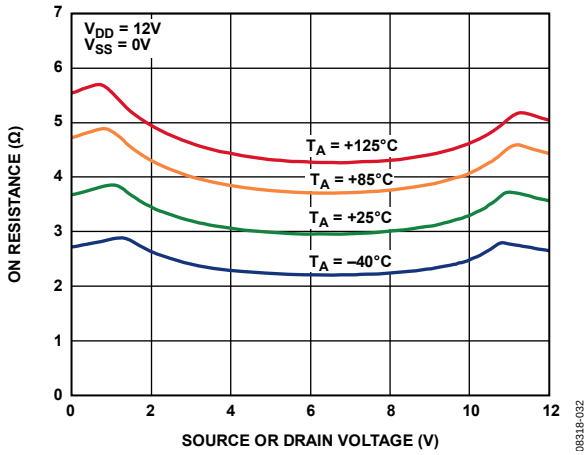

Figure 10. On Resistance vs. V_D (V_S) for Different Temperatures, 12 V Single Supply

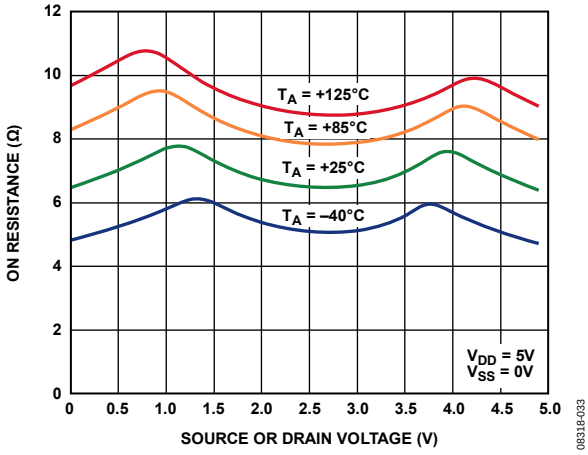

Figure 11. On Resistance vs. V_D (V_S) for Different Temperatures, 5 V Single Supply

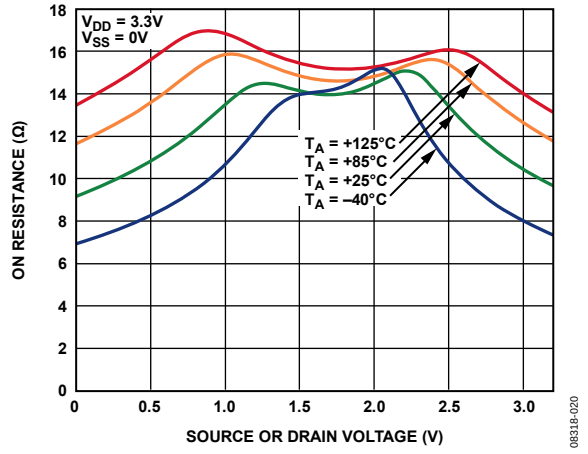

Figure 12. On Resistance vs. V_D (V_S) for Different Temperatures, 3.3 V Single Supply

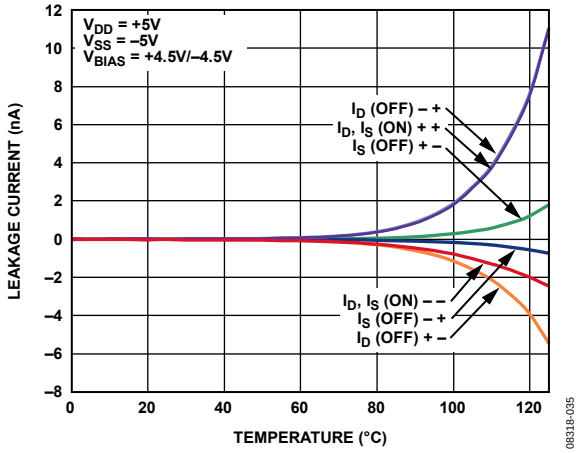

Figure 13. ADG1608 Leakage Currents vs. Temperature, ±5 V Dual Supply

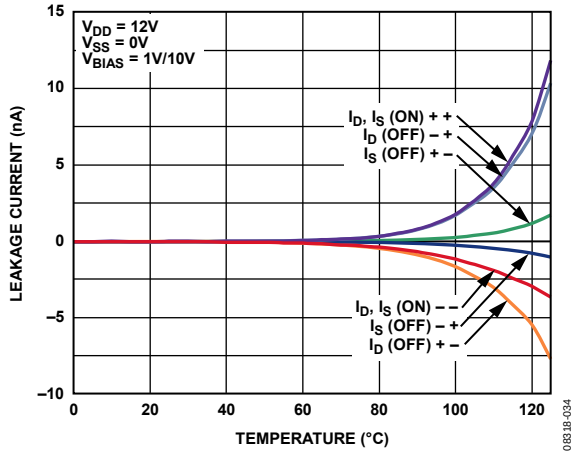

Figure 14. ADG1608 Leakage Currents vs. Temperature, 12 V Single Supply

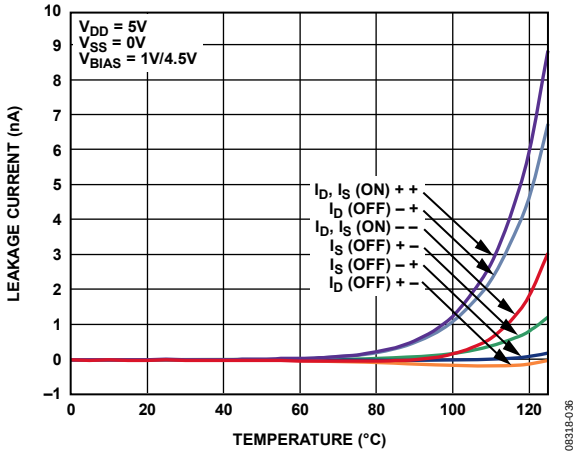

Figure 15.ADG1608 Leakage Currents vs. Temperature, 5 V Single Supply

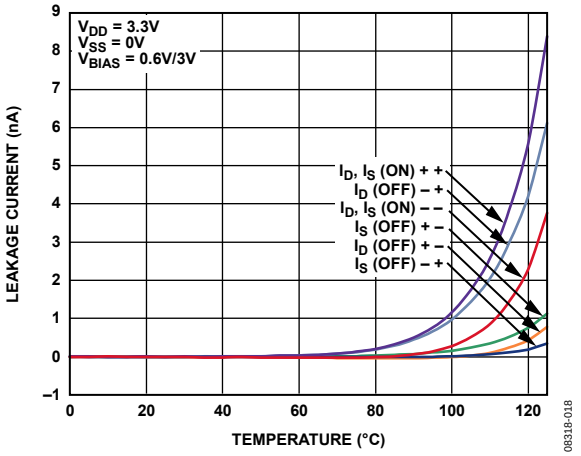

Figure 16. ADG1608 Leakage Currents vs. Temperature, 3.3 V Single Supply

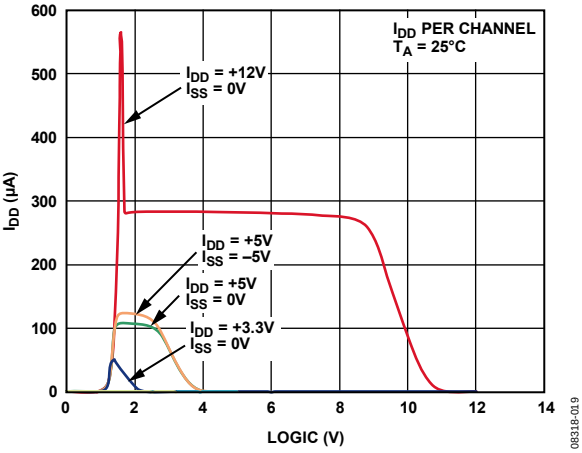

Figure 17. I_{DD} vs. Logic Level

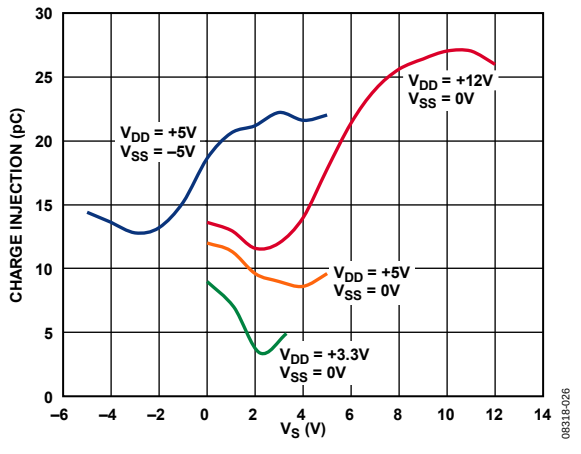

Figure 18. Charge Injection vs. Source Voltage

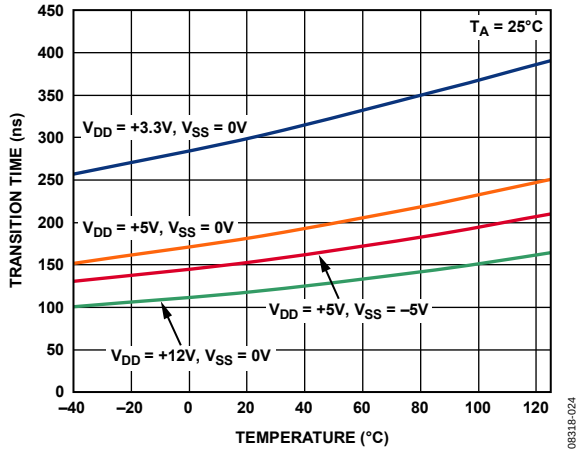

Figure 19. Transition Time vs. Temperature

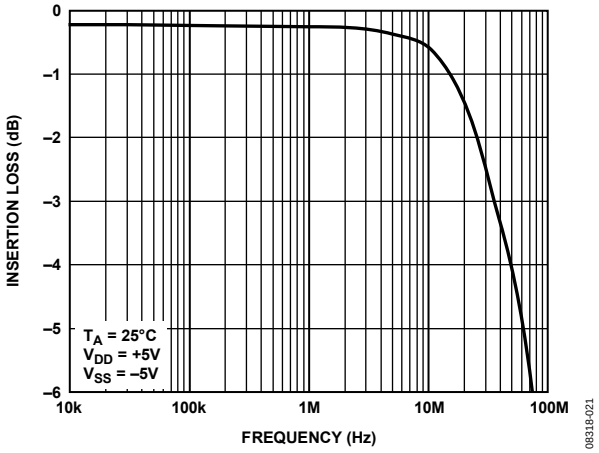

Figure 22. On Response vs. Frequency

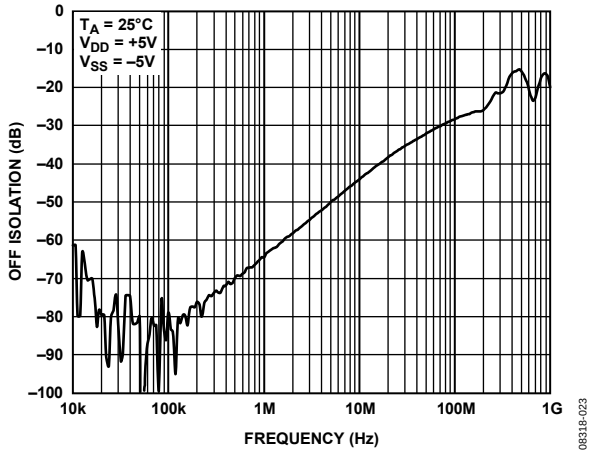

Figure 20. Off Isolation vs. Frequency

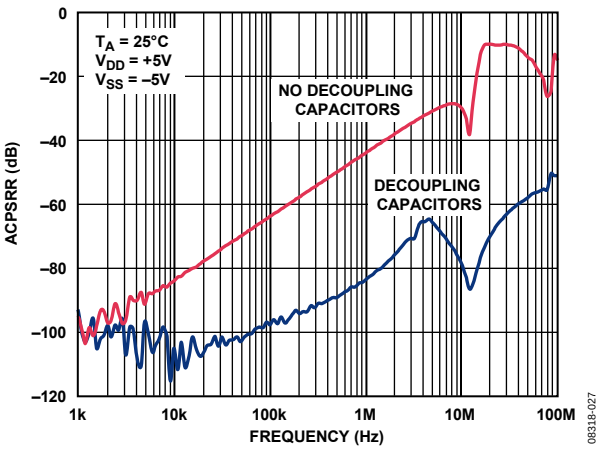

Figure 23. ACPSRR vs. Frequency

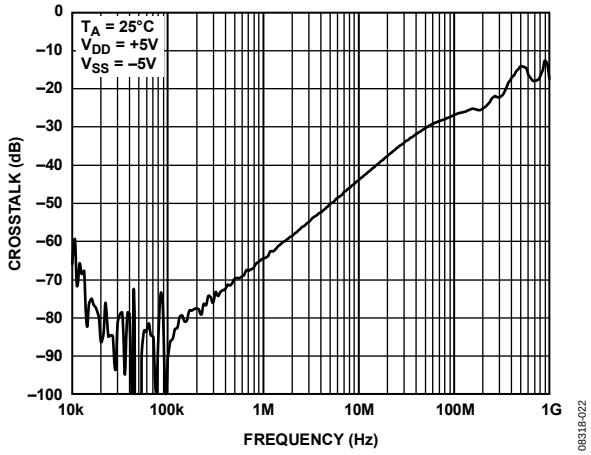

Figure 21. Crosstalk vs. Frequency

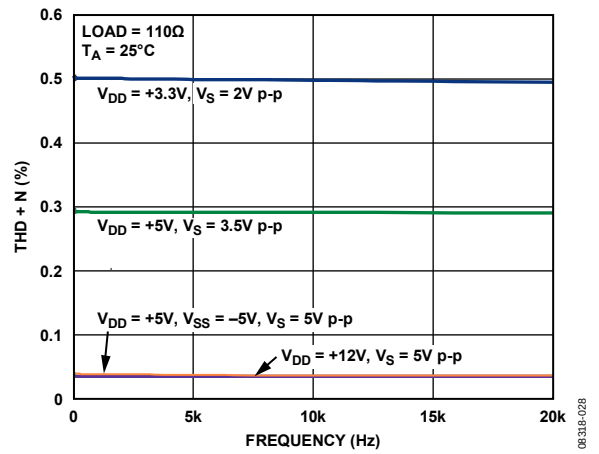

Figure 24. THD + N vs. Frequency

TEST CIRCUITS

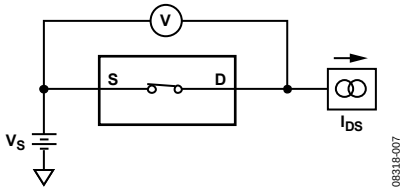

Figure 25. On Resistance

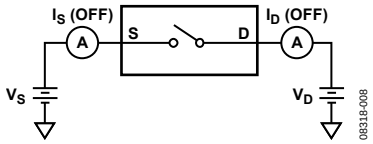

Figure 26. Off Leakage

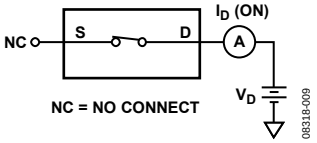

Figure 27. On Leakage

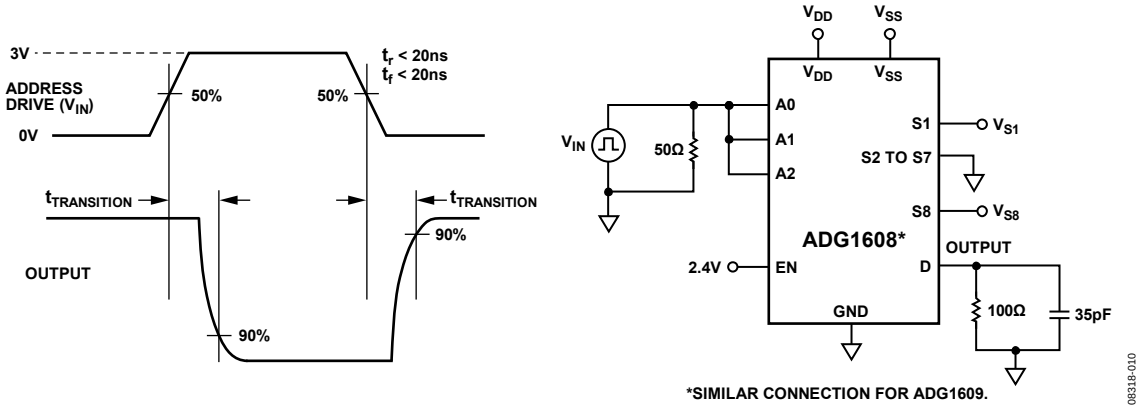

Figure 28. Address to Output Switching Times, $t_{TRANSITION}$

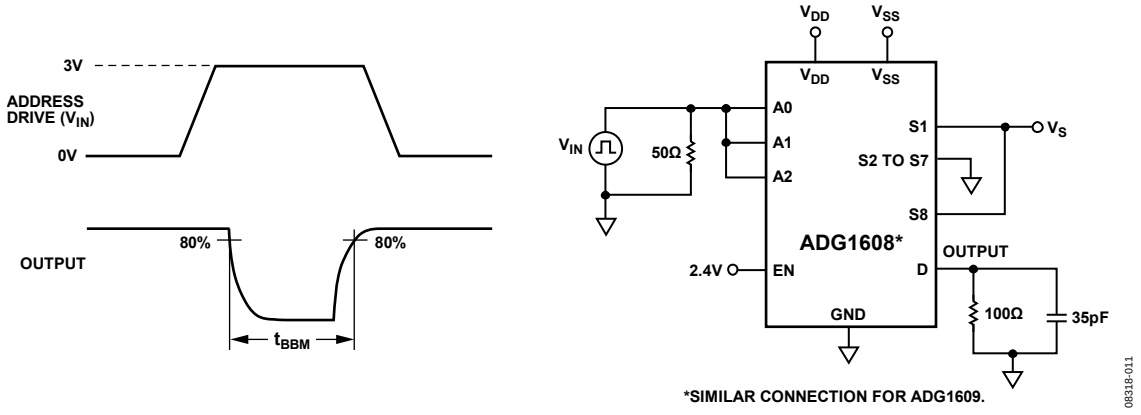

Figure 29. Break-Before-Make Delay, t_{BBM}

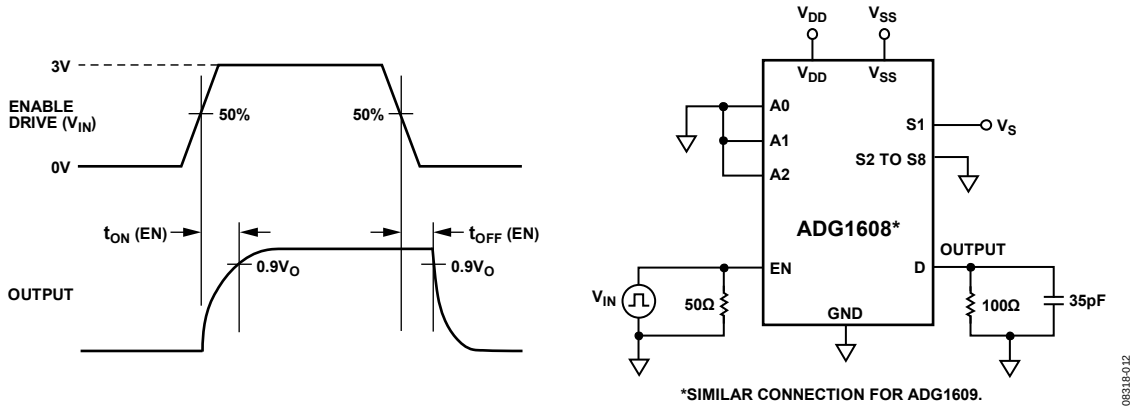

Figure 30. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

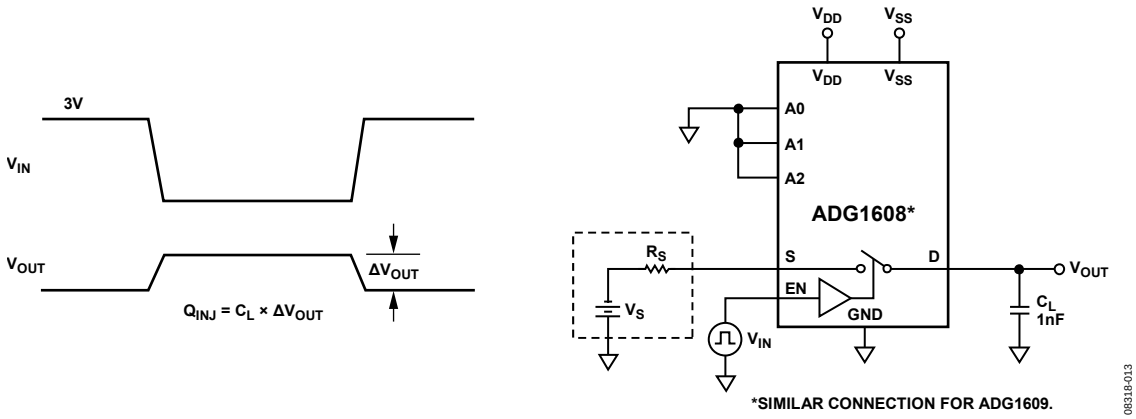

Figure 31. Charge Injection

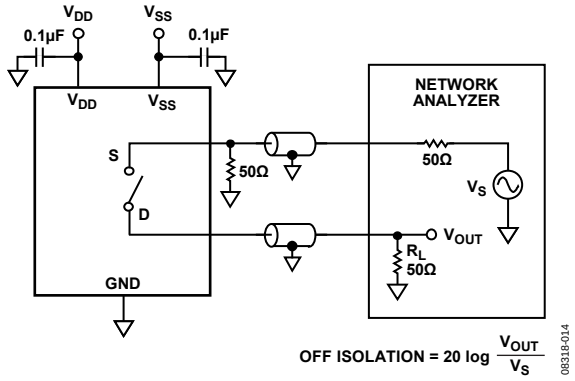

Figure 32. Off Isolation

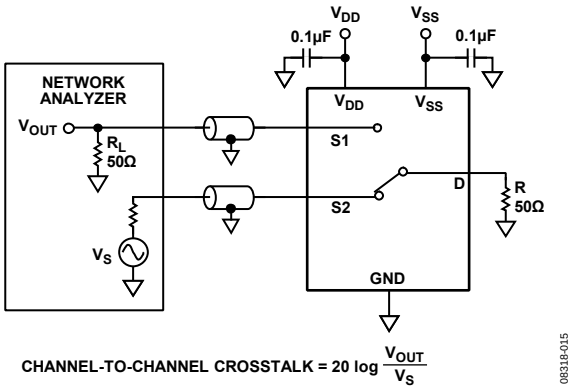

Figure 34. Channel-to-Channel Crosstalk

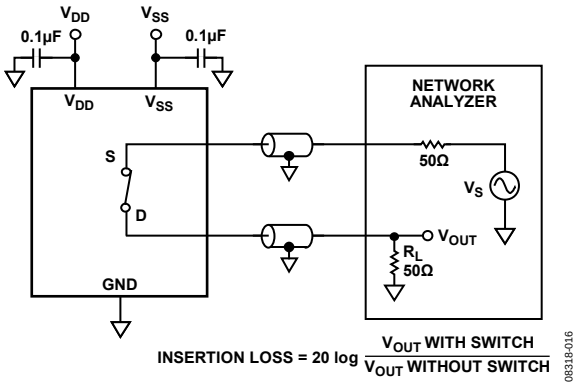

Figure 33. Bandwidth

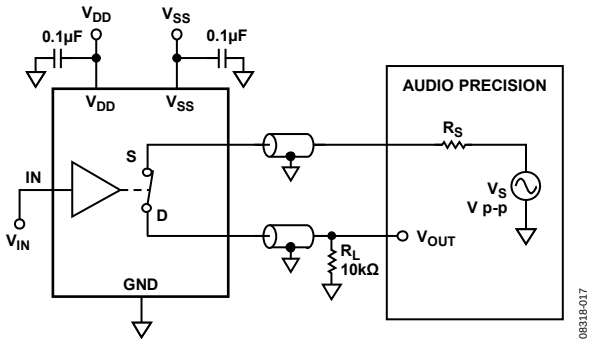

Figure 35. THD + Noise

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D (V_S)
The analog voltage on Terminal D and Terminal S.

R_{ON}
The ohmic resistance between Terminal D and Terminal S.

$R_{FLAT(ON)}$
Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, which is measured with reference to ground.

C_D (Off)
The off switch drain capacitance, which is measured with reference to ground.

C_D, C_S (On)
The on switch capacitance, which is measured with reference to ground.

C_{IN}
The digital input capacitance.

$t_{TRANSITION}$
The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

t_{ON} (EN)
The delay between applying the digital control input and the output switching on.

t_{OFF} (EN)
The delay between applying the digital control input and the output switching off .

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)
The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

OUTLINE DIMENSIONS

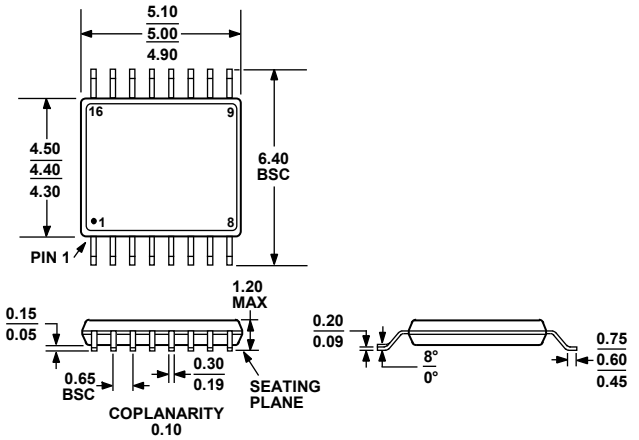

Figure 36. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

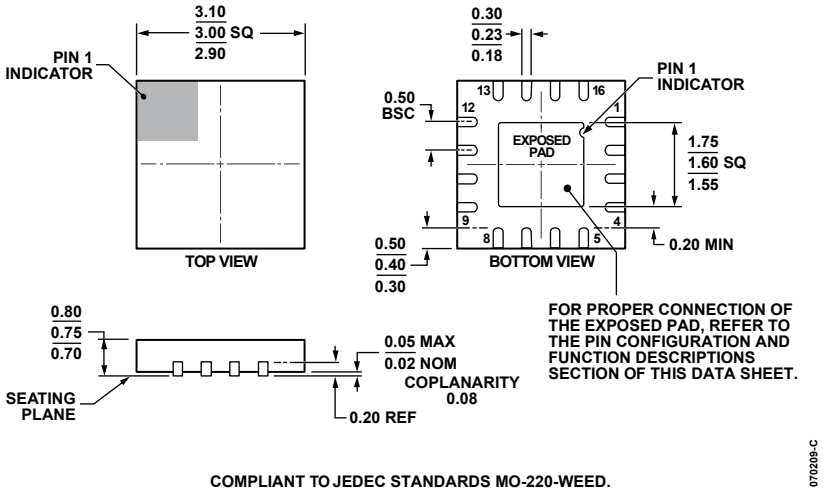

Figure 37. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm x 3 mm Body, Very Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG1608BRUZ[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1608BRUZ-REEL7[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1608BCPZ-REEL7[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	S38
ADG1609BRUZ[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1609BRUZ-REEL7[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1609BCPZ-REEL7[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	S39

[1] Z = RoHS Compliant Part.

NOTES

NOTES