NCP1205

Single Ended PWM Controller Featuring QR Operation and Soft Frequency Foldback

The NCP1205 combines a true Current Mode Control modulator and a demagnetization detector to ensure full Discontinuous Conduction Mode in any load/line conditions and minimum drain voltage switching (Quasi−Resonant operation, also called critical conduction operation). With its inherent Variable Frequency Mode (VFM), the controller decreases its operating frequency at constant peak current whenever the output power demand diminishes. Associated with automatic multiple valley switching, this unique architecture guarantees minimum switching losses and the lowest power drawn from the mains when operating at no−load conditions. Thus, the NCP1205 is optimal for applications targeting the newest International Energy Agency (IEA) recommendations for standby power.

The internal High−Voltage current source provides a reliable charging path for the V_{CC} capacitor and ensures a clean and short startup sequence without deteriorating the efficiency once off.

The continuous feedback signal monitoring implemented with an Overcurrent fault Protection circuitry (OCP) makes the final design rugged and reliable. The PDIP−14 offers an adjustable version of the OVP threshold via an external resistive network.

Features

- Natural Drain Valley Switching for Lower EMI and Quasi−Resonant Operation (QR)
- Smooth Frequency Foldback for Low Standby and Minimum Ripple at Light−Load
- Adjustable Maximum Switching Frequency
- Internal 200 ns Leading Edge Blanking on Current Sense
- 250 mA Sink and Source Driver
- Wide Operating Voltages: 8.0 to 30 V
- Wide UVLO Levels: 7.2 to 15 V Typical
- Auto−Recovery Internal Short−Circuit Protection (OCP)
- Integrated 3.0 mA Typ Startup Source
- Current Mode Control
- Adjustable Overvoltage Level
- Pb−Free Packages are Available*

Applications

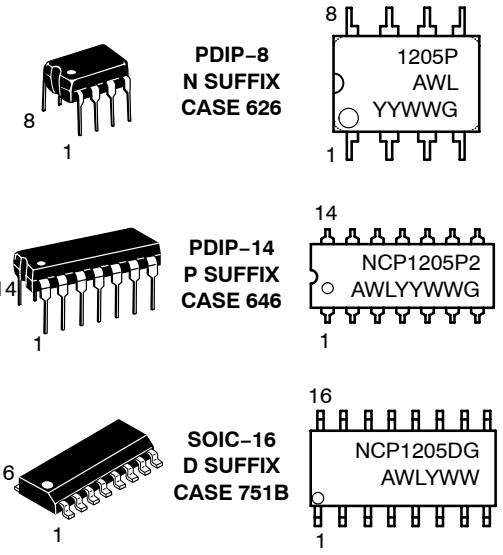
- High Power AC/DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Power Supplies for DVD, CD Players, TVs, Set−Top Boxes, etc.
- Auxiliary Power Supplies (USB, Appliances, etc.)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM



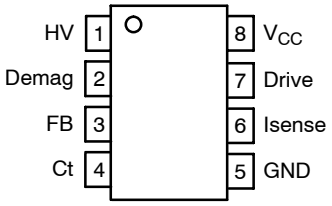
A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

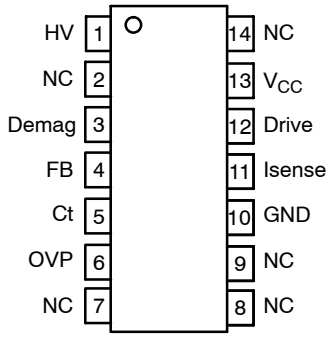
Device	Package	Shipping†
NCP1205P	PDIP−8	50 Units/Rail
NCP1205PG	PDIP−8 (Pb−Free)	50 Units/Rail
NCP1205P2	PDIP−14	25 Units/Rail
NCP1205P2G	PDIP−14 (Pb−Free)	25 Units/Rail
NCP1205DR2	SOIC−16	2500/Tape & Reel
NCP1205DR2G	SOIC−16 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

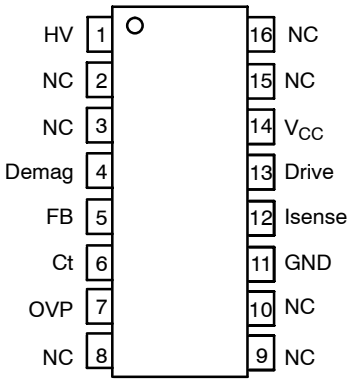
PIN CONNECTIONS



PDIP−8



PDIP−14



SOIC−16

PIN FUNCTION DESCRIPTION

Pin No.			Pin Name	Function	Description
PDIP−8	PDIP−14	SOIC−16			
1	1	1	HV	Startup rail	Connected to the rectified HV rail, this pin provides a charging path to V_{CC} bulk capacitor.
2	3	4	Demag	Zero primary−current detection	This pin ensures the restart of the main switcher when operating in free−run.
3	4	5	FB	Feedback signal to control the PWM	This level modulates the peak current level in free−running operation and modulates the frequency in VFM operation.
4	5	6	Ct	Timing capacitor	By adding a capacitor from Ct to the ground, the user selects the minimum/maximum operating frequency.
5	10	11	GND	The IC's ground	−
NA	6	7	OVP	Overvoltage input	By applying a 2.8 V typical level on this pin, the IC is permanently latched−off until V_{CC} falls below $UVLO_L$.
6	11	12	Isense	The primary−current sensing pin	This pin senses the primary current via an external shunt resistor.
7	12	13	Drv	This pin drives the external switcher	The IC is able to deliver or absorb 250 mA peak currents while delivering a clamped driving signal.
8	13	14	V_{CC}	Powers the IC	A positive voltage up to 30 V maximum can be applied upon this pin before the IC stops.

1. PDIP−14 has different pinouts. Please see Pin Connections.
2. Pin 2, 7, 8, 9 and 14 are nonconnected on PDIP−14.
3. Pin 2, 3, 8, 9, 10, 15 and 16 are nonconnected on SOIC−16.

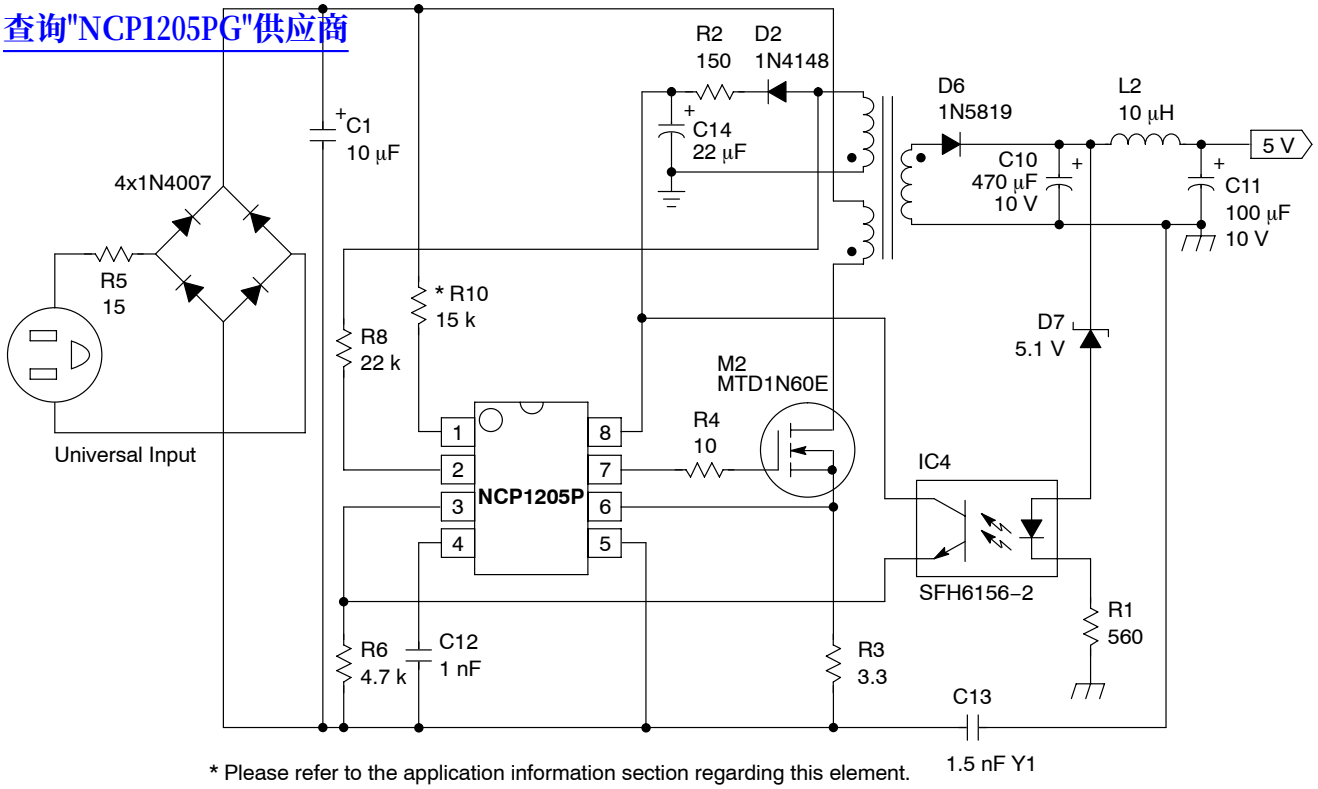


Figure 1. Typical Application Example for PDIP−8 Version

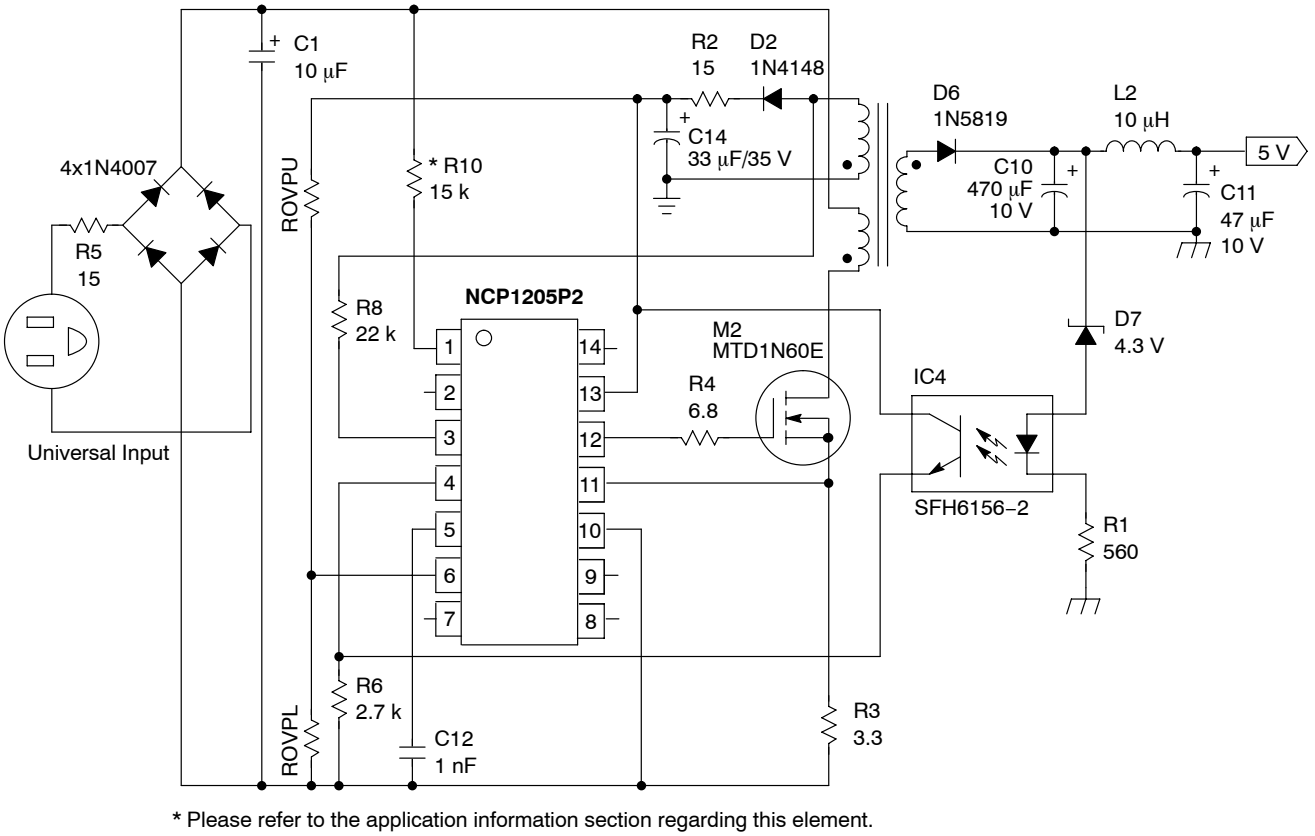


Figure 2. Typical Application Example for PDIP−14 Version

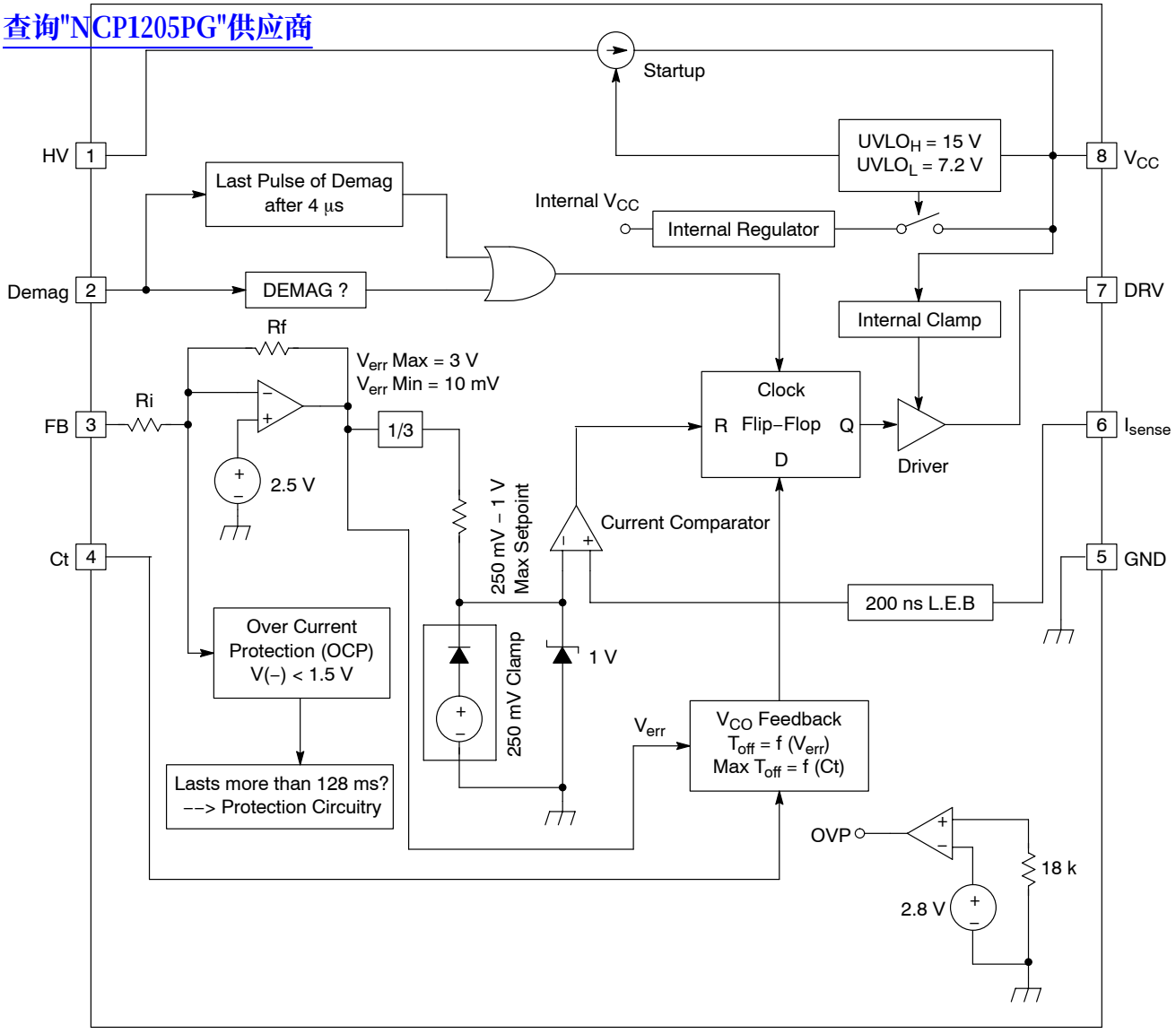


Figure 3. Internal Circuit Architecture for PDIP−8 Version

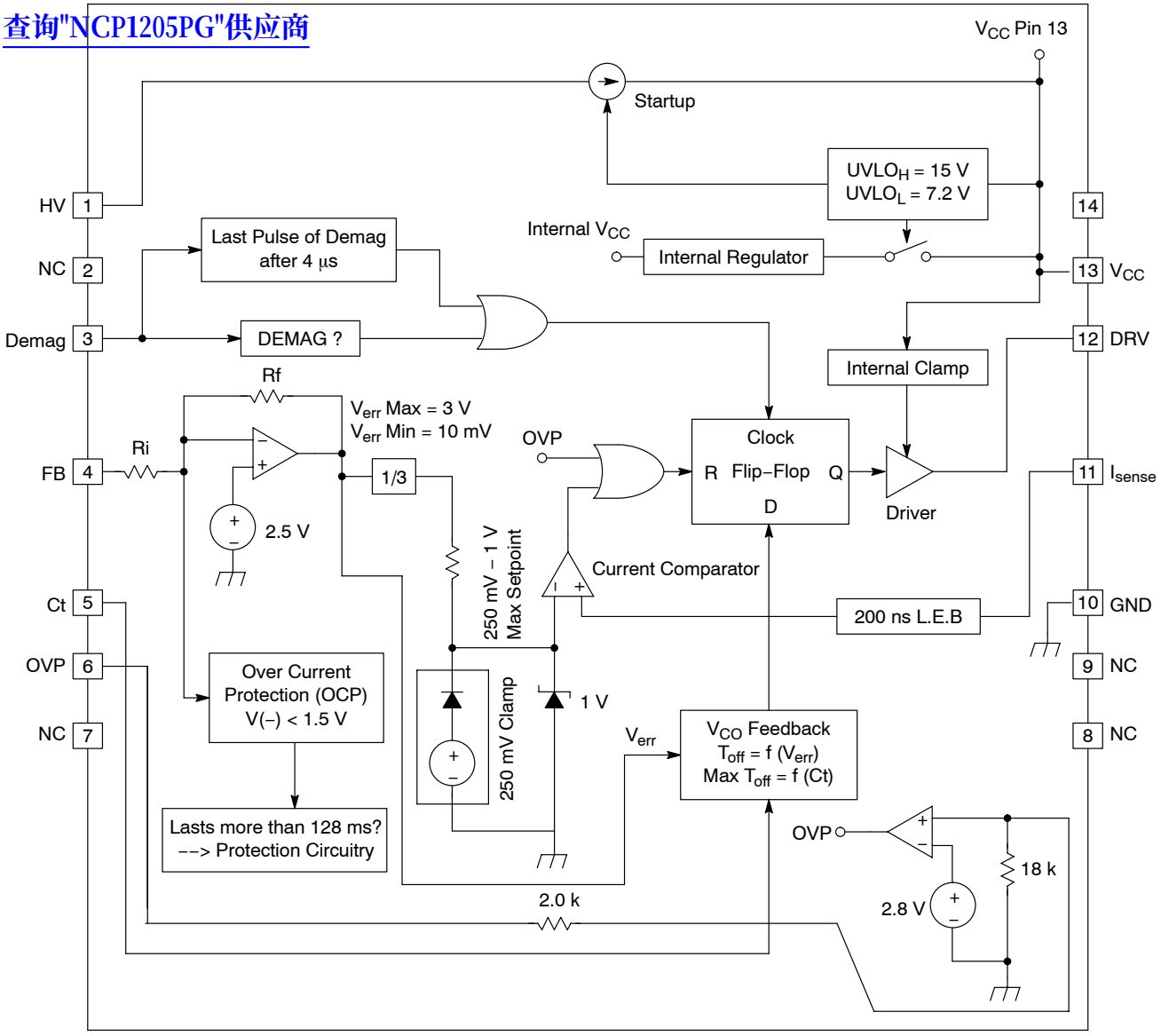


Figure 4. Internal Circuit Architecture for PDIP−14 Version

MAXIMUM RATINGS

Rating		Pin No. PDIP−8	Pin No. PDIP−14	Pin No. SOIC−16	Symbol	Value Min	Value Max	Unit
Power Supply Voltage		8	13	14	V_{in}	−	30	V
Thermal Resistance Junction−to−Air	PDIP−8	−	−	−	$R_{\theta JA}$	−	100	°C/W
	PDIP−14	−	−	−		−	100	
	SOIC−16	−	−	−			145	
Operating Junction Temperature Range		−	−	−	T_J	−	−25 to +125	°C
Maximum Junction Temperature		−	−	−	T_{Jmax}	−	150	°C
Storage Temperature Range		−	−	−	T_{stg}	−	−60 to +150	°C
ESD Capability, HBM Model		All Pins	All Pins	All Pins	−	−	2.0	kV
ESD Capability, Machine Model		All Pins	All Pins	All Pins	−	−	200	V
Demagnetization Pin Current		2	3	4	−	−	−5.0/+10	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_J = −25°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted.)

Characteristics	Pin No. PDIP−8	Pin No. PDIP−14	Pin No. SOIC−16	Symbol	Min	Typ	Max	Unit
Demagnetization Block								
Input Threshold Voltage (V_{pin2} increasing)	2	3	4	Vth	50	65	85	mV
Hysteresis (V_{pin2} decreasing)	2	3	4	V_H	−	30	−	mV
Input Clamp Voltage High State (I_{pin2} = 3.0 mA) Low State (I_{pin2} = −3.0 mA)	2	3	4	 VC_H VC_L	 8.0 −0.9	 10 −0.7	 12 −0.5	V
Demag Propagation Delay	−	−	−	−	100	300	350	ns
No Demag Signal Activation	−	−	−	−	−	4.0	8.0	μs
Internal Input Capacitance at 1.0 V	2	3	4	C_{pin2}	−	10	−	pF
Demag Propagation Delay with 22 kΩ External Resistor	2	3	4	−	100	370	480	ns
Feedback Path								
Input Impedance at V_{FB} = 3.0 V	3	4	5	Zin	−	50	−	kΩ
Internal Error Amplifier Closed Loop Gain	3	4	5	AV_{CL}	−	−3.0	−	−
Internal Built−In Offset Voltage for Error Detection	−	−	−	V_{ref}	2.2	2.5	2.8	V
Error Amplifier Level of VCO Take Over	−	−	−	−	−	1.0	−	V
Internal Divider from Internal Error Amp, Pin to Current Setpoint	−	−	−	−	−	3.0	−	−
Fault Detection Circuitry								
Internal Over Current Level	−	−	−	WL_L	−	1.5	−	V
Fault Time Duration to Latch Activation @ Ct = 1.0 ηF	−	−	−	−	−	128	−	ms
Over Current Latchoff Phase @ Ct = 1.0 ηF	−	−	−	−	−	1.0	−	s
Hysteresis when V_{FB} goes back into Regulation	−	−	−	−	−	100	−	mV
Overvoltage Protection Threshold for PDIP−14 and SOIC−16 versions	6	−	7	OVP1	2.5	2.8	3.1	V
Current Sense Comparator								
Input Bias Current @ 1.0 V	6	11	12	I_{IB}	−	0.02	−	μA
Maximum Current Setpoint	6	11	12	V_{cl}	0.9	1.0	1.1	V
Minimum Current Setpoint	6	11	12	V_{min}	225	250	285	mV

ELECTRICAL CHARACTERISTICS (continued) (For typical values T_A = 25°C, for min/max values T_J = 25°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted.)

Characteristics	Pin No. PDIP−8	Pin No. PDIP−14	Pin No. SOIC−16	Symbol	Min	Typ	Max	Unit
Current Sense Comparator (continued)								
Propagation Delay from Current Detection to Gate OFF State	6	11	12	T_{del}	–	200	250	ns
Leading Edge Blanking (LEB)	6	11	12	T_{leb}	–	200	–	ns
Frequency Modulator								
Minimum Frequency Operation @ Ct = 1.0 ηF and V_{CC} = 30 V	4	5	6	F_{min}	–	0	–	kHz
Maximum Frequency Operation @ Ct = 1.0 ηF and V_{CC} = 30 V	4	5	6	F_{max}	90	110	125	kHz
Minimum Ct Charging Current (Note 4)	4	5	6	I_{Ct}min	–	0	–	μA
Maximum Ct Charging Current (Note 4)	4	5	6	I_{Ct}max	280	350	420	μA
Discharge Time @ Ct = 1.0 ηF	4	5	6	–	–	500	–	ns
Drive Output								
Output Voltage Rise Time @ C_L = 1.0 ηF (ΔV = 10 V)	7	12	13	t_r	–	30	50	ns
Output Voltage Fall Time @ C_L = 1.0 ηF (ΔV = 10 V)	7	12	13	t_f	–	30	50	ns
Clamped Output Voltage @ V_{CC} = 30 V (Note 5)	7	12	13	V_{DRV}	11	13	16	V
Voltage Drop on the Stage @ V_{CC} = 10 V (Note 5)	12	12	12	V_{DRV}	–	–	0.5	V
Undervoltage Lockout								
Startup Threshold (V_{CC} Increasing)	8	13	14	$UVLO_H$	13.5	15	16.5	V
Minimum Operating Voltage (V_{CC} Decreasing)	8	13	14	$UVLO_L$	6.5	7.2	8.0	V
Startup Current Source								
Maximum Voltage, Pin 1 Grounded	1	1	1	–	–	450	–	V
Maximum Voltage, Pin 1 Decoupled (470 μF)	1	1	1	–	–	500	–	V
Startup Current Source Flowing through Pin 1	1	1	1	–	2.3	3.0	4.8	mA
Leakage Current in Offstate @ Vpin 1 = 500 V	1	1	1	–	–	32	70	μA
Device Current Consumption								
V_{CC} less than $UVLO_H$	8	13	14	–	–	1.5	1.8	mA
V_{CC} = 30 V and Fsw = 2.0 kHz, C_L = 1.0 ηF	8	13	14	–	–	1.2	3.0	mA
V_{CC} = 30 V and Fsw = 125 kHz, C_L = 1.0 ηF	8	13	14	–	–	3.0	4.0	mA
Startup Current to V_{CC} Capacitor	8	13	14	–	1.4	–	–	mA

4. Typical capacitor swing is between 0.5 V and 3.5 V.
5. Guaranteed by design, T_J = 25°C.

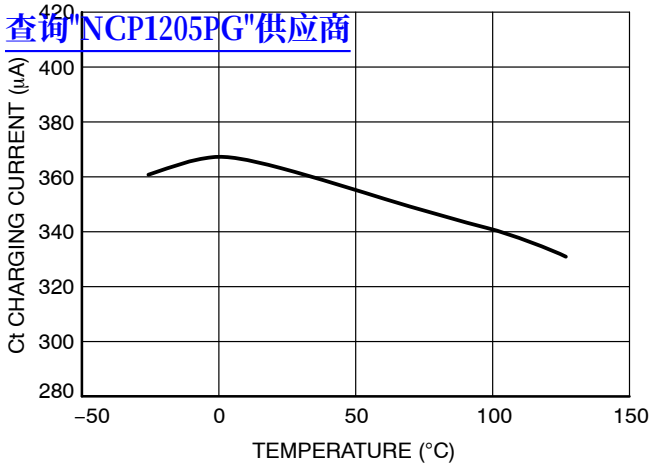


Figure 5. Ct Charging Current versus Temperature

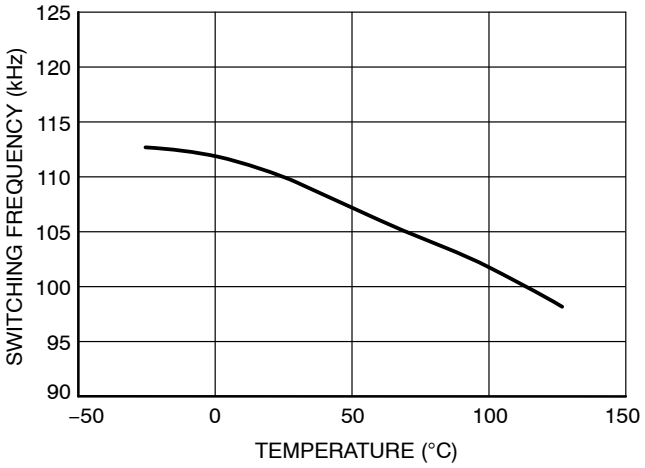


Figure 6. Switching Frequency @ Ct = 1 nF versus Temperature

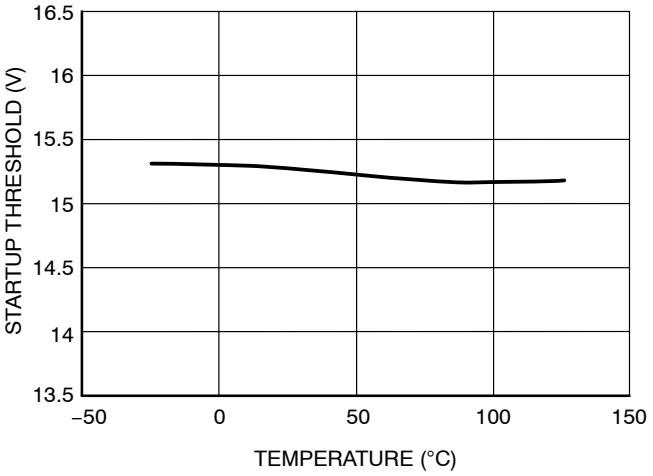


Figure 7. Startup Threshold versus Temperature

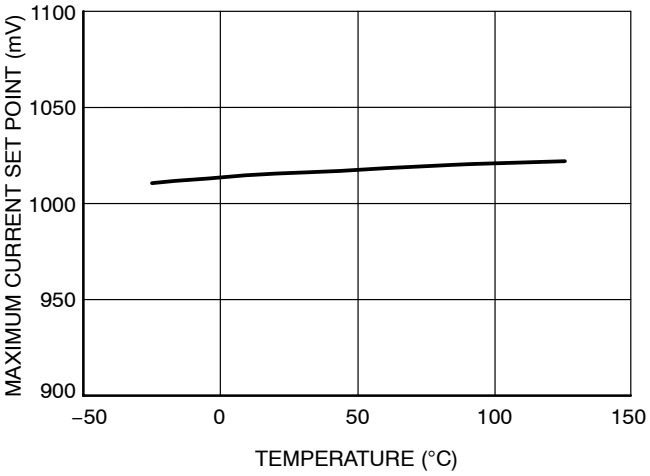


Figure 8. Maximum Current Setpoint versus Temperature

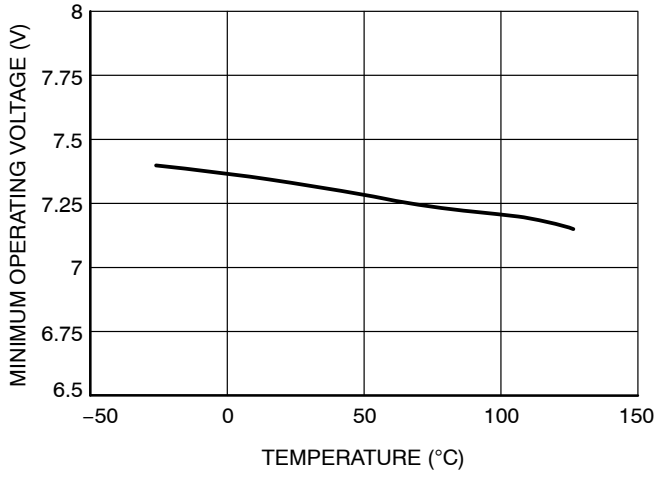


Figure 9. Minimum Operating Voltage versus Temperature

APPLICATION INFORMATION

Introduction

By implementing a unique smooth frequency reduction technique, the NCP1205 represents a major leap toward low−power Switchmode Power Supply (SMPS) integrated management. The circuit combines free−running operation with minimum drain−source switching (so−called valley switching), which naturally reduces the peak current stress as well as the ElectroMagnetic Interferences (EMI). At nominal output power, the circuit implements a traditional current−mode SMPS whose peak current setpoint is given by the feedback signal. However, rather than keeping the switching frequency constant, each cycle is initiated by the end of the primary demagnetization. The system therefore operates at the boundary between Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM). Figure 10 details this terminology:

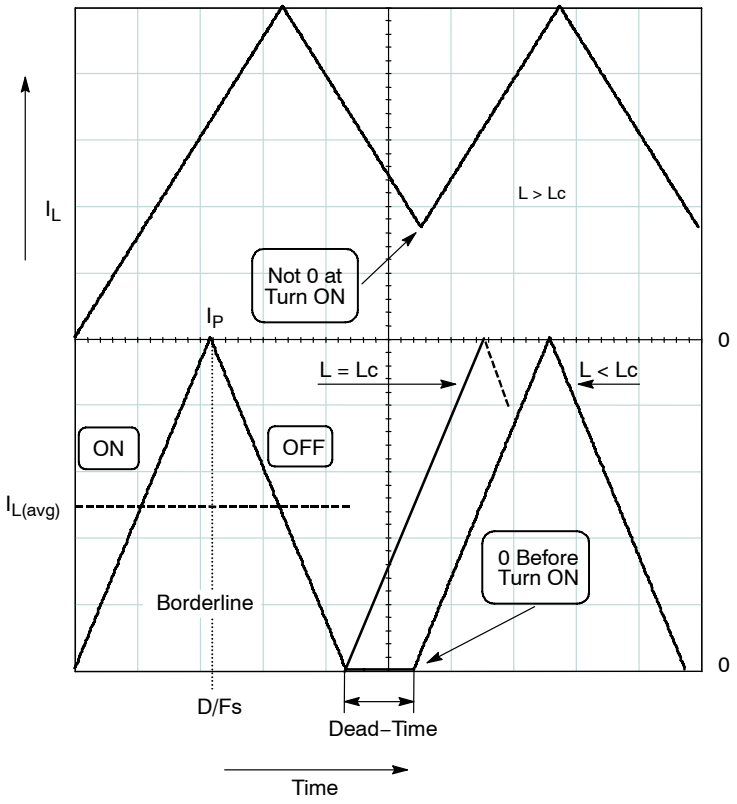


Figure 10. Defining the Conduction Mode, Discontinuous, Continuous and Borderline

When the output power demands decreases, the natural switching frequency raises. As a natural result, switching losses also increase and degrade the SMPS efficiency. To overcome this problem, the maximum switching frequency of the NCP1205 is clamped to typically 125 kHz. When the free running mode (also called Borderline Control Mode, BCM) reaches this clamp value, an internal Voltage−Controlled Oscillator (VCO) takes over and starts to decrease the switching frequency: we are in Variable Frequency Mode (VFM). Please note that during this transition phase, the peak current is not fixed but is still decreasing because the output power demand does. At a given state, the peak current reaches a minimum peak (typically 250 mV/Rsense), and cannot go further down: the switching frequency continues its decrease down to a possible minimum of 0 Hz (the IC simply stops switching). During normal free−running operation and VFM, the controller always ensures single or multiple drain−source valley switching. We will see later on how this is internally implemented.

The FLYBACK operation is mainly defined through a simple formula:

$$Pout = \frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw \qquad \text{(eq. 1)}$$

With:

Lp the primary transformer inductance (also called the magnetizing inductance)

Ip the peak current at which the MOSFET is turned off

Fsw the nominal switching frequency

To adjust the transmitted power, the PWM controller can play on the switching frequency or the peak current setpoint. To refine the control, the NCP1205 offers the ability to play on both parameters either altogether on an individual basis.

In order to clarify the device behavior, we can distinguish the following *simplified* operating phases:

1. The load is at its nominal value. The SMPS operates in borderline conduction mode and the switching frequency is imposed by the external elements (Vin, Lp, Ip, Vout). The MOSFET is turned on at the minimum drain−source level.
2. The load starts to decrease and the free−running frequency hits the internal clamp.
3. The frequency can no longer naturally increase because of the clamp. The frequency is now controlled by the internal VCO but remains constant. The peak current finds no other option that diminishing to satisfy equation (1).
4. The peak current has reached the internal minimum ceiling level and is now frozen for the remaining cycles.
5. To further reduce the transmitted power (V_{FB} goes up), the VCO decreases the switching frequency. In case of output overshoot, the VCO could decrease the frequency down to zero. When the overshoot has gone, V_{FB} diminishes again and the IC smoothly resumes its operation.

Advantages of the Method

By implementing the aforementioned control scheme, the NCP1205 brings the following advantages:

- Discontinuous only operation: in DCM, the Flyback is a first order system (at low frequencies) and thus naturally eases the feedback loop compensation.
- A low−cost secondary rectifier can be used due to smooth turn−off conditions.
- Valley switching ensures minimum switching losses brought by Coss and all the parasitic capacitances.
- By folding back the switching frequency, you turn the system into Pulse Duration Modulation. This method prevents from generating *uncontrolled* output ripple as with hysteretic controllers.
- By letting you control the peak current value at which the frequency goes down, you ensure that this level is low enough to avoid transformer acoustic noise generation even at audible frequencies.

Detailed Description

The following sections describe the internal behavior of the NCP1205.

Free−Running Operation

As previously said, the operating frequency at nominal load is dictated by the external elements. We can split the different switching sections in two separated instants. In the following text we use the internal error voltage, Verr. This level is elaborated in Figure 13. Verr is linked to VFB (pin 4) by the following formula:

$$Verr = 10 - 3 \cdot V_{FB} \qquad \text{(eq. 2)}$$

ON time: The ON time is given by the time it takes to reach the peak current setpoint imposed by the level on FB pin (pin 4). Since this level is internally divided by three, the peak setpoint is simply:

$$Ipk = \frac{1}{3 \cdot Rsense} \cdot Verr \qquad \text{(eq. 3)}$$

The rising slope of the peak current is also dependent on the inductance value and the rectified DC input voltage by:

$$\frac{dIL}{dt} = \frac{Vin_{DC}}{Lp} \qquad \text{(eq. 4)}$$

By combining both equations, we obtain the ON time definition:

$$ton = \frac{Lp}{Vin_{DC}} \cdot Ip = \frac{Lp \cdot V_{ERR}}{Vin_{DC} \cdot 3 \cdot Rsense} \qquad \text{(eq. 5)}$$

OFF time: The time taken by the demagnetization of the transformer depends on the reset voltage applied at the switch opening. During the conduction time of the secondary diode, the primary side of the transformer undergoes a reflected voltage of: [Np/Ns . (Vf + Vout)]. This voltage applied on the primary inductance dictates the time needed to decrease from Ip down to zero:

$$toff = \frac{Lp}{\left[\frac{Np}{Ns} \cdot (Vout + Vf)\right]}$$

$$\cdot Ip = \frac{Lp \cdot Verr}{\left[\frac{Np}{Ns} \cdot (Vout + Vf)\right] \cdot 3 \cdot Rsense} \qquad \text{(eq. 6)}$$

By adding ton + toff, we obtain the natural switching frequency of the SMPS operating in Borderline Conduction Mode (BCM):

$$ton + toff = \frac{Verr \cdot Lp}{3 \cdot Rsense} \cdot \left[\frac{1}{Vin_{DC}} + \frac{1}{\left[\frac{Np}{Ns} \cdot (Vout + Vf)\right]}\right]$$

(eq. 7)

If we now enter this formula into a spreadsheet, we can easily plot the switching frequency versus the output power demand:

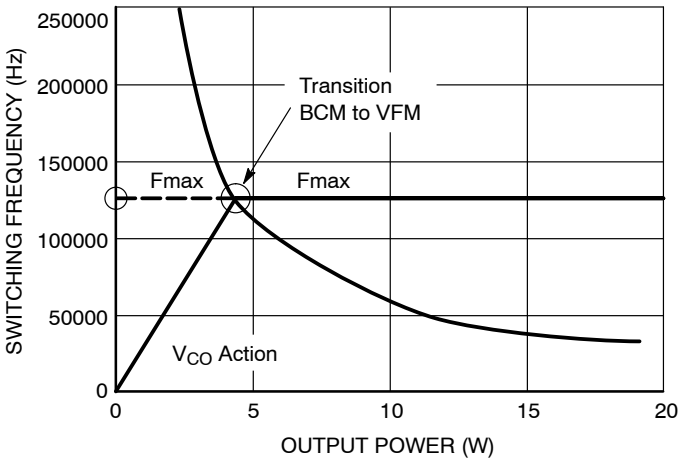


Figure 11. A Typical Behavior of Free Running Systems with a Smooth Frequency Foldback with the NCP1205

The typical above diagram shows how the frequency moves with the output power demand. The components used for the simulation were: Vin = 300 V, Lp = 6.5 mH, Vout = 10 V, Np/Ns = 12.

The red line indicates where the maximum frequency is clamped. At this time, the VCO takes over and decreases the switching frequency to the minimum value.

VCO Operation

The VCO is controlled from the Verr voltage. For Verr levels *above* 1.0 V, the VCO frequency remains unchanged at 125 kHz. As soon as Verr starts to decrease below 1.0 V, the VCO frequency decreases with a typical *small−signal* slope of −175 kHz/mV @ Verr = 500 mV down to zero (typically at FB ≈ 3.3 V). The demagnetization synchronization is however kept when the Toff expands. The maximum switching frequency can be altered by adjusting the Ct capacitor on pin 5. The 125 kHz maximum operation ensures that the fundamental component stays external from the international EMI CISPR−22 specification beginning.

The following drawing explains the philosophy behind the idea:

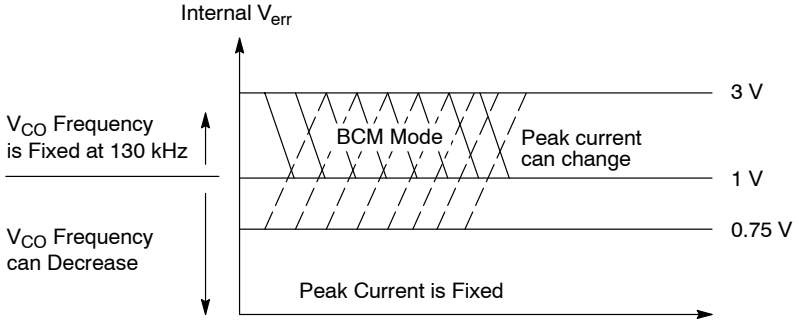


Figure 12. When the Power Demand goes Low, the Peak Current is Frozen and the Frequency Decreases

Zero Crossing Detector

To detect the zero primary current, we make use of an auxiliary winding. By coupling this winding to the primary, we have a voltage image of the flux activity in the core. Figure 10 details the shape of the signal in BCM (L = Lc).

The auxiliary winding for demagnetization needs to be wired in Forward mode. However, the application note describes an alternative solution showing how to wire the winding in Flyback as well. As Figure 13 depicts, when the MOSFET closes, the auxiliary winding delivers (Naux/Np . Vin). At the switch opening, we couple the auxiliary winding to the main output power winding and thus deliver: (−Naux/Ns . Vout). When DCM occurs, the ringing also takes place on the auxiliary winding. As soon as the level crosses−up the internal reference level (65 mV), a signal is internally sent to restart the MOSFET. Three different conditions can occur:

1. In BCM, every time the 65 mV line is crossed, the switch is immediately turned−on. By accounting for the internal Demag pin capacitance (10−15 pF typical), you can introduce a fixed delay, which, combined to the propagation delay, allows to precisely restart in the drain−source valley (minimum voltage to reduce capacitive losses).
2. When the IC enters VFM, the VCO delivers a pulse which is internally latched. As soon as the demagnetization pulse appears, the logic restarts the MOSFET.
3. As can be seen from Figure 13, the parasitic oscillations on the drain are subject to a natural damping, mainly imputed to ohmic losses. At a given point, the demag activity on the auxiliary winding becomes too low to be detected. To avoid any restart problem, the NCP1205 features an internal 4.0 μs timeout delay. This timeout runs after each demag pulse. If within 4.0 μs further to a demag pulse no activity is detected, an internal signal is combined with the VCO to actually restart the MOSFET (synchronized with Ct).

Error Amplifier and Fault Detection

The NCP1205 features an internal error amplifier solely used to detect an overcurrent problem. The application assumes that all the error gain associated with the precise reference level is located on the secondary side of the SMPS. Various solutions can be purposely implemented such as the TL431 or a dedicated circuit like the MC33341. In the NCP1205, the internal OPAMP is used to create a virtual ground permanently biased at 2.5 V (Figure 14), an internal reference level. By monitoring this virtual ground further called V(−), we have the possibility to confirm the good behavior of the loop. If by any mean the loop is broken (shorted optocoupler, open LED etc.) or the regulation cannot be reached (true output short−circuit), the OPAMP network is adjusted in order to no longer be able to ensure the 2.5 V virtual point V(−). If V(−) passes down the 1.5 V level (e.g. output shorted) for a time longer than 128 ms, then the pulses are stopped for 8 x 128 ms. The IC enters a kind of burst mode with bunch of pulses lasting 128 ms and repeating every 8 x 128 ms. If the loop is restored within the 8 x 128 ms period, then the pulses are back again on the output drive (synchronized with $UVLO_H$).

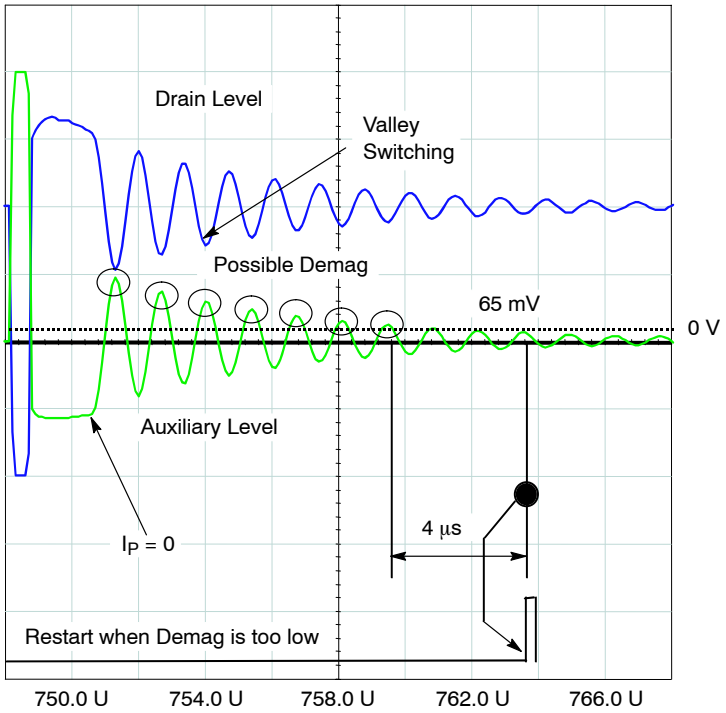


Figure 13. Core Reset Detection is done through an Auxiliary Winding Operated in Forward

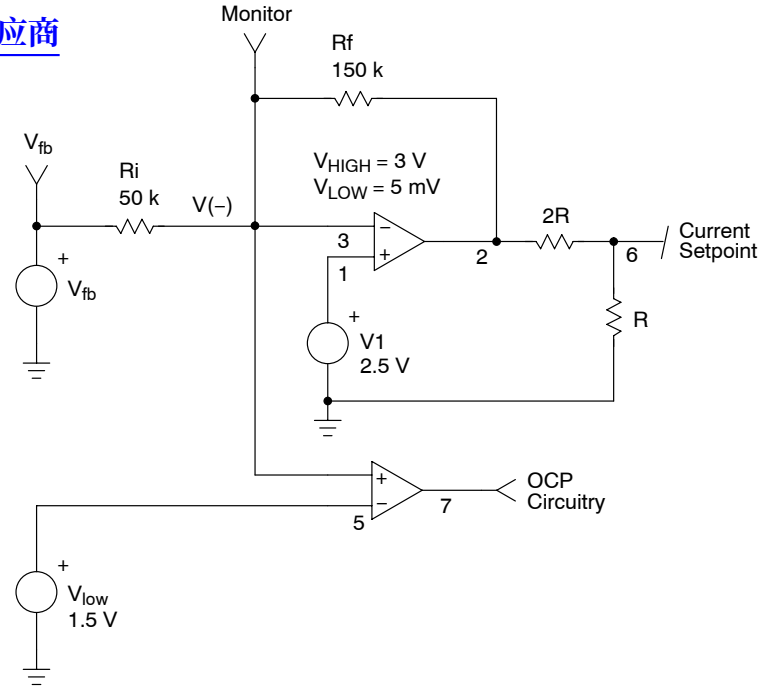


Figure 14. This Typical Arrangement Allows for an Easy Fault Detection Management

To illustrate how the system reacts to a variable FB level, we have entered the above circuit into a SPICE simulator and observed the output waveforms. When FB is within regulation, the error flag is low. However, as soon as FB leaves its normal operating area, the OPAMP can no longer keep the V(−) point and either goes to the positive top or down to zero: the error flag goes high.

Because of the large amount of delay necessary for this 128 ms operation, the capacitor used for the timing is Ct, connected from ground to pin 5. In normal VFM operation, this timing capacitor serves as the VCO capacitor and the error management circuit is transparent. As soon as an error is detected (error flag goes high), an internal switch routes Ct to the 128 ms generator. As a first effect, the switching frequency is no longer controlled by the VCO (if the error appears during VFM) and the system is relaxed to natural BCM. The capacitor now ramps up and down to be further divided and finally create the 128 ms delay.

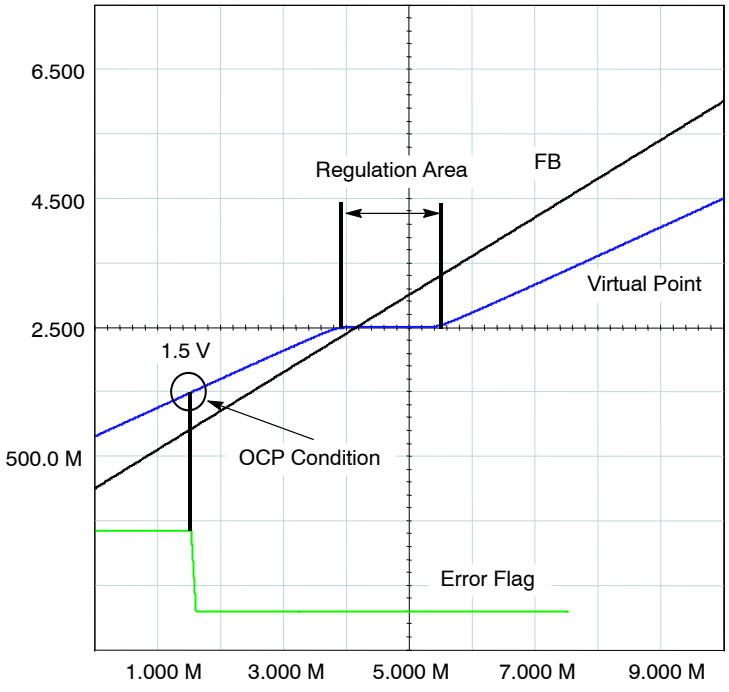


Figure 15. By Monitoring the Internal Virtual Ground, the System can Detect the Presence of a Fault

As soon as the system recovers from the error, e.g. FB is back within its regulation area, the IC operation comes back to normal.

To avoid any system thermal runaway, another internal 8 x 128 ms delay is combined with the previous 128 ms. It works as follows: the 128 ms delay is provided to account for any normal transients that engender a temporary loss of feedback (FB goes toward ground). However, when the 128 ms period is actually over (the feedback is definitively lost) the IC stops the output driving pulses for a typical period of 8 x 128 ms. During this mode, the rest of the functions are still activated. For instance, in lack of pulses, the self−supplied being no longer provided, the startup source turns on and off (when reaching the corresponding $UVLO_L$ and $UVLO_H$ levels), creating an hiccup waveform on the Vcc line. As soon as the feedback condition is restored, the 8 x 128 ms is interrupted and, in synchronism with the Vcc line, the IC is back to normal. The following diagrams show how this mechanism takes place when FB is down to zero (optocoupler opened) or up to Vcc (optocoupler shorted). If we assume that the error is permanently present, then a burst mode takes place with a 128/8 x 128 = 12.5% duty−cycle. The real transmitted power is thus:

$$Pout_{BURST} = \frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw \cdot Duty_{BURST}$$

Overvoltage Detection (OVP)

On the PDIP−14 and the SOIC−16 versions, an OVP pin allows to shutdown the controller as soon as the level on this pin exceeds 2.8V, as detailed in Figure 16. In lack of switching pulses, the Vcc capacitor is no longer refreshed by the auxiliary supply and slowly discharges toward ground. When the Vcc level crosses UVLOL, a new startup sequence occurs. If the OVP has gone, the converter resumes its operation.

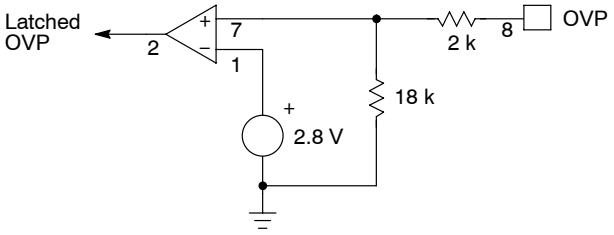


Figure 16. In the PDIP−8 Version, the OVP Pad is not Pinned Out and is Available with PDIP−14 Devices Only

Protecting Pin 1 Against Negative Spikes

As any CMOS controller, NCP1205 is sensitive to negative voltages that could appear on it's pins. To avoid any adverse latch−up of the IC, we strongly recommend inserting a 15 k resistor in series with pin 1 and the high−voltage rail, as shown in Figures 17 and 18. This 15 k resistor prevents from adversely latching the controller in case of negative spikes appearing on the bulk capacitor during the power−off sequence. Please note that this resistor does not dissipate any continuous power and can therefore be of low power type. Two 8.2 k can also be wired in series to sustain the large DC voltage present on the bulk.

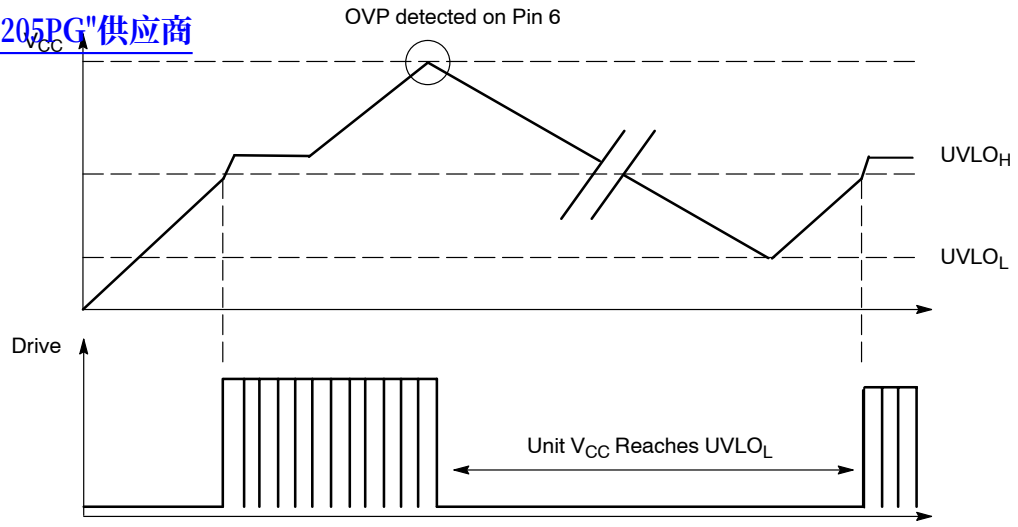


Figure 17. When the V_{CC} Voltage Goes Above the Maximum Value, the Device Enters Safe Burst Mode

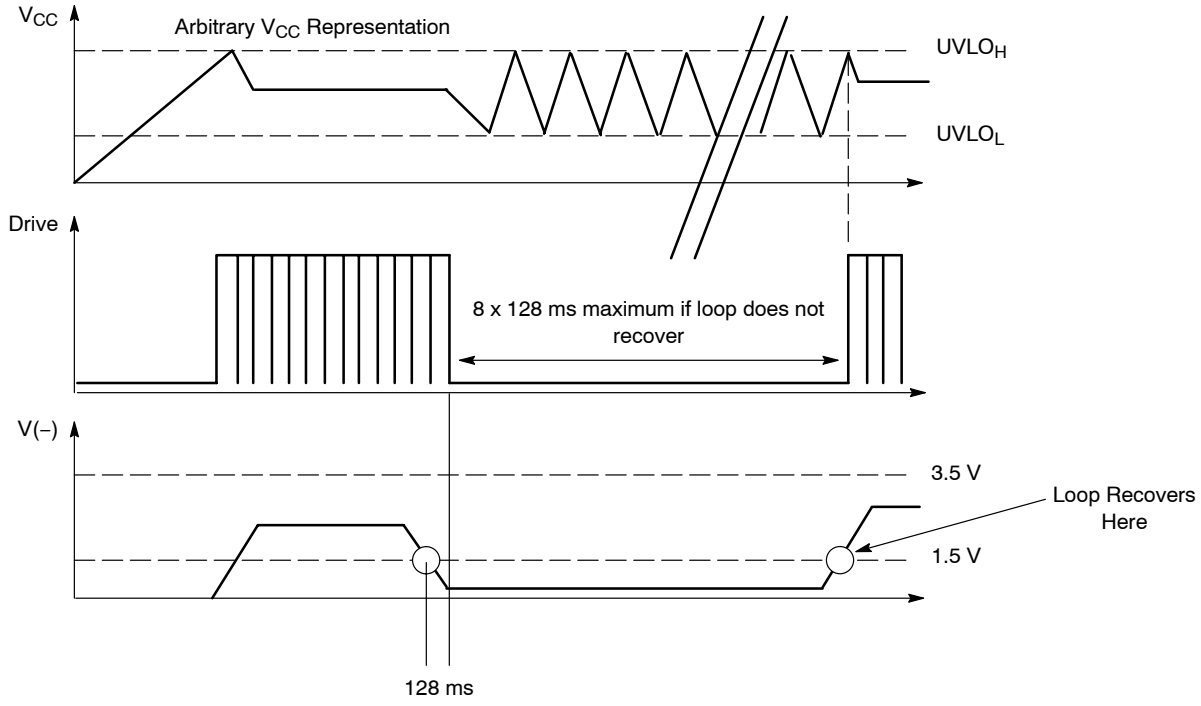
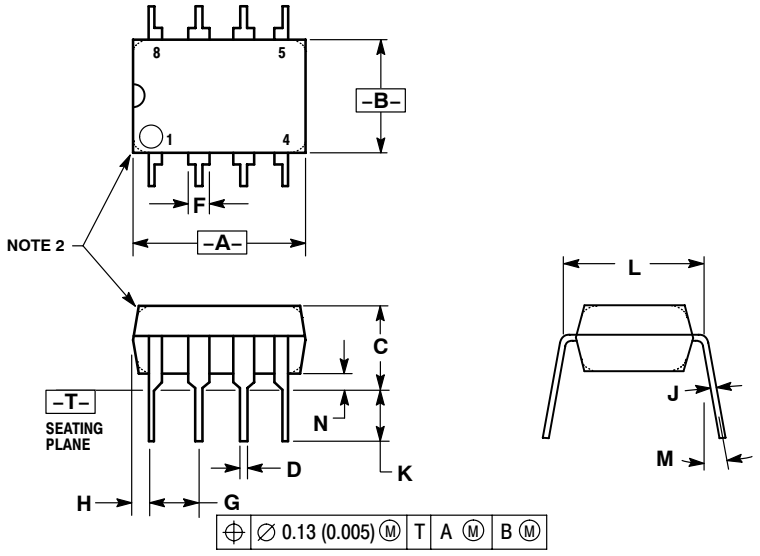


Figure 18. When the Internal V(−) Passes Below 1.5 V, the IC Senses a Short−Circuit Event

PACKAGE DIMENSIONS

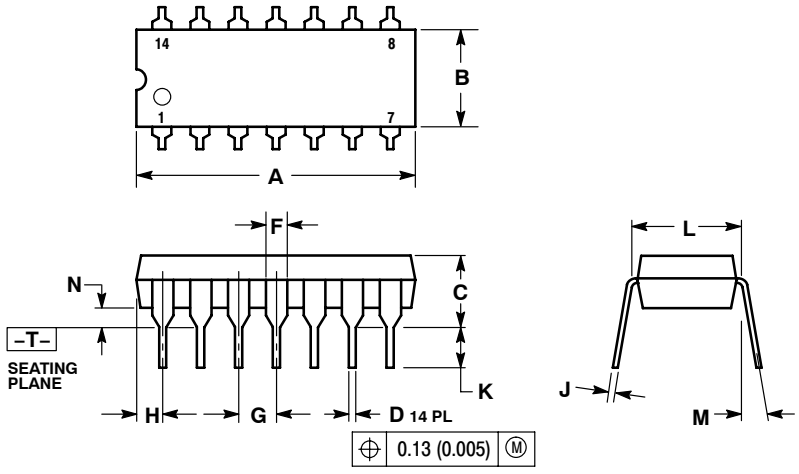
PDIP−8
N SUFFIX
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

PDIP−14
CASE 646−06
ISSUE P

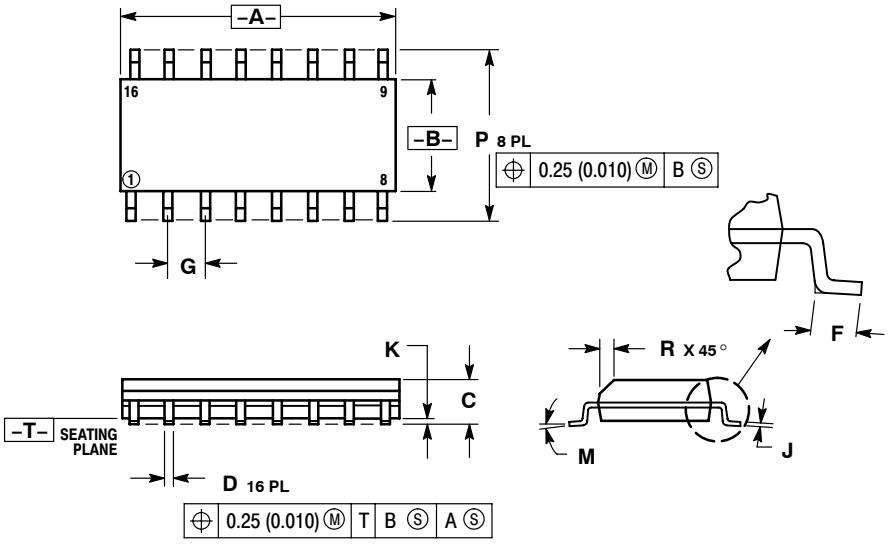


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

PACKAGE DIMENSIONS

SOIC−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative