

# MRFIC1505A Integrated GPS Downconverter

## 1.575 GHz GPS DOWNCONVERTER

This integrated circuit is intended for GPS receiver applications. The dual conversion design is implemented in Freescale's low-cost, high-performance MOSAIC 5. silicon bipolar process and is packaged in a low-cost surface mount LQFP-48 package. In addition to the mixers, a VCO, PLL, Crystal Oscillator, A/D converter and a loop filter are integrated on-chip. Output IF is nominally 4.1 MHz.

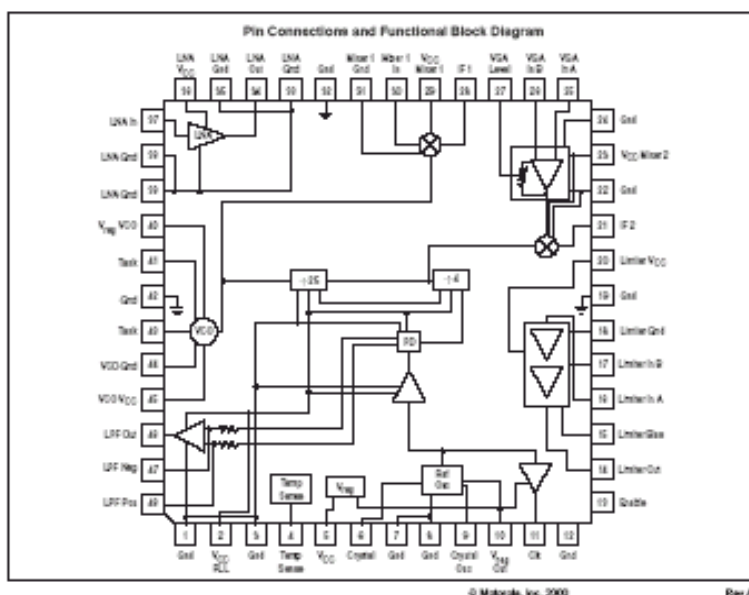
- 105 dB Typical Conversion Gain
- 2.7 V Operation
- 28 mA Typical Current Consumption
- Low-Cost, Low-Profile Plastic LQFP Package

### Ordering Information

Device	Operating Temperature Range	Package
MRFIC1505R2	$T_A = -40$ to $85^\circ\text{C}$	LQFP-48



Plastic Package  
Case 932  
(LQFP-48)



## Maximum Ratings

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}$	5.0	Vdc
DC Supply Current	$I_{DD}$	60	mA
Operating Ambient Temperature	$T_A$	-40 to 85	°C
Storage Temperature Range	$T_{stg}$	-65 to 150	°C
Lead Soldering Temperature Range	—	260	°C

**Note:** Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the limits in the Electrical Characteristics tables.

## Electrical Characteristics (VCC = 2.7 to 3.3 V; TA = -40 to 85°C; Enable = 2.7 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Total Device</b>					
Supply Voltage	$V_{CC}$	2.7	3.0	3.3	V
Supply Current (TA = 25°C, VCC = 2.7 V, Enable = 2.7V)	$I_{CC}$	—	28	36	mA
Supply Current (TA = 25°C, VCC = 2.7 V, Enable = 2.7V)	$I_{CC}$	—	2.0	4.0	mA
<b>RF Amplifier</b>					
RF Input Frequency	$f_{in}$	—	1575.42	—	MHz
Input Impedance	$Z_{in}$	—	50	—	$\Omega$
Input VSWR	$VSWR_{in}$	—	2.0	—	—
Gain	G	13	15	—	dB
Noise Figure	NF	—	2.0	—	dB
1.0 dB Compression (Measured at Output)	$P_{1dB}$	—	1.0	—	dBm
<b>First Mixer</b>					
Input Frequency	$f_{in}$	—	1575.42	—	MHz
Gain	G	10	14	—	dB
Noise Figure	NF	—	13	—	dB
1.0 dB compression (Measured at Output)	$P_{1dB}$	—	-13	—	dBm
First Local Oscillator Frequency	$f_{LO1}$	—	1636.8	—	MHz
First Intermediate Frequency	$f_{IF1}$	—	61.38	—	MHz
LO Leakage at IF Port	—	—	-40	—	dBm
LO Leakage at RF Port	—	—	-50	—	dBm
Output Impedance	$Z_{out}$	—	50	—	$\Omega$
<b>First IF Amplifier and Second Mixer</b>					
Input Frequency	$f_{in}$	—	61.38	—	MHz
Input Impedance	$Z_{in}$	—	230	—	$\Omega$
Output Impedance	$Z_{out}$	—	50	—	$\Omega$
Second Local Oscillator Frequency	$f_{LO2}$	—	65.47	—	MHz
Second Intermediate Frequency	$f_{IF2}$	—	4.092	—	MHz
LO Leakage at IF Port	—	—	-40	—	dBm
Gain	G	40	43	—	dB
Cascaded Noise Figure	NF	—	9.3	—	dB
1.0 dB Compression Point (Measured at Output)	$P_{1dB}$	—	-13	—	dBm
<b>Limiting Amplifier</b>					
Second Intermediate Frequency	$f_{IF2}$	—	4.092	—	MHz
Input Signal Level	—	4.0	11	31	Mv
Output Voltage Swing (into 10 pF    100 k $\Omega$ )	$V_{out}$	800	—	—	mVpp
DC Output Level	—	—	1.4	—	V
Gain	G	—	50	—	dB
<b>Reference Oscillator</b>					
Reference Frequency	$f_r$	—	16.368	—	MHz
Reference Frequency Input Level (Crystal Output Pin)	—	—	500	—	mVpp
Reference Oscillator Output Voltage Level (Into 15 pF    10 k $\Omega$ )	—	750	—	—	mVpp

# Electrical Characteristics (V<sub>CC</sub> = 2.7 to 3.3 V; TA = –40 to 85°C; Enable = 2.7 V unless otherwise noted)

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Characteristic	Symbol	Min	Typ	Max	Unit
Reference Oscillator Output Voltage Level (Into 15 pF    10kΩ)	–	750	–	–	mVpp
Reference Clock Input Drive Level	–	400	800	1500	mVpp

## PLL

First Local Oscillator Frequency	f <sub>LO1</sub>	–	1636.8	–	MHz
Second Local Oscillator Frequency	f <sub>LO2</sub>	–	65.47	–	MHz
VCO C/N (at 10 kHz Offset)	–	–	-80	–	dBc/Hz
VCO Gain (TBD Varactor)	–	–	200	–	MHz/V

## Enable

Enable Active Level	–	0.8 x V <sub>CC</sub>	V <sub>CC</sub>	–	V
Disable Active Level	–	–	0	0.2 x V <sub>CC</sub>	V

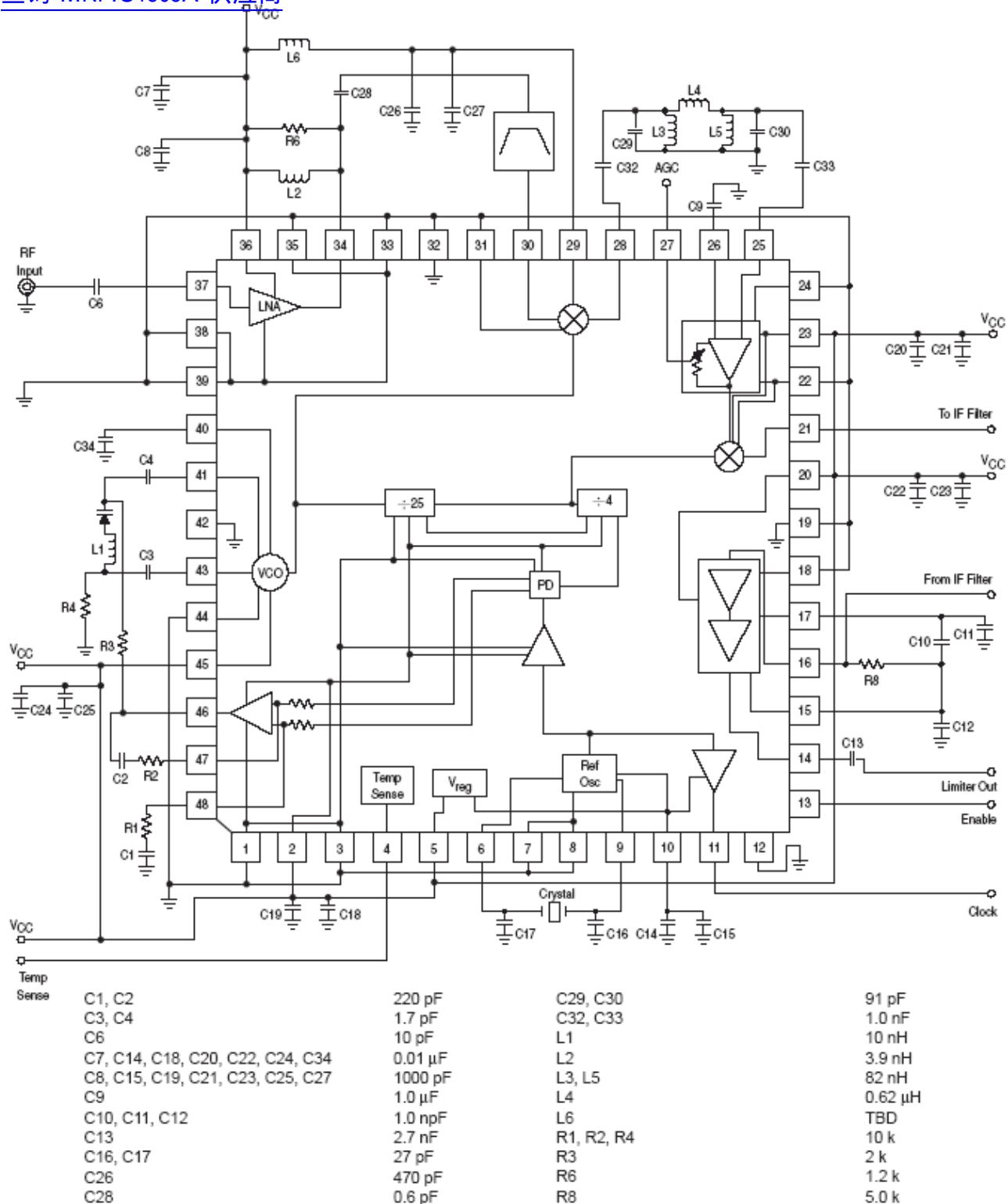
## Voltage Regulator

Regulator Output Voltage (V <sub>CC</sub> = 2.7 to 3.3 V, I <sub>out</sub> = 3.0 mA)	V <sub>O</sub>	2.1	2.3	2.5	V
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## Temperature Sense

Temperature Sensor Output Voltage @ 25°C	–	1.270	1.395	1.463	V
Temperature Sensor Slope over Temperature	–	–	5.0	–	mV/°C

MRFIC1505A does not meet AEC100 specifications for ESD. The AEC method zapping of the plastic packaged device with both positive and negative polarity pulses resulted in failures at 200 V, 500 V, 1 KV, 1.5 KV, 2 KV, and 2.5 KV HBM, as well as 100 V, 150 V, and 200 V MM. The primary failure mode for these zap levels is the Reference Oscillator. The 1505 device can withstand discharges up to 150 V HBM and 40 V MM.

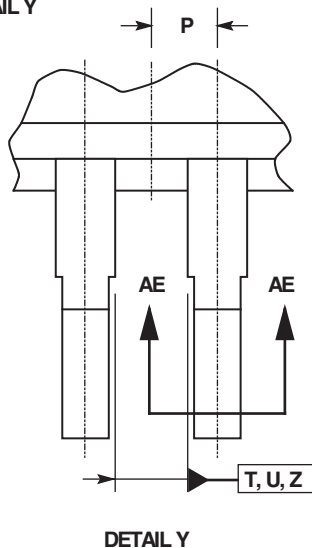
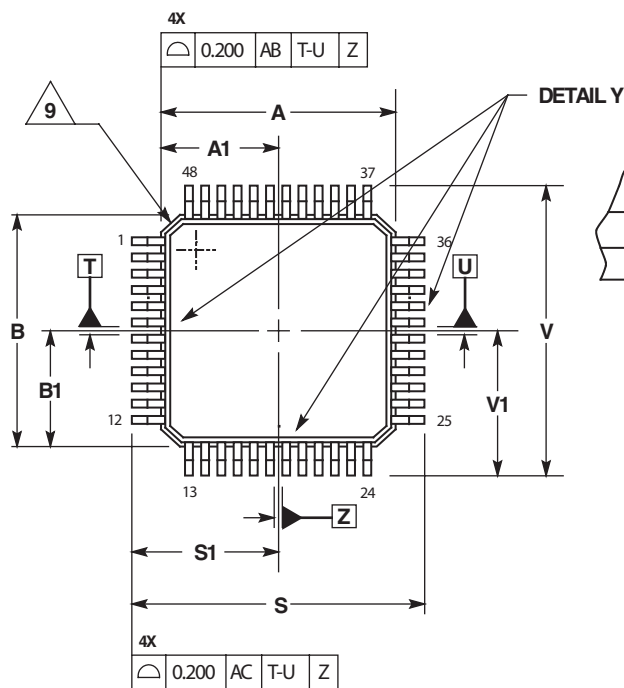


NOTES: 1. R8 must be set to match your 2nd IF filter impedance.  
2. Layout of capacitors C10, C11, C12 is critical for stability of Limiter.

Figure 1 Applications Schematic (1636.8 MHz LO)

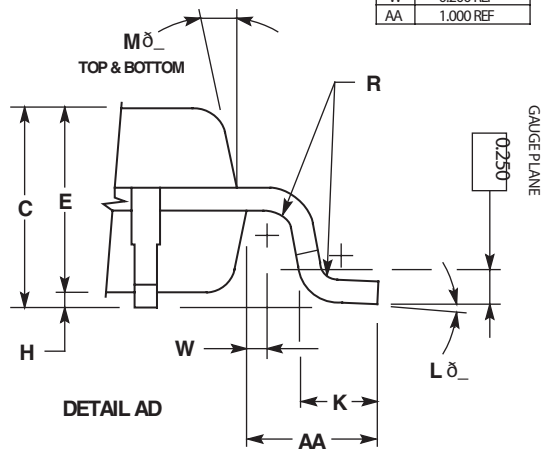
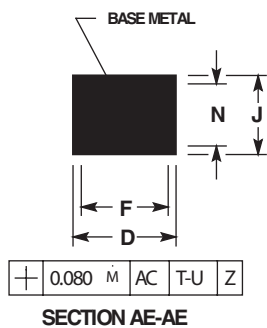
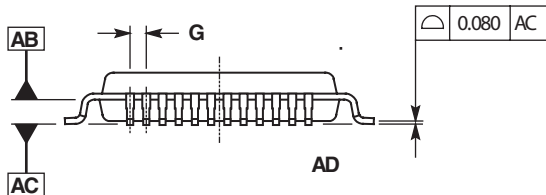
# Outline Dimensions

PLASTIC PACKAGE  
CASE 932-03  
(LQFP-48)  
ISSUE F



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5.
  2. DIMENSION A1 IS THE MINIMUM DIMENSION OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM AND TOP.
  3. DIMENSION A1 IS TO BE DETERMINED AT THE MINIMUM DIMENSION OF LEAD.
  4. DIMENSION B1 IS TO BE DETERMINED AT THE MINIMUM DIMENSION OF LEAD.
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MILLIMETERS		
DIM	MIN	MAX
A	7.000	BSC
A1	3.500	BSC
B	7.000	BSC
B1	3.500	BSC
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500	BSC
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0.000	0.000
M	12.000	REF
N	0.090	0.160
P	0.250	BSC
R	0.150	0.250
S	9.000	BSC
S1	4.500	BSC
V	9.000	BSC
V1	4.500	BSC
W	0.200	REF
AA	1.000	REF



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## NOTES

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