

MOS FIELD EFFECT TRANSISTOR

2SK3992

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3992 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3992	TO-251 (MP-3)
2SK3992-ZK	TO-252 (MP-3ZK)

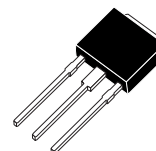
FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 4.8 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 32 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2900 \text{ pF TYP.}$
- 5 V drive available

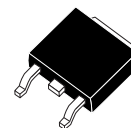
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	25	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 64	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 256	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	38	W
Total Power Dissipation	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	33	A
Single Avalanche Energy ^{Note2}	E_{AS}	109	mJ

(TO-251)



(TO-252)



Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 12.5 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

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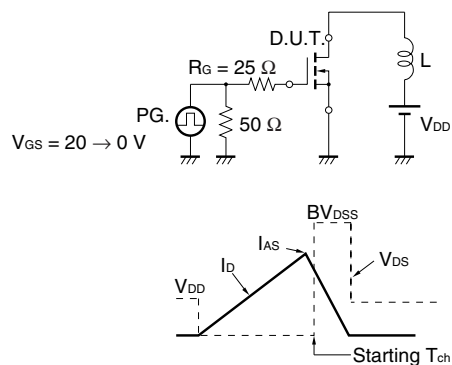
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

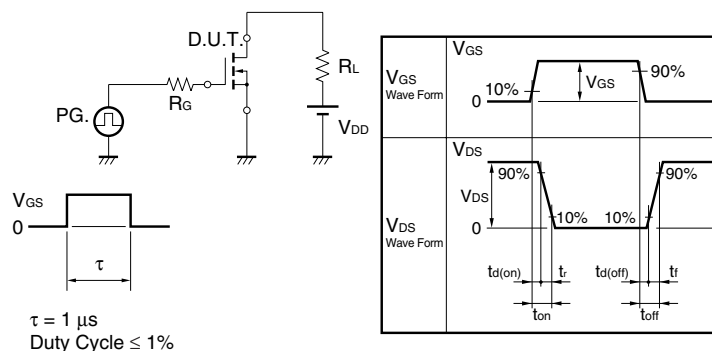
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 25 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.0	2.5	3.0	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 16 A	12			S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 32 A		3.4	4.8	mΩ
	R _{DS(on)2}	V _{GS} = 5.0 V, I _D = 16 A		5.9	10.8	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		2900		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		640		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		440		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 12.5 V, I _D = 32 A		21		ns
Rise Time	t _r	V _{GS} = 10 V		26		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		69		ns
Fall Time	t _f			32		ns
Total Gate Charge	Q _G	V _{DD} = 20 V		56		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		11		nC
Gate to Drain Charge	Q _{GD}	I _D = 64 A		19		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 64 A, V _{GS} = 0 V		0.94		V
Reverse Recovery Time	t _{rr}	I _F = 64 A, V _{GS} = 0 V		38		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		44		nC

Note Pulsed

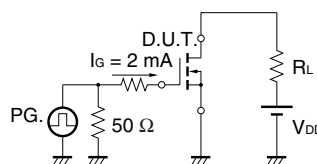
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

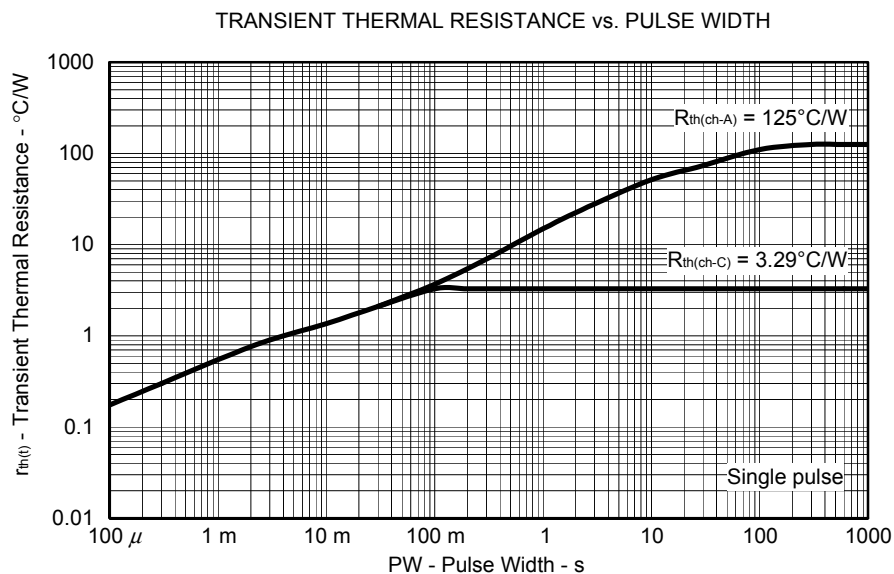
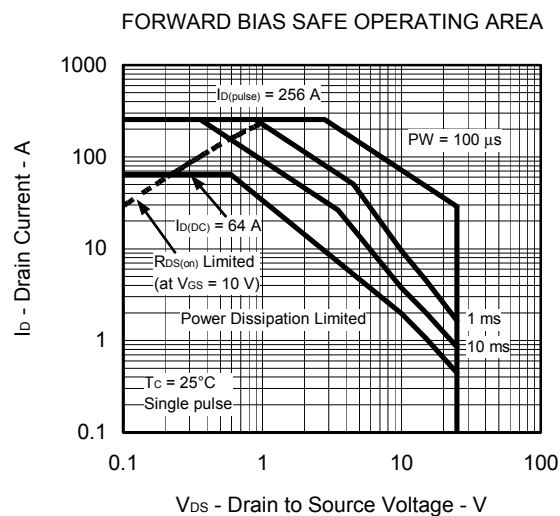
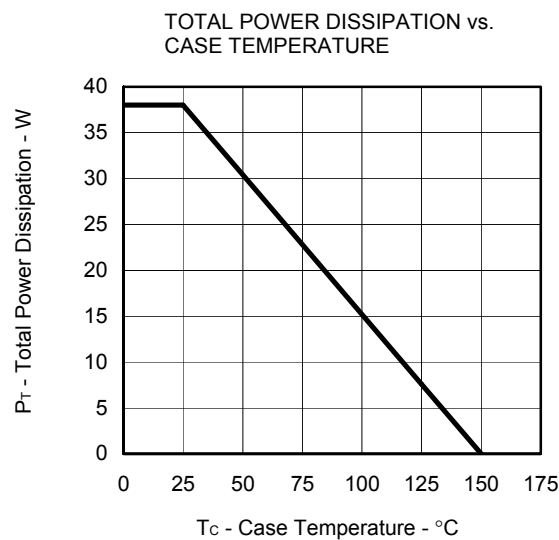
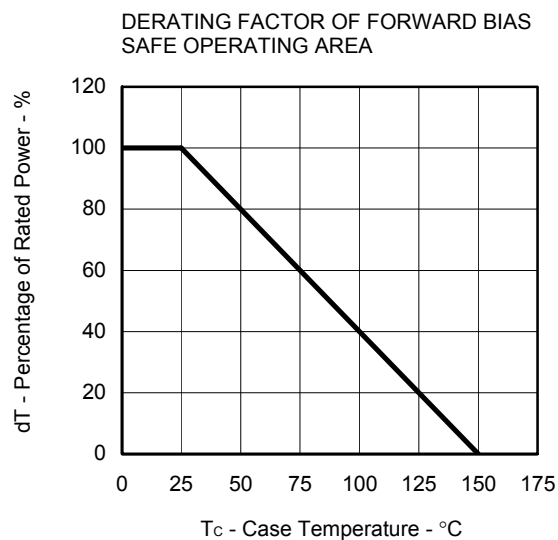


TEST CIRCUIT 3 GATE CHARGE



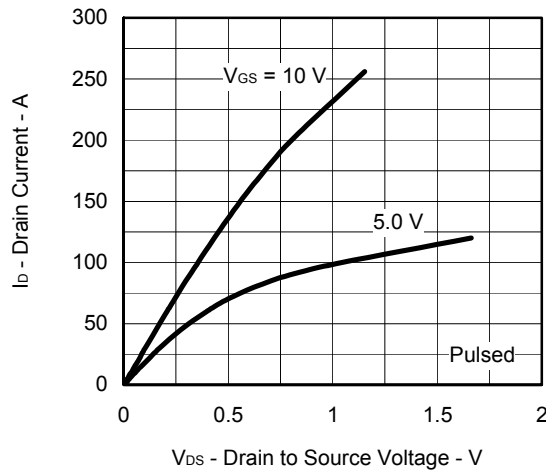
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TYPICAL CHARACTERISTICS (T_A = 25°C)

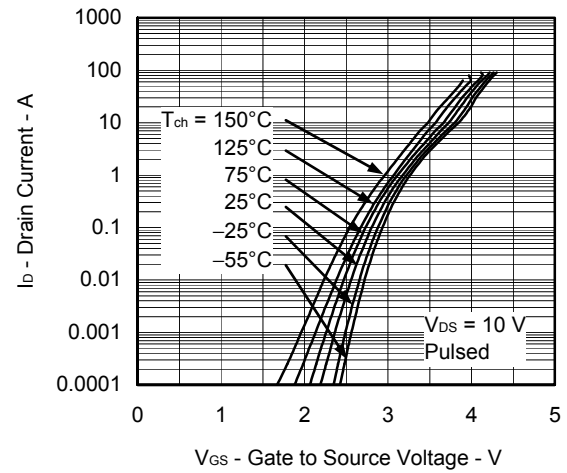


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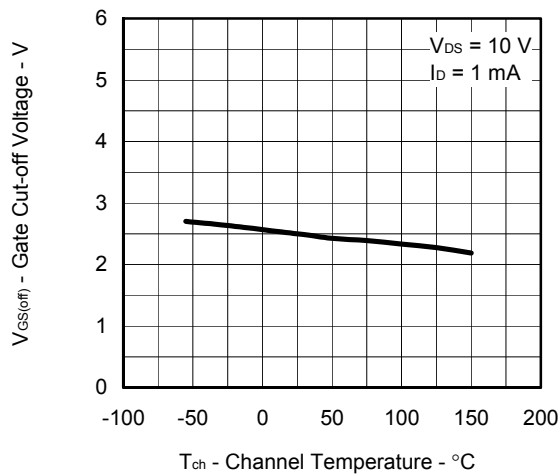
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



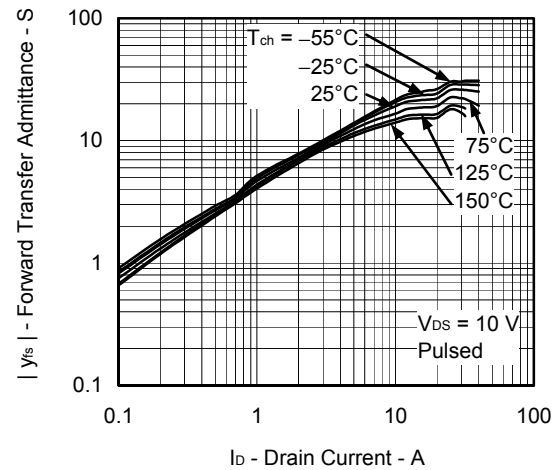
FORWARD TRANSFER CHARACTERISTICS



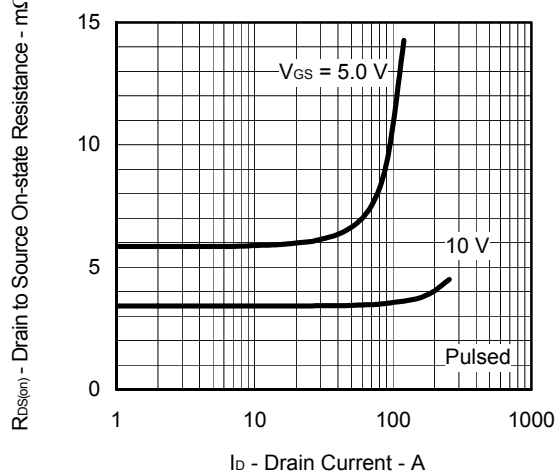
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



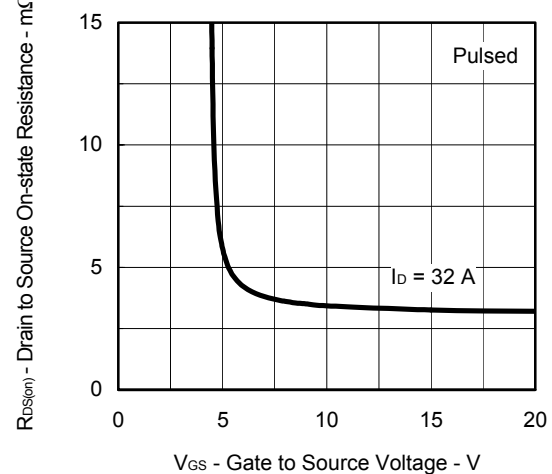
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT

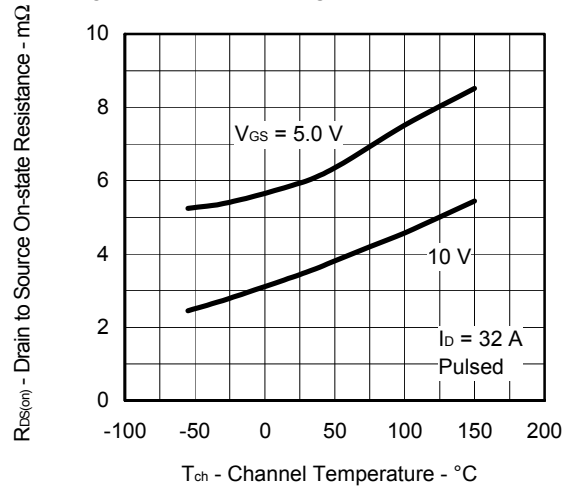


DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE

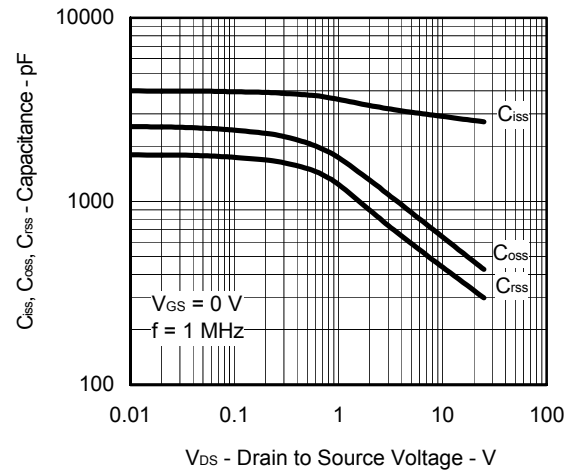


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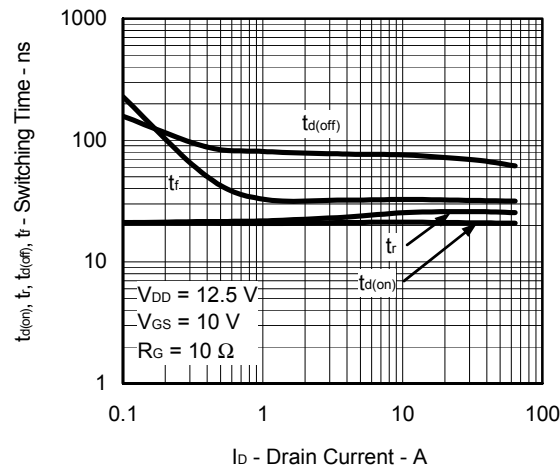
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



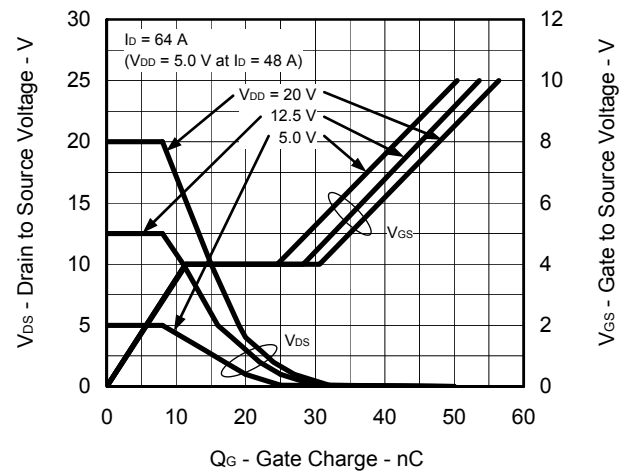
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



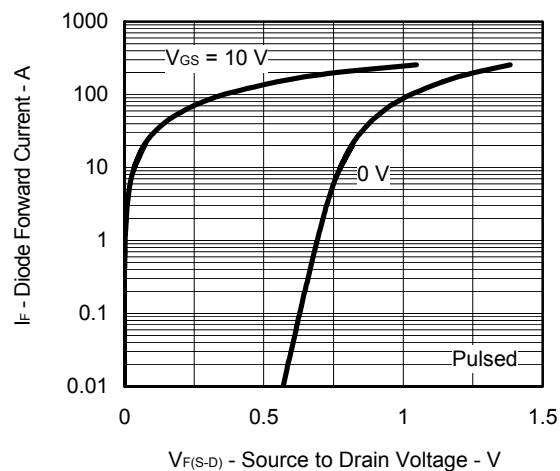
SWITCHING CHARACTERISTICS



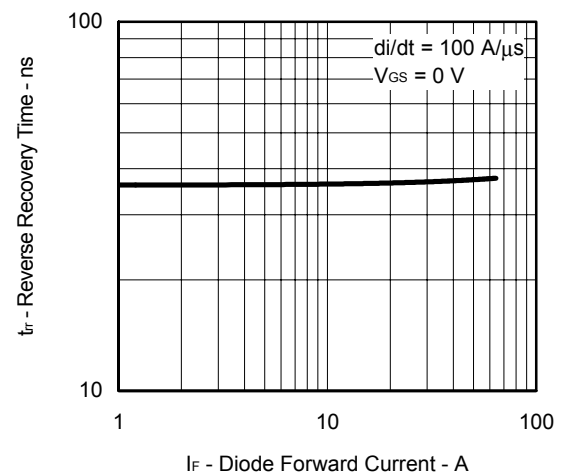
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

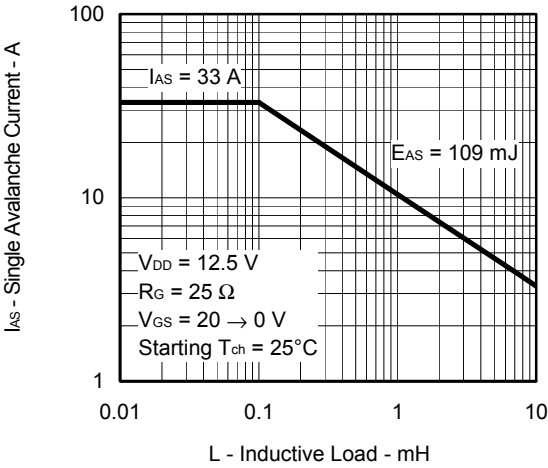


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

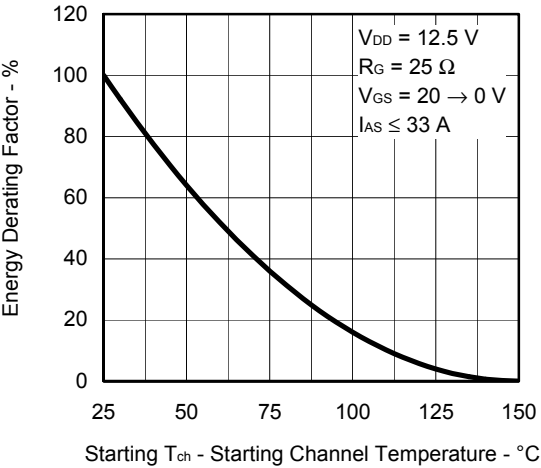


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SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



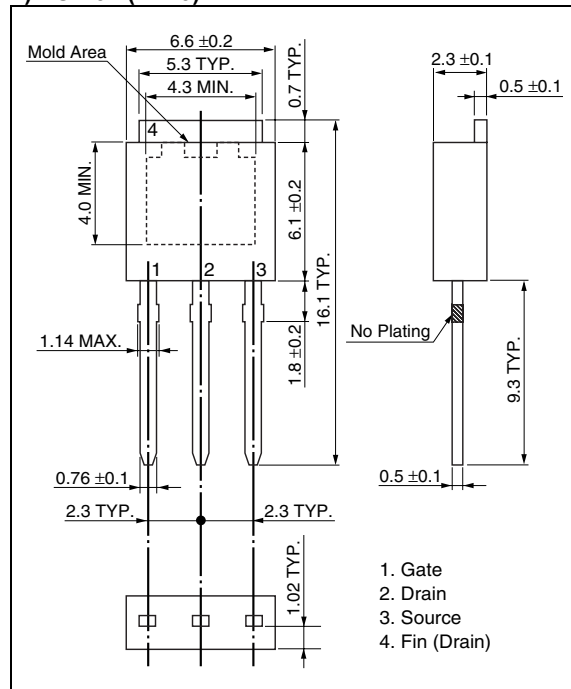
SINGLE AVALANCHE ENERGY
DERATING FACTOR



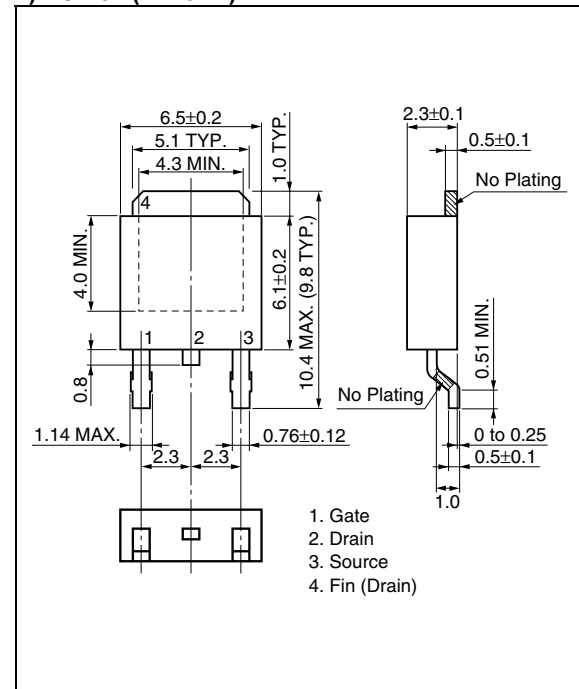
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PACKAGE DRAWINGS (Unit: mm)

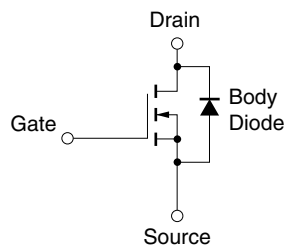
1) TO-251 (MP-3)



2) TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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