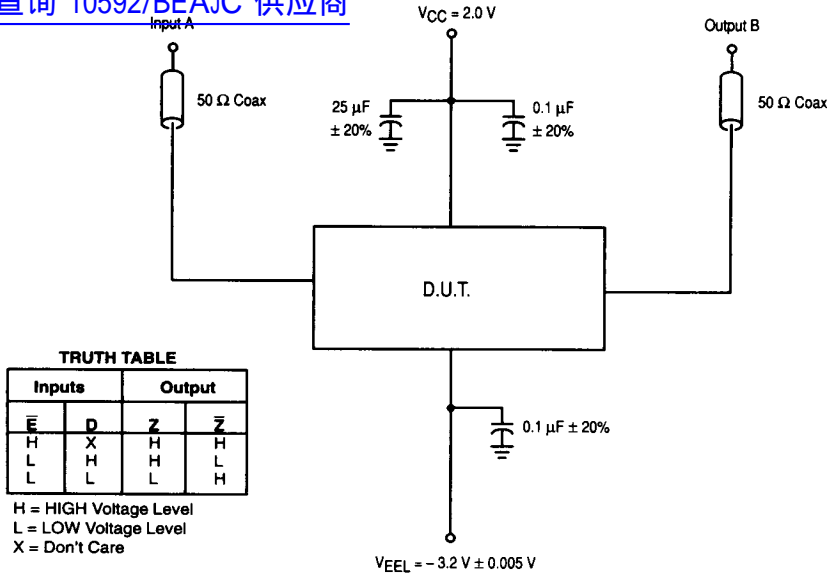


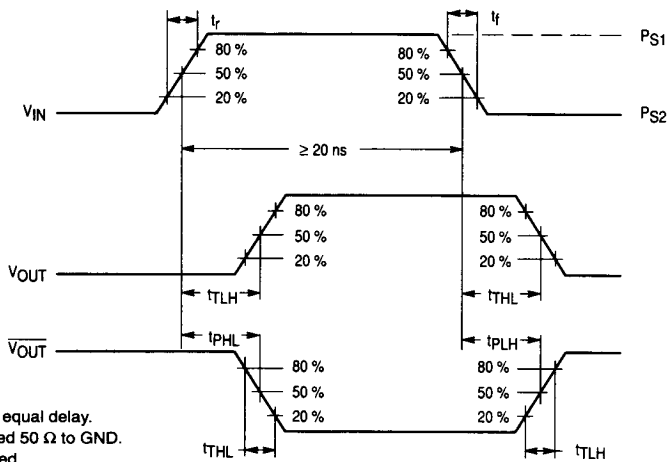
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TRUTH TABLE

Inputs		Output	
\bar{E}	D	Z	\bar{Z}
H	X	H	H
L	H	H	L
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care



NOTES

- L1 = L2: Matched for equal delay.
- All other outputs loaded 50 Ω to GND.
- 2:1 divider may be used.
- V_{IN} has the following characteristics:
 - pulse width ≥ 20 ns.
 - frequency = 1.0 MHz.
 - t_r and t_f = 2.0 ns ± 0.2 ns.

Figure 1. Switching Test Circuit and Waveforms

10592 QUIESCENT LIMIT TABLE *

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Test Temperature	Test Voltage Values (Volts)											
	V _{IH}	V _{IL}	V _{IH1}	V _{IL1}	PS1	PS2	VEE (MIN)	VEE (MAX)	VEE (Nom)	BVO	V _{LK}	V _{OLS}
T _A = 25 °C	-0.780	-1.85	-1.105	-1.475	-0.89	-1.69	-5.72	-4.68	-5.2	+5.095	-1.850	-2.4
T _A = 125 °C	-0.630	-1.82	-1.000	-1.400	-0.78	-1.655	-5.72	-4.68	-5.2	+4.960	-1.825	-2.4
T _A = -55 °C	-0.880	-1.92	-1.255	-1.510	-0.97	-1.715	-5.72	-4.68	-5.2	+4.960	-1.89	-2.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
		+25 °C		+125 °C		-55 °C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = GND, Output Load = 50 Ω to GND, V _L R = 270 Ω to +5.5 V							
		Subgroup 1		Subgroup 2		Subgroup 3			V _{IH}	V _{IL}	V _{IH1}	V _{IL1}	V _L R	V _{OLS}	V _{EE}	V _{CC}
V _{OH}	High Output Voltage	-0.10	+0.10	-0.10	+0.10	-0.15	+0.05	V	5, 6, 10, 11	5, 6, 10, 11			8	16	1-4, 12-15	
V _{OL}	Low Output Voltage	-0.90	-0.70	-0.95	-0.70	-0.85	-0.60	V	5, 6, 10, 11	5, 6, 10, 11			8	16	1-4, 12-15	
V _{OLC}	Low Output Voltage	-0.90	-0.70	-0.95	-0.70	-0.85	-0.60	V	5, 6, 10, 11	5, 6, 10, 11			8	16	1-4, 12-15	
V _{OHC}	High Output Voltage	-0.10	+0.10	-0.10	-0.10	-0.15	+0.05	V	5, 6, 10, 11	5, 6, 10, 11			8	16	1-4, 12-15	
I _{IH1}	Input Current High		220		350		350	μA	5-7, 9-11				8	16	5-7, 9-11	
I _{IL}	Input Current Low	0.5		0.3		0.5		μA	5-7, 9-11				8	16	5-7, 9-11	
I _{OV}	Short Circuit Current (No Output Voltage)		104.4		102.2		102.2	mA			1-4, 12-15		8	16	1-4, 12-15	
I _{OS}	Output Short Circuit Current	34.1		34.7		-34.7		mA	5, 6, 10, 11				8	16	1-4, 12-15	
I _{QOFF}	Open Collector Input Current		500		500		500	μA	2, 7, 9, 14, 15				8	16	2, 7, 9, 14, 15	
I _{EE}	Power Supply Drain Current	-140		-154		-154		mA					8	16	8	

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to Gnd.

10592
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)											
	V _{IH}	V _{IL}	V _{IH1}	V _{IL1}	PS1	PS2	VEE (MIN)	VEE (MAX)	VEE (Nom)	BVO	V _{LK}	VOLS
T _A = 25 °C	-0.780	-1.85	-1.105	-1.475	-0.89	-1.69	-5.72	-4.68	-5.2	+5.085	-1.850	-2.4
T _A = 125 °C	-0.630	-1.82	-1.000	-1.400	-0.78	-1.655	-5.72	-4.68	-5.2	+4.960	-1.825	-2.4
T _A = -55 °C	-0.880	-1.92	-1.255	-1.510	-0.97	-1.715	-5.72	-4.68	-5.2	+4.960	-1.89	-2.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = GND, Output Load = 50 Ω to GND					
		Subgroup 9	Subgroup 10	Subgroup 9	Subgroup 10	Subgroup 11	Subgroup 11		VIN	VOUT	VCC	VEEL	PS1	P. U. T.
t _{TLH}	Rise Time	0.5	3.3	0.5	4.7	0.5	3.8	ns	6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 - 15
t _{FHL}	Fall Time	0.5	3.3	0.5	4.7	0.5	3.8	ns	6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 - 15
t _{PLH} t _{PHL}	Propagation Delay Data	1.5	4.5	1.5	5.6	1.5	5.3	ns	6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 - 15
t _{PLH} t _{PHL}	Propagation Delay Enable	2.0	6.0	1.0	9.0	1.0	6.0	ns	6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 - 15

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to Gnd.