

Quad Bus Priver供应商

ELECTRICALLY TESTED PER: MPG 10592

The 10592 contains four line drivers with complementary outputs. Each driver has a Data (D) input and shares an Enable (E) input with another driver. The two driver outputs are the uncommitted collectors of a pair of NPN transistors operating as a current switch. Each driver accepts 10K MECL input signals and provides a nominal signal swing of 800 mV across a 50 Ω load at each output collector.

Outputs can drive higher values of load resistance, provided that the combination of IR drop and load return voltage V_{LR} does not cause an output collector to go more negative than -2.4 V with respect to V_{CC} . To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5 V with respect to V_{CC} .

When the \overline{E} input is high, both output transistors of a driver are nonconducting. When not used, the \overline{E} inputs, as well as the D inputs, may be left open.

- Open Collector Outputs Drive Terminated Lines or Transformers
- 50 kΩ Input Pull-down Resistors on All Inputs (Unused Inputs May be left Open)
- 805 mW typ/pkg (No Load)
- Propagation Delay = 3.5 ns typ (E-Output)
 = 3.0 ns typ (D-Output)

PIN ASSIGNMENTS **FUNCTION** DIL **FLATS** LCC **BURN-IN** (CONDITION C) Z₂ 1 5 2 GND Zο 2 3 GND 6 z_1 3 7 GND <u>Z</u>1 **GND** 8 5 D_1 9 7 **OPEN** D_2 10 8 **OPEN** E₁ 7 9 OPEN 11 VEE 8 12 10 VEE E₂ 13 12 **OPEN** D_3 10 13 **OPEN** 14 DA OPEN 11 15 14 $\overline{Z_A}$ 12 GND 16 15 **Z**4 13 1 17 GND $\overline{Z_3}$ 2 GND 14 18 Z₃ 15 3 19 GND Vcc 16 20 GND

BURN - IN CONDITIONS:

 $V_{TT} = -2.0 \text{ V MAX} - 2.2 \text{ V MIN}$

VEE = - 5.7 V MAX/ - 5.2 V MIN

Military 10592



AVAILABLE AS

1) JAN: N/A 2) SMD: N/A

3) 883: 10592/BXAJC

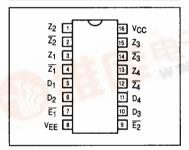
X = CASE OUTLINE AS FOLLOWS:

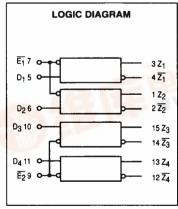
PACKAGE: CERDIP: E CERFLAT: F

LCC: 2

The letter "M" appears before

the slash on LCC.





MOTOROLA MILITARY MECL DATA 3-244

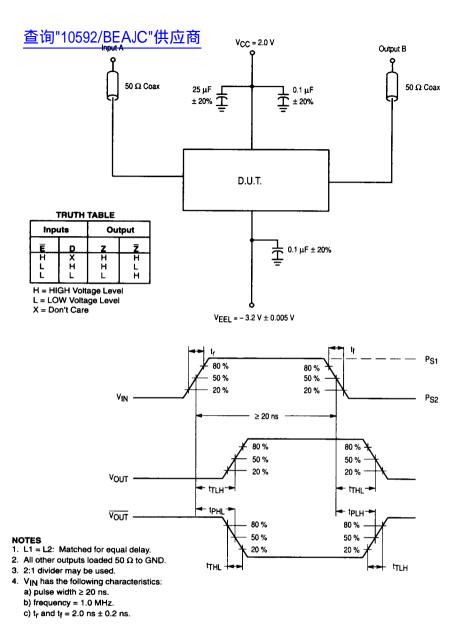


Figure 1. Switching Test Circuit and Waveforms

10592 QUIESCENT LIMIT TABLE *

Test						Test Vo	Test Voltage Values (Volts)	Volts)				
Temperature	ΑIΛ	۸۱۲	VIL VIH1	VIL1 P	SI	PS2	VEE (MIN)	VEE (MAX)	PS2 VEE (MIN) VEE (MAX) VEE (Nom)	Bvo	VLK	VOLS
TA = 25 °C - 0.780	- 0.780	- 1.85	- 1.85 - 1.105	- 1.475 - 0.89 - 1.69	- 0.89	- 1.69	- 5.72	- 4.68	- 5.2	+ 5.095 - 1.850	- 1.850	-2.4
T_A = 125 °C -0.630 -1.82 -1.000 -1.400 -0.78 -1.655	- 0.630	- 1.82	-1.000	- 1.400	- 0.78	- 1.655	- 5.72	- 4.68	-5.2	+ 4.960	+ 4.960 - 1.825	-2.4
TA = - 55 °C - 0.880	- 0.880	- 1.92	- 1.92 - 1.255	-1.510 -0.97 -1.715	- 0.97	-1.715	- 5.72	- 4.68	-5.2	+ 4.960 - 1.89	- 1.89	- 2.4

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V _{CC} = GND, Output Load = 50 Ω to GND, V _{LR} = 270 Ω to + 5.5 V V _{IL} V _{IH1} V _{IL1} V _{LR} V _{OLS} V _{EE} V _{CC} P. U. T.
VIL1 VLR VOLS
VIH1 VIL1
5,6,
+0.05
110
+ 0.10
-0.10
- 0.10
- 0.70
+ 0.10

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to Gnd.

10592 QUIESCENT LIMIT TABLE *

Test						Test Vol	Test Voltage Values (Volts)	(Volts)					
Temperature	ΗΛ	VIL.	VIH1	VIL1	Ps1	PS2	VEE (MIN)	VEE (MAX)	VIL VIH1 VIL1 PS1 PS2 VEE (MIN) VEE (MAX) VEE (Nom)	BVO	VLK VOLS	VOLS	
TA = 25 °C - 0.780	- 0.780	- 1.85	- 1.105	-1.105 -1.475 -0.89 -1.69	- 0.89	- 1.69	- 5.72	- 4.68	-5.2	+ 5.095	- 1.850	- 2.4	
TA = 125 °C - 0.630	- 0.630	- 1.82	- 1.82 - 1.000 - 1.400 - 0.78 - 1.655	- 1.400	- 0.78	- 1.655	- 5.72	- 4.68	-5.2	+ 4.960	- 1.825	- 2.4	
T_A = -55 °C · 0.880 · 1.92 · 1.255 · 1.510 · 0.97 · 1.715 · 5.72	- 0.880	- 1.92	- 1.255	- 1.510	- 0.97	- 1.715	- 5.72	- 4.68	- 5.2	+ 4.960	- 1.89	- 2.4	
Symbol	Parameter	er			Limits			Units	-	FEST VOLT	AGE APPI	TEST VOLTAGE APPLIED TO PINS BELOW	IS BELOW
			+ 25 °C		+ 125 °C		ე _° 55 -		Pinouts ref	erenced ar	re for DIL p	ackage, ch	Pinouts referenced are for DIL package, check Pin Assig

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Symbol	Parameter			Limits	ts			Units		TEST VO	LTAGE AP	PLIED TO	TEST VOLTAGE APPLIED TO PINS BELOW	<u>7</u> [₹
	i.	+ 25 °C	ပ္	+ 125 °C	ပွ	ე _。 99 -	၁့		Pinouts	referenced	are for Di	L package	, check Pin	Pinouts referenced are for DIL package, check Pin Assignmen
	Functional Parameters:	Subgro	Subgroup 9 ·	Subgroup 10	up 10	Subgroup 11	up 11			Acc =	GND, Outp	ut Load =	V _{CC} = GND, Output Load = 50 Ω to GND	٥
	•	Min	Max	Min Max	Мах	Min	Мах		NIA	Vou	VOUT VCC VEEL	VEEL	PS1	P. U. T.
Ħ_LH	Rise Time	0.5	3.3	0.5	4.7	0.5	3.8	SU	ns 6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 -
五五	Fall Time	0.5	3.3	0.5	4.7	0.5	3.8	SU	ns 6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1-4, 12-
퍞	Propagation Delay Data	1.5	4.5	1.5	5.6	1.5	5.3	SU	ns 6, 9, 10, 11 1-4, 12-15	1 - 4, 12 - 15	16	80	10, 11	1 - 4, 12 -
护	Propagation Delay Enable	2.0	6.0	1.0	9.0	1.0	6.0	ns	ns 6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1-4, 12-

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* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to Gnd.