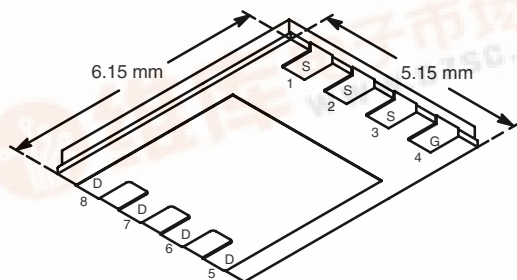


N-Channel 30-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
30	0.0048 at V _{GS} = 10 V	50	27.8 nC
	0.0066 at V _{GS} = 4.5 V	50	

PowerPAK[®] SO-8

Bottom View

Ordering Information: Si7748DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

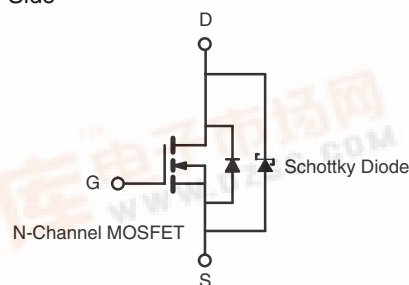
FEATURES

- Halogen-free
- SkyFET™ Monolithic TrenchFET[®] Power MOSFET and Schottky Diode
- 100 % R_g Tested
- 100 % UIS Tested

RoHS
COMPLIANT

APPLICATIONS

- Notebook
- Vcore Low-Side

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	50 ^a
		T _C = 70 °C	50 ^a
		T _A = 25 °C	23.5 ^{b, c}
		T _A = 70 °C	18.6 ^{b, c}
Pulsed Drain Current	I _{DM}	80	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	4.3 ^{b, c}
Single Pulse Avalanche Current	I _{AS}	30	mJ
Single Pulse Avalanche Energy	E _{AS}	45	
Maximum Power Dissipation	P _D	T _C = 25 °C	56
		T _C = 70 °C	31
		T _A = 25 °C	4.8 ^{b, c}
		T _A = 70 °C	3 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	21	26	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.7	2.2	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 68 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	30			V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$	1.3		2.7	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$		0.075	0.30	mA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 100\text{ }^\circ\text{C}$		6.7	65	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	40			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		0.0039	0.0048	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		0.0053	0.0066	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		80		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		3770		pF
Output Capacitance	C_{oss}			575		
Reverse Transfer Capacitance	C_{rss}			215		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		61	92	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		27.8	42	
Gate-Source Charge	Q_{gs}			10.2		
Gate-Drain Charge	Q_{gd}			7.3		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.2	1.0	2.0	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		15	30	ns
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(off)}$			35	70	
Fall Time	t_f			8	16	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		36	75	
Rise Time	t_r			16	30	
Turn-Off Delay Time	$t_{d(off)}$			44	85	
Fall Time	t_f			16	30	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			50	A
Pulse Diode Forward Current ^a	I_{SM}				80	
Body Diode Voltage	V_{SD}	$I_S = 2\text{ A}$		0.42	0.55	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		25	50	ns
Body Diode Reverse Recovery Charge	Q_{rr}			13	26	nC
Reverse Recovery Fall Time	t_a			12		ns
Reverse Recovery Rise Time	t_b			13		

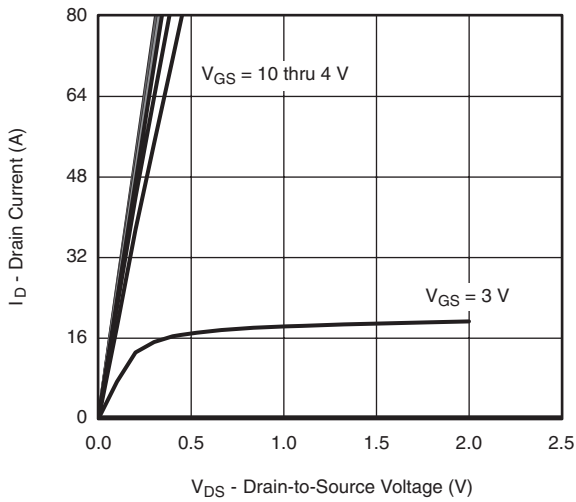
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

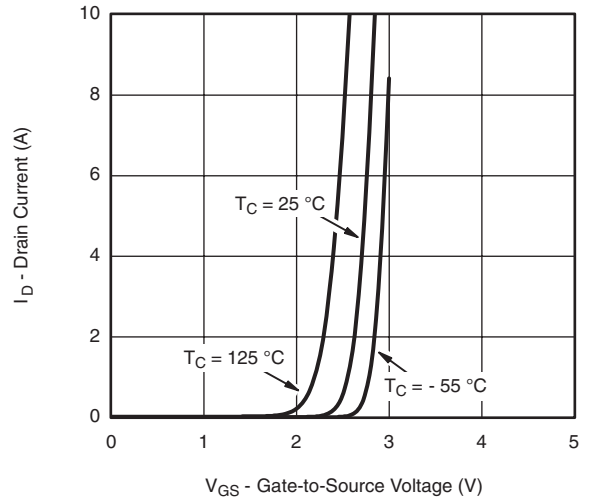
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



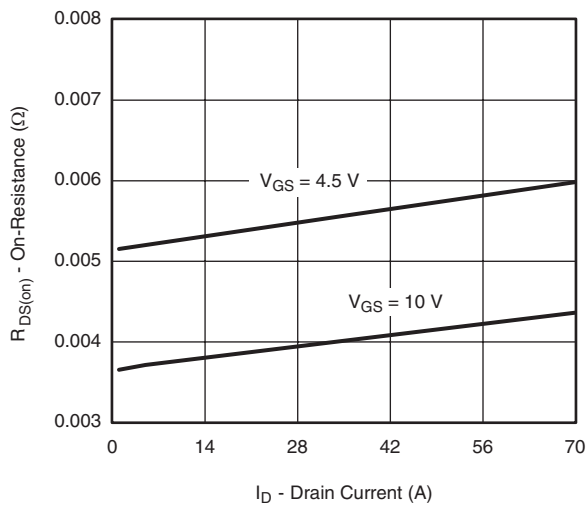
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



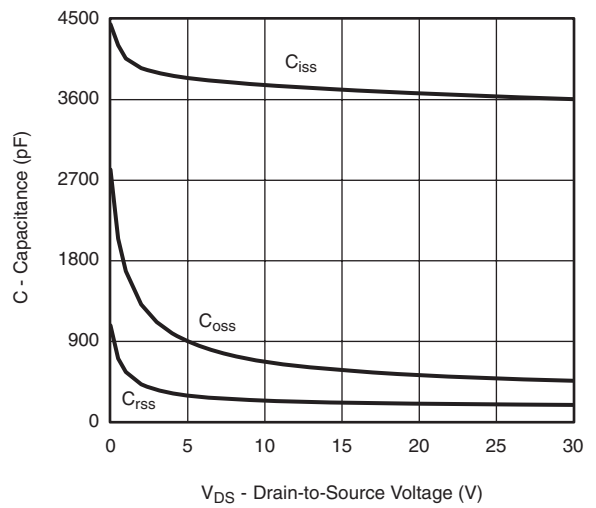
Output Characteristics



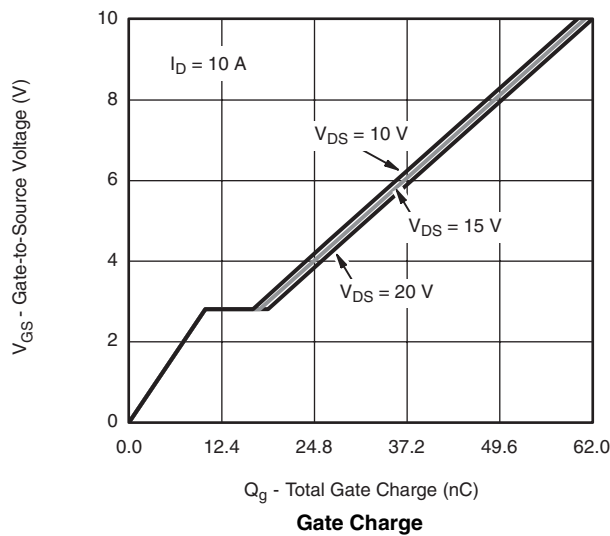
Transfer Characteristics



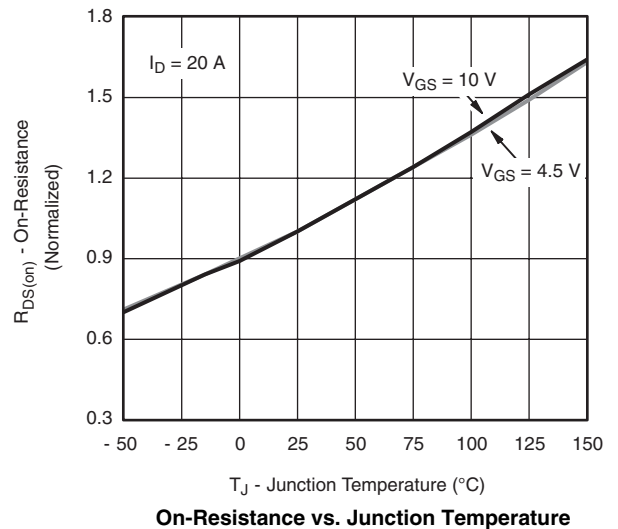
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



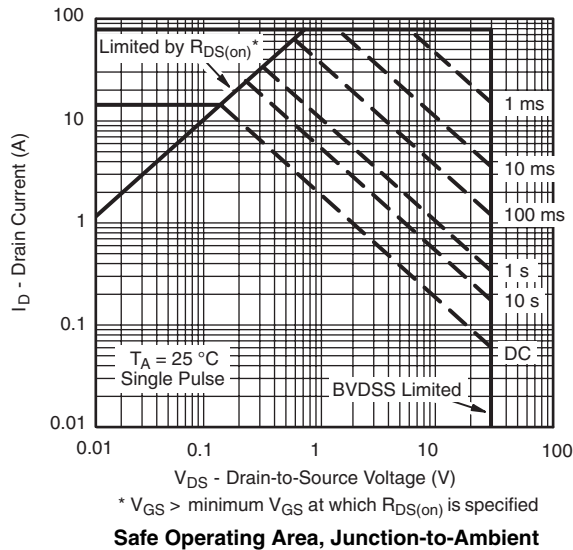
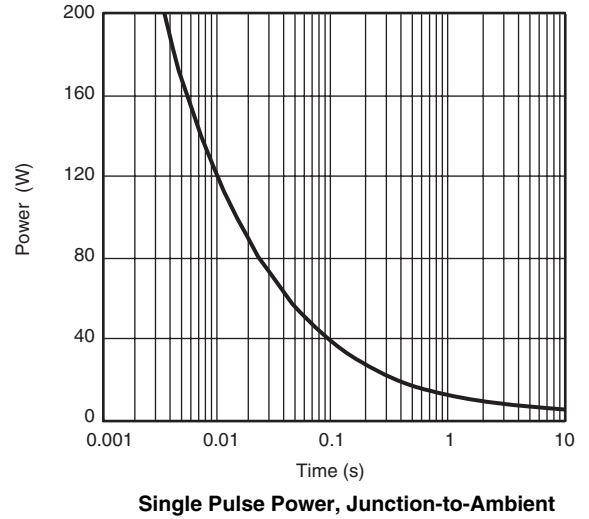
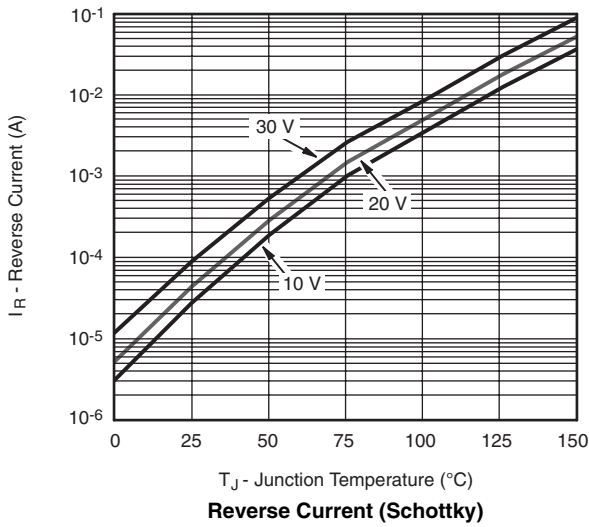
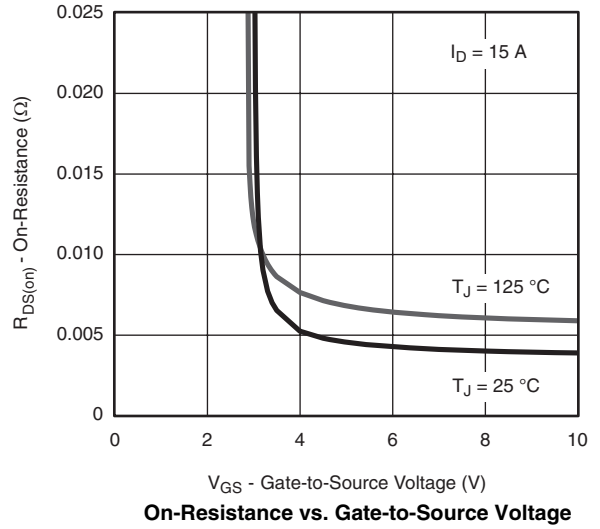
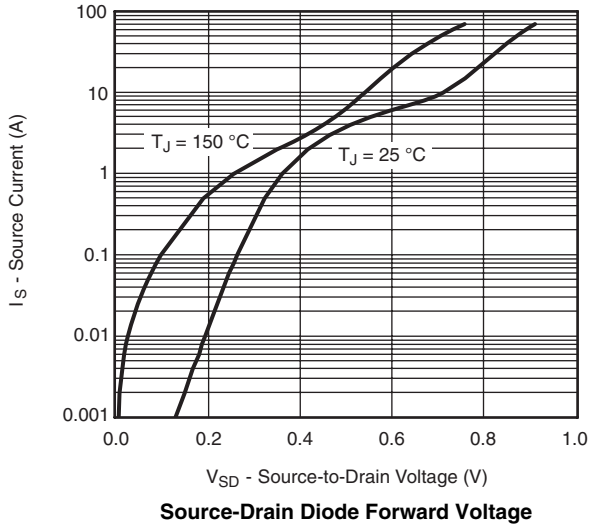
On-Resistance vs. Junction Temperature

Si7748DP



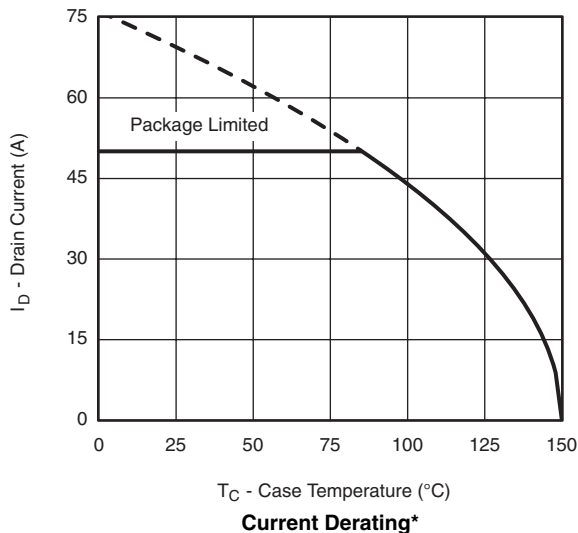
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

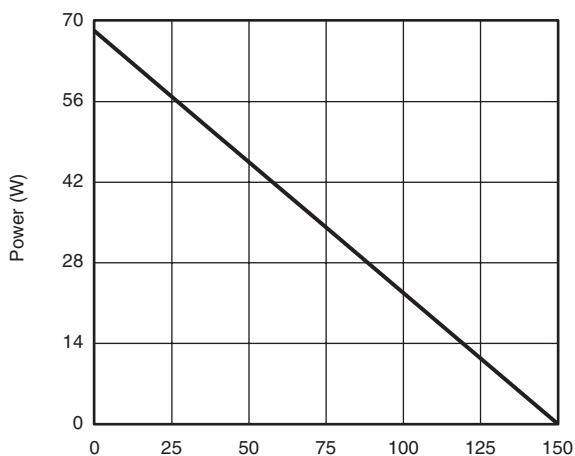




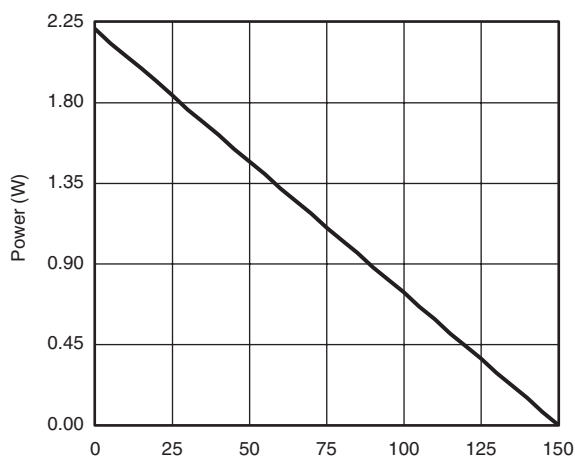
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



Power, Junction-to-Case



Power, Junction-to-Ambient

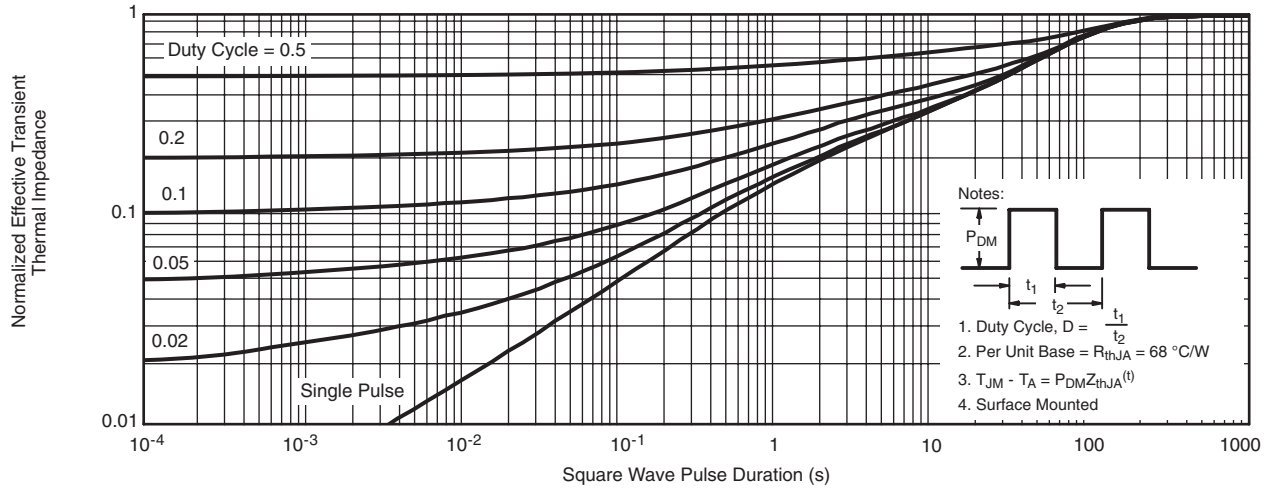
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si7748DP

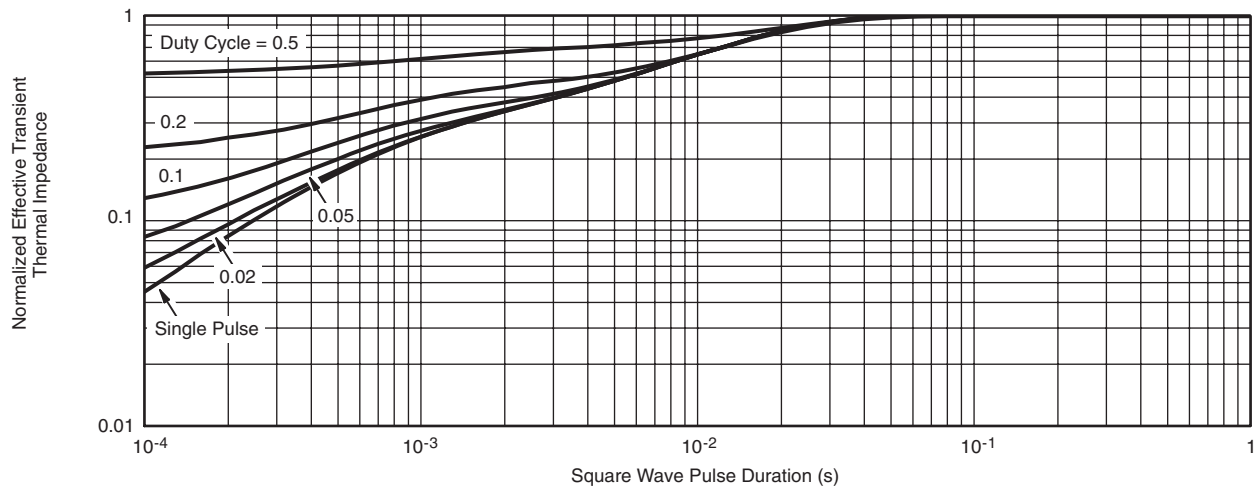


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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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