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Features

- 35% power reduction of the 100164
- 2000V ESD protection
- Pin/function compatible with 100164
- Voltage compensated operating range= -4.2V to -5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

(Absolute Maximum Ratings) (Note 1)

Storage Temperature (Istg)	-65C to +150C
Maximum Junction Temperature (Tj) Ceramic Plastic	+175C +150C
Vee Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	Vee to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	<u>></u> 2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: $\dot{\text{ESD}}$ testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (Tc)	
Commercial	0 C to +85 C
Industrial	-40 C to +85C
Military	-55C to +125C
Supply Voltage (Vee)	
	-5.7V to -4.2V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.) DC: Vee Range: -4.2V to -5.7V, Tc=-55C to +125C, VCC=VCCA=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN- NAME	MIN	MAX	UNIT	SUB- GROUPS
IIH	Input HIGH Current	VEE=-5.7V, VM=-0.87V	1, 3	INPUTS		300	uA	1, 2
			1, 3	INPUTS		450	uA	3
IIL	Input Low Current	VEE=-4.2V, VM=-1.83V	1, 3	INPUTS	0.5		uA	$\frac{1}{3}$, 2,
VOH	Output HIGH Voltage	VEE=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1025	-870	mV	1, 2
	Vortage		1, 3	OUTPUTS	-1085	-870	mV	3
VOL		Vee=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1830	-1620	mV	1, 2
Vortage		1, 3	OUTPUTS	-1830	-1555	mV	3	
VOHC	VOHC Output HIGH Voltage Corner	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, Loading: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1035		mV	1, 2
Point High	The first, boaring. to this to first	1, 3	OUTPUTS	-1085		mV	3	
VOLC	OLC Output LOW Vee=-4.2V/-5.7V, VIH=-1.165V, Voltage Corner VIL=-1.475V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS		-1610	mV	1, 2	
Point High		1, 3	OUTPUTS		-1555	mV	3	
VIH	Input HIGH Voltage		1, 3, 7	INPUTS	-1165	-870	mV	1, 2, 3
VIL	Input LOW Voltage		1, 3, 7	INPUTS	-1830	-1475	mV	$\frac{1}{3}$, 2,
IEE	Input LOW Voltage	VEE=-4.2/-5.7V	1, 3	INPUTS	-95	-35	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.) AC: VEE Range: -4.2V to -5.7V, LOADING: 50 Ohms to -2.0V, VCC=VCCA=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN- NAME	MIN	мах	UNIT	SUB- GROUPS
tpLH/tpHL(1)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	In to Zn	0.6	2.4	ns	9
			2, 4	In to Zn	0.6	2.8	ns	10
			2, 4	In to Zn	0.5	2.6	ns	11
tpLH/tpHL(2)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	SO, S1 to Zn	0.9	3.1	ns	9
			2, 4	SO, S1 to Zn	1.0	3.5	ns	10
			2, 4	SO, S1 to Zn	0.7	3.3	ns	11
tpLH/tpHL(3)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	S2, S3 to Zn	0.7	2.6	ns	9
			2, 4	S2, S3 to Zn	0.6	3.0	ns	10
			2, 4	S2, S3 to Zn	0.5	2.9	ns	11
tTLH/tTHL	Transistion Time	VEE=-4.2/-5.7V	6	Zn	0.2	1.2	ns	9, 10, 11
Note 1: Screen tested 100% on each device at -55 C, +25 C and +125 C temp., subgroups 1, 2,								

np., νg. up 3, 7 & 8.

5, / & 8. For QB devices, screen tested 100% on each device at +25C temperature only, subgroup A9. For QMLV devices, screen tested 100% on each device at +25C, +125C & -55C temperature, subgroups A9, 10 & 11. Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, +125 C & -55 C temp., subgroups A1, 2, 3, 7 & 8. Generating (Method 5005, Table 1) on each MFG. lot at +25 C, enderson 10, and etc. Note 2:

Note 3:

Note 4:

Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, subgroup A9, and at +125 C & -55 C temp., subgroups A10 & 11. Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C temp. only, subgroup Note 5: A9. A9. Not tested at +25 C, +125 C & -55 C temp. (DESIGN CHARACTERIZATION DATA). Guaranteed by applying specified input condition and testing VOH/VOL.

Note 6:

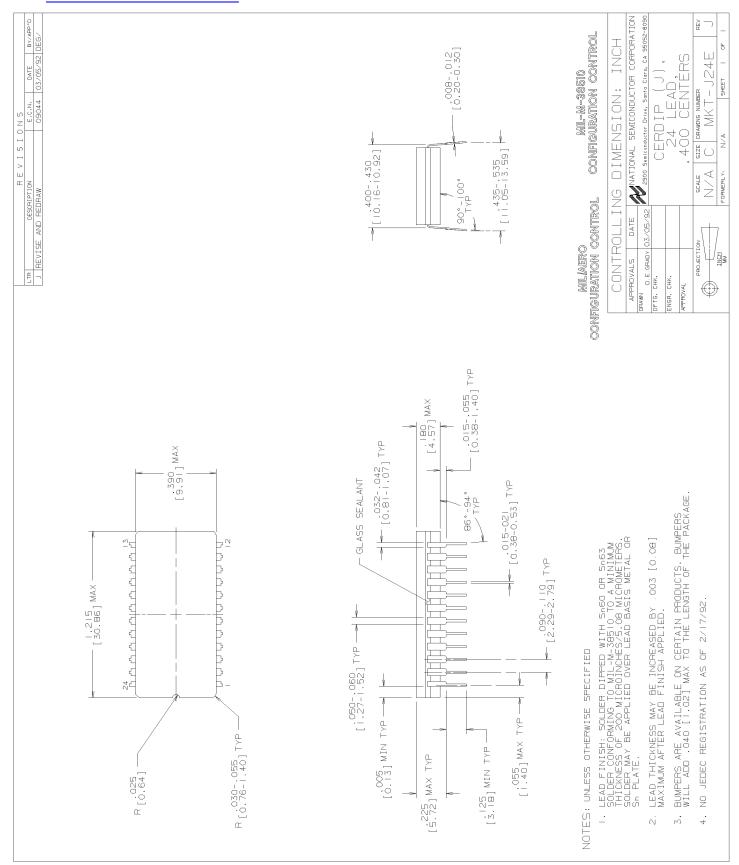
Note 7:

Graphics and Diagrams

GRAPHICS#	DESCRIPTION	
J24ERJ	CERDIP(J), 24LD .400 CENTERS (P/P DWG)	
P000088A	CERDIP (J), 24LD .400 CENTERS (PIN OUT)	
P000089 A	CERPAC, QUAD, 24 LEAD (PIN OUT)	
W24BRE	CERPAC, QUAD, 24 LEAD (P/P DWG)	

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See attached graphics following this page.



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