

## Four LVPECL Output, High-Performance Clock Buffer

Check for Samples: [CDCLVP2102](#)

### FEATURES

- Dual 1:2 Differential Buffer
- Two Clock Inputs
- Universal Inputs Can Accept LVPECL, LVDS, LVC MOS/LVTTL
- Four LVPECL Outputs
- Maximum Clock Frequency: 2 GHz
- Maximum Core Current Consumption: 48 mA
- Very Low Additive Jitter: <100 fs,rms in 10-kHz to 20-MHz Offset Range
- 2.375-V to 3.6-V Device Power Supply
- Maximum Propagation Delay: 450 ps
- Maximum Within Bank Output Skew: 10 ps
- LVPECL Reference Voltage,  $V_{AC\_REF}$ , Available for Capacitive-Coupled Inputs
- Industrial Temperature Range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Available in 3-mm  $\times$  3-mm QFN-16 (RGT) Package
- ESD Protection Exceeds 2 kV (HBM)

### APPLICATIONS

- Wireless Communications
- Telecommunications/Networking
- Medical Imaging
- Test and Measurement Equipment

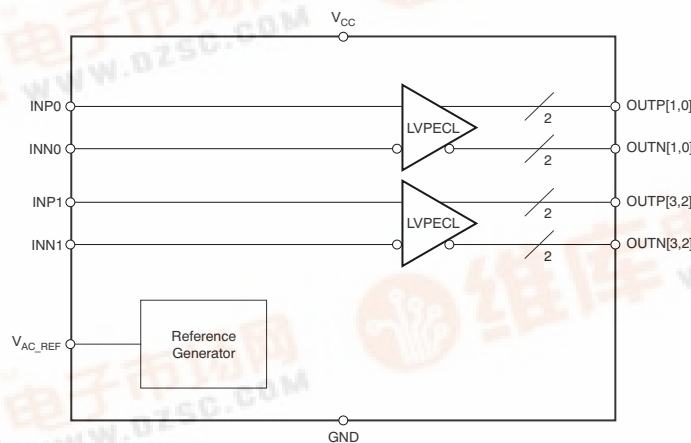
### DESCRIPTION

The CDCLVP2102 is a highly versatile, low additive jitter buffer that can generate four copies of LVPECL clock outputs from two LVPECL, LVDS, or LVC MOS inputs for a variety of communication applications. It has a maximum clock frequency up to 2 GHz. Each buffer block consists of one input that feeds two LVPECL outputs. The overall additive jitter performance is less than 0.1 ps, RMS from 10 kHz to 20 MHz, and overall output skew is as low as 10 ps, making the device a perfect choice for use in demanding applications.

The CDCLVP2102 clock buffer distributes two clock inputs (IN0, IN1) to four pairs of differential LVPECL clock outputs (OUT0, OUT3) with minimum skew for clock distribution. Each buffer block consists of one input that feeds two LVPECL clock outputs. The inputs can be LVPECL, LVDS, or LVC MOS/LVTTL.

The CDCLVP2102 is specifically designed for driving 50- $\Omega$  transmission lines. When driving the inputs in single-ended mode, the LVPECL bias voltage ( $V_{AC\_REF}$ ) should be applied to the unused negative input pin. However, for high-speed performance up to 2 GHz, differential mode is strongly recommended.

The CDCLVP2102 is characterized for operation from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and is available in a QFN-16, 3-mm  $\times$  3-mm package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2009, Texas Instruments Incorporated



## CDCLVP2102 电压转换器



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### AVAILABLE OPTIONS<sup>(1)</sup>

T <sub>A</sub>	PACKAGED DEVICES	FEATURES
–40°C to +85°C	CDCLVP2102RGTT	16-pin QFN (RGT) package, small tape and reel
	CDCLVP2102RGTR	16-pin QFN (RGT) package, tape and reel

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this data sheet or refer to our web site at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted).<sup>(1)</sup>

		CDCLVP2102	UNIT
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	–0.5 to 4.6	V
V <sub>IN</sub>	Input voltage range <sup>(3)</sup>	–0.5 to V <sub>CC</sub> + 0.5	V
V <sub>OUT</sub>	Output voltage range <sup>(3)</sup>	–0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IN</sub>	Input current	20	mA
I <sub>OUT</sub>	Output current	50	mA
T <sub>A</sub>	Specified free-air temperature range (no airflow)	–40 to +85	°C
T <sub>STG</sub>	Storage temperature range	–65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+125	°C
ESD	Electrostatic discharge (HBM)	2	kV

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All supply voltages must be supplied simultaneously.

(3) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		CDCLVP2102			UNIT
		MIN	TYP	MAX	
V <sub>CC</sub>	Supply voltage	2.375	2.50/3.30	3.60	V
T <sub>A</sub>	Ambient temperature	−40		+85	°C

### PACKAGE DISSIPATION RATINGS<sup>(1) (2)</sup>

PARAMETER	TEST CONDITIONS	VALUE	UNIT
		2 × 2 VIAS ON PAD	
θ <sub>JA</sub>	0 LFM	51.8	°C/W
	150 LFM	45	°C/W
	400 LFM	48.0	°C/W
θ <sub>JP</sub> <sup>(3)</sup>	Thermal resistance, junction-to-pad	6.12	°C/W

(1) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC 2S2P (high-K board).

(2) Connected to GND with four thermal vias (0.3-mm diameter).

(3) θ<sub>JP</sub> (junction-to-pad) is used for the QFN package, because the primary heat flow is from the junction to the GND pad of the QFN package.

**ELECTRICAL CHARACTERISTICS: LVCMOS Input<sup>(1)</sup>**

At  $V_{CC} = 2.375\text{ V}$  to  $3.6\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	CDCLVP2102			UNIT
		MIN	TYP	MAX	
$f_{IN}$ Input frequency				200	MHz
$V_{th}$ Input threshold voltage	External threshold voltage applied to complementary input	1.1		1.8	V
$V_{IH}$ Input high voltage		$V_{th} + 0.1$		$V_{CC}$	V
$V_{IL}$ Input low voltage		0		$V_{th} - 0.1$	V
$I_{IH}$ Input high current	$V_{CC} = 3.6\text{ V}$ , $V_{IH} = 3.6\text{ V}$			40	$\mu\text{A}$
$I_{IL}$ Input low current	$V_{CC} = 3.6\text{ V}$ , $V_{IL} = 0\text{ V}$			-40	$\mu\text{A}$
$\Delta V/\Delta T$ Input edge rate	20% to 80%	1.5			V/ns
$I_{CAP}$ Input capacitance			5		pF

(1) [Figure 3](#) and [Figure 4](#) show dc test setup.

**ELECTRICAL CHARACTERISTICS: Differential Input<sup>(1)</sup>**

At  $V_{CC} = 2.375\text{ V}$  to  $3.6\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	CDCLVP2102			UNIT
		MIN	TYP	MAX	
$f_{IN}$ Input frequency	Clock input			2000	MHz
$V_{IN, \text{DIFF, PP}}$ Differential input peak-peak voltage	$f_{IN} \leq 1.5\text{ GHz}$	0.1		1.5	V
	$1.5\text{ GHz} \leq f_{IN} \leq 2\text{ GHz}$	0.2		1.5	V
$V_{ICM}$ Input common-mode level		1.0		$V_{CC} - 0.3$	V
$I_{IH}$ Input high current	$V_{CC} = 3.6\text{ V}$ , $V_{IH} = 3.6\text{ V}$			40	$\mu\text{A}$
$I_{IL}$ Input low current	$V_{CC} = 3.6\text{ V}$ , $V_{IL} = 0\text{ V}$			-40	$\mu\text{A}$
$\Delta V/\Delta T$ Input edge rate	20% to 80%	1.5			V/ns
$I_{CAP}$ Input capacitance			5		pF

(1) [Figure 5](#) and [Figure 6](#) show dc test setup. [Figure 7](#) shows ac test setup.

**ELECTRICAL CHARACTERISTICS: LVPECL Output<sup>(1)</sup>**At  $V_{CC} = 2.375\text{ V}$  to  $2.625\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	CDCLVP2102			UNIT
		MIN	TYP	MAX	
$V_{OH}$	Output high voltage	$V_{CC} - 1.26$		$V_{CC} - 0.9$	V
$V_{OL}$	Output low voltage	$V_{CC} - 1.7$		$V_{CC} - 1.3$	V
$V_{OUT, \text{DIFF}, PP}$	Differential output peak-peak voltage	$f_{IN} \leq 2\text{ GHz}$	0.5	1.35	V
$V_{AC\_REF}$	Input bias voltage	$I_{AC\_REF} = 2\text{ mA}$	$V_{CC} - 1.6$	$V_{CC} - 1.1$	V
$t_{PD}$	Propagation delay	$V_{IN, \text{DIFF}, PP} = 0.1\text{ V}$		450	ps
		$V_{IN, \text{DIFF}, PP} = 0.3\text{ V}$		450	ps
$t_{SK, PP}$	Part-to-part skew			100	ps
$t_{SK, O\_WB}$	Within bank output skew			10	
$t_{SK, O\_BB}$	Bank-to-bank output skew	Both inputs have equal skew		15	ps
$t_{SK, P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, $f_{OUT} = 100\text{ MHz}$	-50	50	ps
$t_{RJIT}$	Random additive jitter (with 50% duty cycle input)	$f_{OUT} = 100\text{ MHz}$ , $V_{IN, SE} = V_{CC}$ , $V_{th} = 1.25\text{ V}$ , 10 kHz to 20 MHz	0.089		ps, RMS
		$f_{OUT} = 100\text{ MHz}$ , $V_{IN, SE} = 0.9\text{ V}$ , $V_{th} = 1.1\text{ V}$ , 10 kHz to 20 MHz	0.093		ps, RMS
		$f_{OUT} = 2\text{ GHz}$ , $V_{IN, \text{DIFF}, PP} = 0.2\text{ V}$ , $V_{ICM} = 1\text{ V}$ , 10 kHz to 20 MHz	0.037		ps, RMS
		$f_{OUT} = 100\text{ MHz}$ , $V_{IN, \text{DIFF}, PP} = 0.15\text{ V}$ , $V_{ICM} = 1\text{ V}$ , 10 kHz to 20 MHz	0.094		ps, RMS
		$f_{OUT} = 100\text{ MHz}$ , $V_{IN, \text{DIFF}, PP} = 1\text{ V}$ , $V_{ICM} = 1\text{ V}$ , 10 kHz to 20 MHz	0.091		ps, RMS
$P_{SPUR}$	Coupling on differential OUT8 from OUT7 in the frequency spectrum of $f_{OUT, 8} \pm (f_{OUT, 8}/2)$ with synchronous inputs	$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, \text{DIFF}, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 62.5\text{ MHz}$ , $V_{IN, SE, 1} = V_{CC}$ , $V_{th, 1} = V_{CC}/2$	-52.5		dBc
		$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, \text{DIFF}, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 62.5\text{ MHz}$ , $V_{IN, \text{DIFF}, PP, 1} = 1\text{ V}$ , $V_{ICM, 1} = 1\text{ V}$	-66.8		dBc
		$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, \text{DIFF}, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 15.625\text{ MHz}$ , $V_{IN, SE, 1} = V_{CC}$ , $V_{th, 1} = V_{CC}/2$	-52		dBc
		$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, \text{DIFF}, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 15.625\text{ MHz}$ , $V_{IN, \text{DIFF}, PP, 1} = 1\text{ V}$ , $V_{ICM, 1} = 1\text{ V}$	-66.4		dBc
$t_R/t_F$	Output rise/fall time	20% to 80%		200	ps
$I_{EE}$	Supply internal current	Outputs unterminated		48	mA
$I_{CC}$	Output and internal supply current	All outputs terminated, $50\ \Omega$ to $V_{CC} - 2$		173	mA

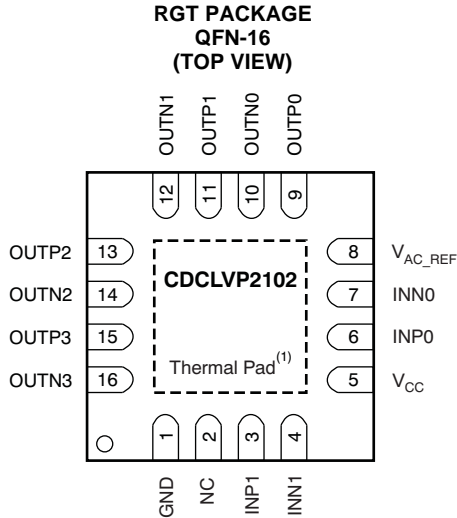
(1) Figure 8 and Figure 9 show dc and ac test setup.

**ELECTRICAL CHARACTERISTICS: LVPECL Output<sup>(1)</sup>**

At  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$  and  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	CDCLVP2102			UNIT
		MIN	TYP	MAX	
$V_{OH}$	Output high voltage	$V_{CC} - 1.26$		$V_{CC} - 0.9$	V
$V_{OL}$	Output low voltage	$V_{CC} - 1.7$		$V_{CC} - 1.3$	V
$V_{OUT, \text{DIFF, PP}}$	Differential output peak-peak voltage	$f_{IN} \leq 2\text{ GHz}$	0.65	1.35	V
$V_{AC\_REF}$	Input bias voltage	$I_{AC\_REF} = 2\text{ mA}$	$V_{CC} - 1.6$	$V_{CC} - 1.1$	V
$t_{PD}$	Propagation delay	$V_{IN, \text{DIFF, PP}} = 0.1\text{ V}$		450	ps
		$V_{IN, \text{DIFF, PP}} = 0.3\text{ V}$		450	ps
$t_{SK, PP}$	Part-to-part skew			100	ps
$t_{SK, O\_WB}$	Within bank output skew			10	ps
$t_{SK, O\_BB}$	Bank-to-bank output skew	Both inputs have equal skew		15	ps
$t_{SK, P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, $f_{OUT} = 100\text{ MHz}$	-50	50	ps
$t_{RJIT}$	Random additive jitter (with 50% duty cycle input)	$f_{OUT} = 100\text{ MHz}$ , $V_{IN, SE} = V_{CC}$ , $V_{th} = 1.65\text{ V}$ , 10 kHz to 20 MHz	0.081		ps, RMS
		$f_{OUT} = 100\text{ MHz}$ , $V_{IN, SE} = 0.9\text{ V}$ , $V_{th} = 1.1\text{ V}$ , 10 kHz to 20 MHz	0.097		ps, RMS
		$f_{OUT} = 2\text{ GHz}$ , $V_{IN, DIFF, PP} = 0.2\text{ V}$ , $V_{ICM} = 1\text{ V}$ , 10 kHz to 20 MHz	0.05		ps, RMS
		$f_{OUT} = 100\text{ MHz}$ , $V_{IN, DIFF, PP} = 0.15\text{ V}$ , $V_{ICM} = 1\text{ V}$ , 10 kHz to 20 MHz	0.098		ps, RMS
		$f_{OUT} = 100\text{ MHz}$ , $V_{IN, DIFF, PP} = 1\text{ V}$ , $V_{ICM} = 1\text{ V}$ , 10 kHz to 20 MHz	0.095		ps, RMS
$P_{SPUR}$	Coupling on differential OUT8 from OUT7 in the frequency spectrum of $f_{OUT, 8} \pm (f_{OUT, 8}/2)$ with synchronous inputs	$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, DIFF, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 62.5\text{ MHz}$ , $V_{IN, SE, 1} = V_{CC}$ , $V_{th, 1} = V_{CC}/2$	-55.3		dBc
		$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, DIFF, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 62.5\text{ MHz}$ , $V_{IN, SIFF, PP, 1} = 1\text{ V}$ , $V_{ICM, 1} = 1\text{ V}$	-65.1		dBc
		$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, DIFF, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 15.625\text{ MHz}$ , $V_{IN, SE, 1} = V_{CC}$ , $V_{th, 1} = V_{CC}/2$	-54.7		dBc
		$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, DIFF, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 15.625\text{ MHz}$ , $V_{IN, DIFF, PP, 1} = 1\text{ V}$ , $V_{ICM, 1} = 1\text{ V}$	-66.7		dBc
$t_R/t_F$	Output rise/fall time	20% to 80%		200	ps
$I_{EE}$	Supply internal current	Outputs unterminated		48	mA
$I_{CC}$	Output and internal supply current	All outputs terminated, $50\ \Omega$ to $V_{CC} - 2$		173	mA

(1) Figure 8 and Figure 9 show dc and ac test setup.



**PIN DESCRIPTIONS**

**CDCLVP2102 Pin Descriptions**

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
V <sub>CC</sub>	5	Power	2.5-/3.3-V supply for the device
GND	1	Ground	Device ground
INP0, INN0	6, 7	Input	Differential input pair or single-ended input no. 0
INP1, INN1	3, 4	Input	Differential input pair or single-ended input no. 1
OUTP3, OUTN3	15, 16	Output	Differential LVPECL output pair no. 3
OUTP2, OUTN2	13, 14	Output	Differential LVPECL output pair no. 2
OUTP1, OUTN1	11, 12	Output	Differential LVPECL output pair no. 1
OUTP0, OUTN0	9, 10	Output	Differential LVPECL output pair no. 0
V <sub>AC_REF</sub>	8	Output	Bias voltage output for capacitive-coupled input pair no. 0. If used, it is recommended to use a 0.1-μF capacitor to GND on this pin. The output current is limited to 2 mA.
NC	2	—	Do not connect

## TYPICAL CHARACTERISTICS

At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (unless otherwise noted).

### DIFFERENTIAL OUTPUT PEAK-TO-PEAK VOLTAGE vs FREQUENCY

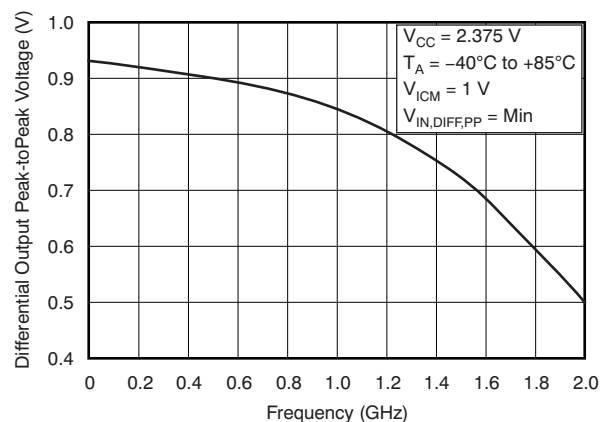


Figure 1.

### DIFFERENTIAL OUTPUT PEAK-TO-PEAK VOLTAGE vs FREQUENCY

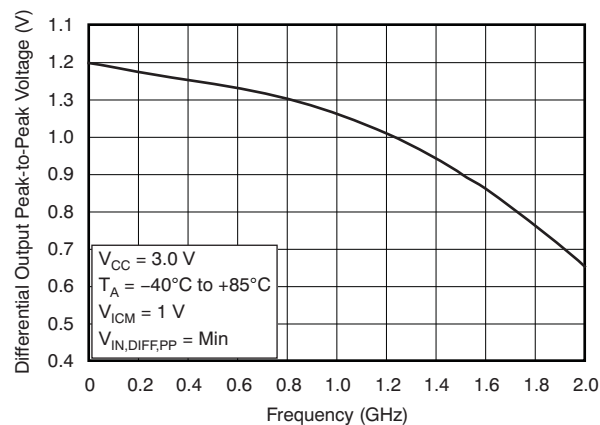
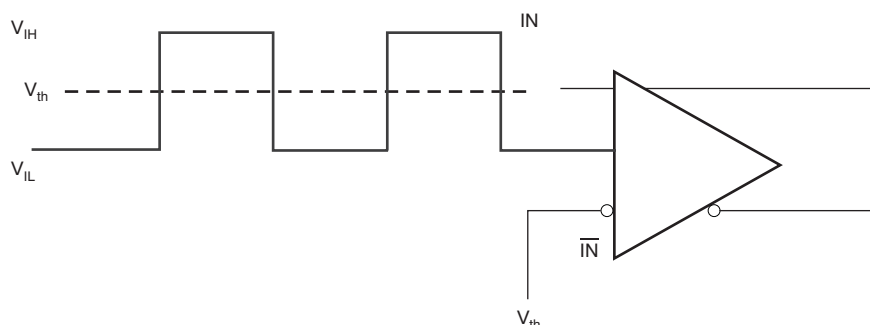


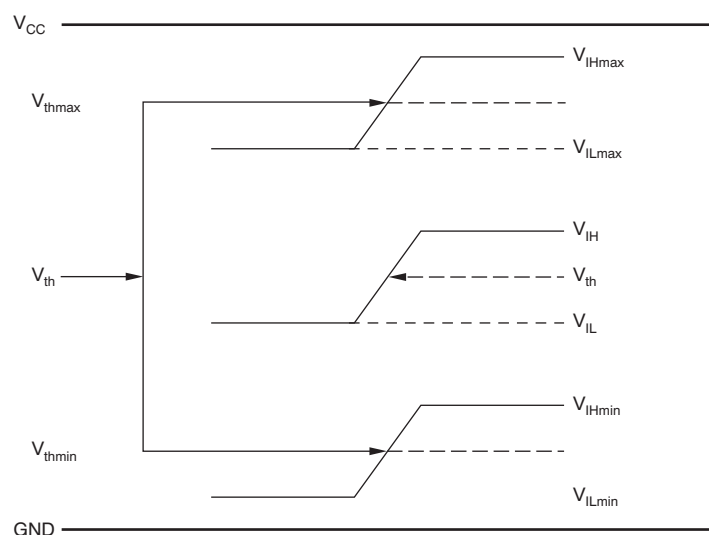
Figure 2.

## TEST CONFIGURATIONS

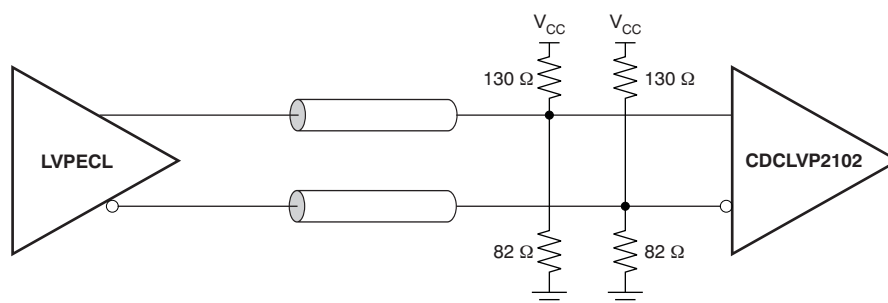
This section describes the function of each block for the CDCLVP2102. Figure 3 through Figure 9 illustrate how the device should be setup for a variety of test configurations.



**Figure 3. DC-Coupled LVCMOS Input During Device Test**



**Figure 4.  $V_{th}$  Variation over LVCMOS Levels**



**Figure 5. DC-Coupled LVPECL Input During Device Test**



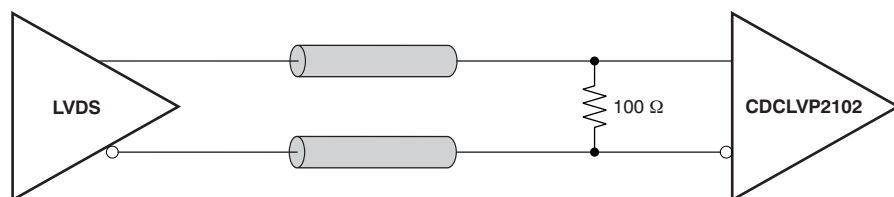


Figure 6. DC-Coupled LVDS Input During Device Test

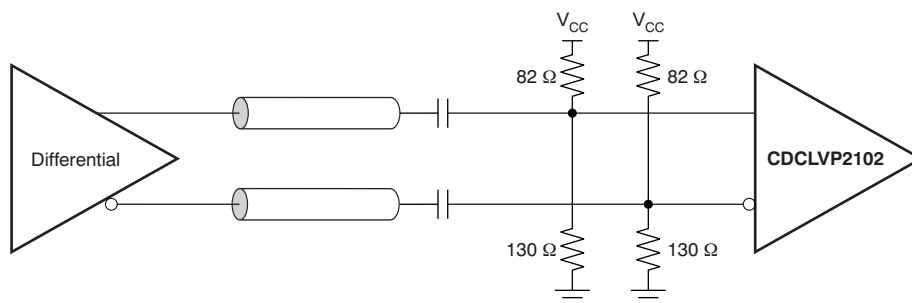


Figure 7. AC-Coupled Differential Input to Device

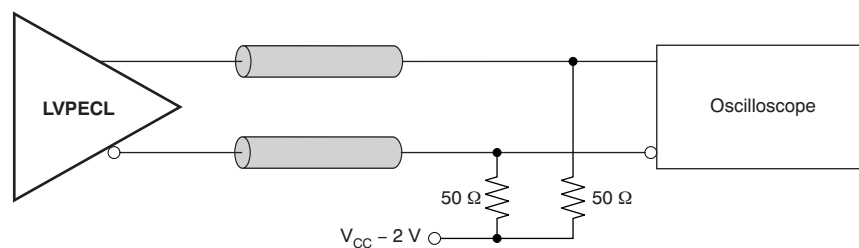


Figure 8. LVPECL Output DC Configuration During Device Test

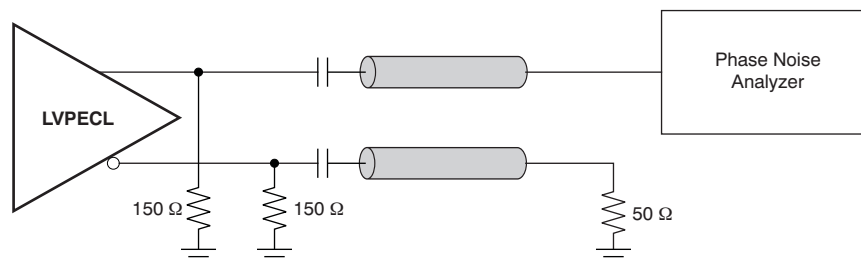
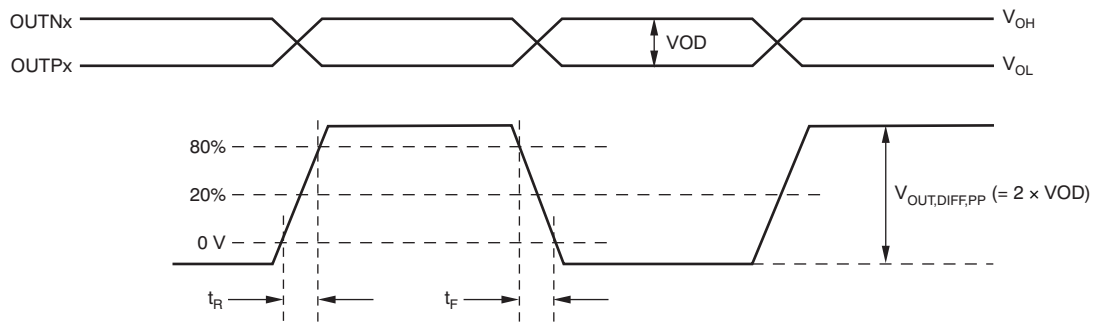
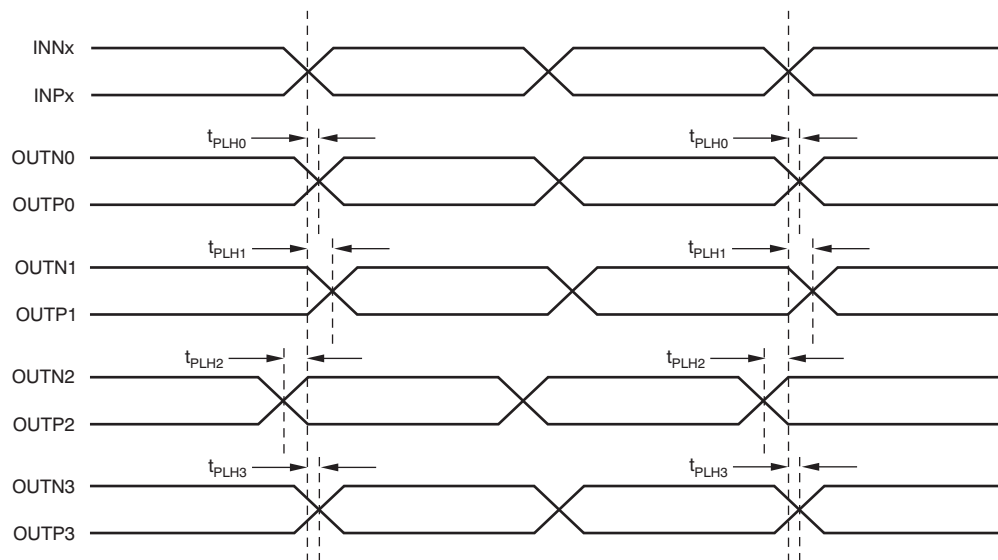


Figure 9. LVPECL Output AC Configuration During Device Test

Figure 10 shows the output voltage and rise/fall time. Output and part-to-part skew are shown in Figure 11.



**Figure 10. Output Voltage and Rise/Fall Time**



- (1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest  $t_{PLHn}$  ( $n = 0, 1, 2, 3$ ), or as the difference between the fastest and the slowest  $t_{PHLn}$  ( $n = 0, 1, 2, 3$ ).
- (2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest  $t_{PLHn}$  ( $n = 0, 1, 2, 3$ ) across multiple devices, or the difference between the fastest and the slowest  $t_{PHLn}$  ( $n = 0, 1, 2, 3$ ) across multiple devices.

**Figure 11. Output and Part-to-Part Skew**

## APPLICATION INFORMATION

### Thermal Management

Power consumption of the CDCLVP2102 can be high enough to require attention to thermal management. For reliability and performance reasons, the die temperature should be limited to a maximum of +125°C. That is, as an estimate, ambient temperature ( $T_A$ ) plus device power consumption times  $\theta_{JA}$  should not exceed +125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. Figure 12 shows a recommended land and via pattern.

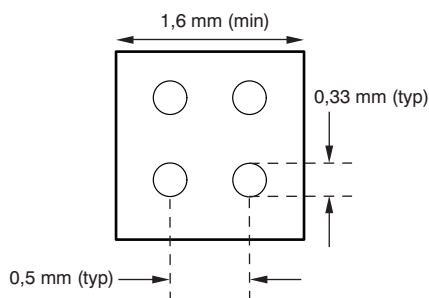


Figure 12. Recommended PCB Layout

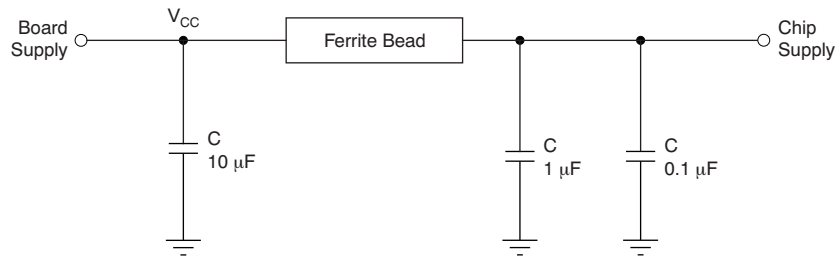
### Power-Supply Filtering

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1-μF) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with very low dc resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

## 德州仪器 CDCLVP2102 快速指南

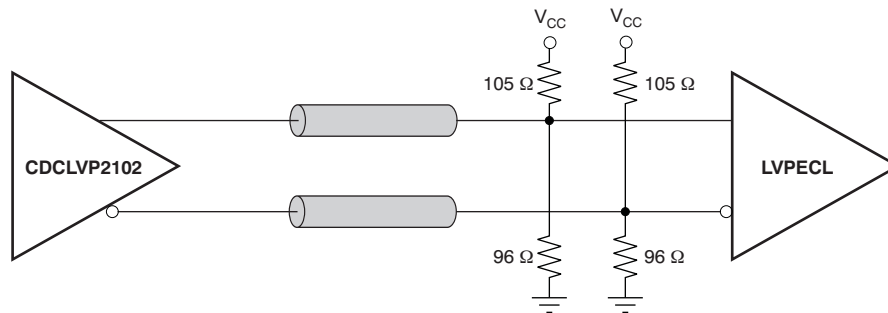
Figure 13 illustrates this recommended power-supply decoupling method.



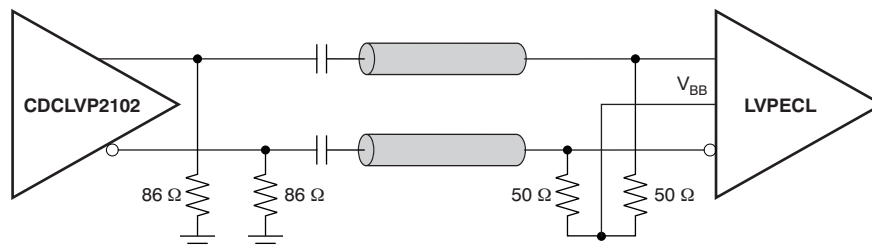
**Figure 13. Power-Supply Decoupling**

### LVPECL Output Termination

The CDCLVP2102 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination are required to ensure correct operation of the device and to minimize signal integrity. The proper termination for LVPECL outputs is a  $50\ \Omega$  to  $(V_{CC} - 2)\text{ V}$ , but this dc voltage is not readily available on PCB. Therefore, a Thevenin equivalent circuit is worked out for the LVPECL termination in both direct-coupled (dc) and ac-coupled configurations. These configurations are shown in Figure 14a and b for  $V_{CC} = 2.5\text{ V}$  and Figure 15a and b for  $V_{CC} = 3.3\text{ V}$ , respectively. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltage for the driver and receiver is different, ac coupling is required.

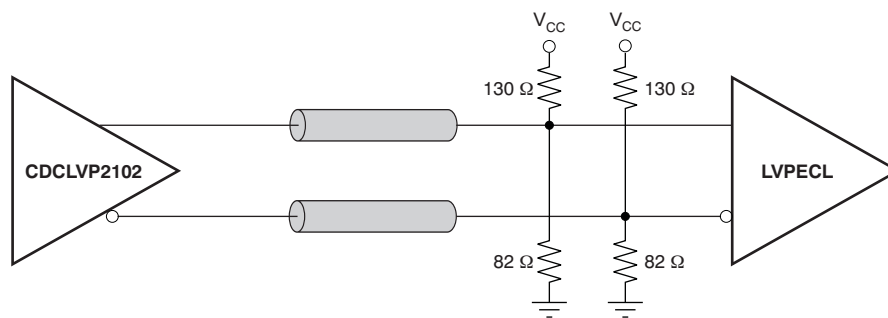


**(a) Output DC Termination**

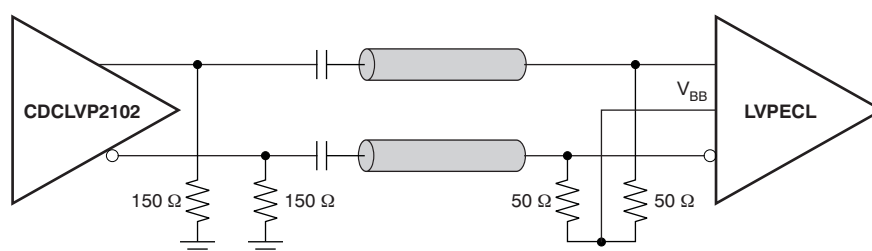


**(b) Output AC Termination**

**Figure 14. LVPECL Output DC and AC Termination for  $V_{CC} = 2.5\text{ V}$**



(a) Output DC Termination



(b) Output AC Termination

Figure 15. LVPECL Output DC and AC Termination for  $V_{CC} = 3.3\text{ V}$

## Input Termination

The CDCLVP2102 inputs can be interfaced with LVPECL, LVDS, or LVC MOS drivers. Figure 16 illustrates how to dc couple an LVC MOS input to the CDCLVP2102. The series resistance ( $R_S$ ) should be placed close to the LVC MOS driver; its value is calculated as the difference between the transmission line impedance and the driver output impedance.

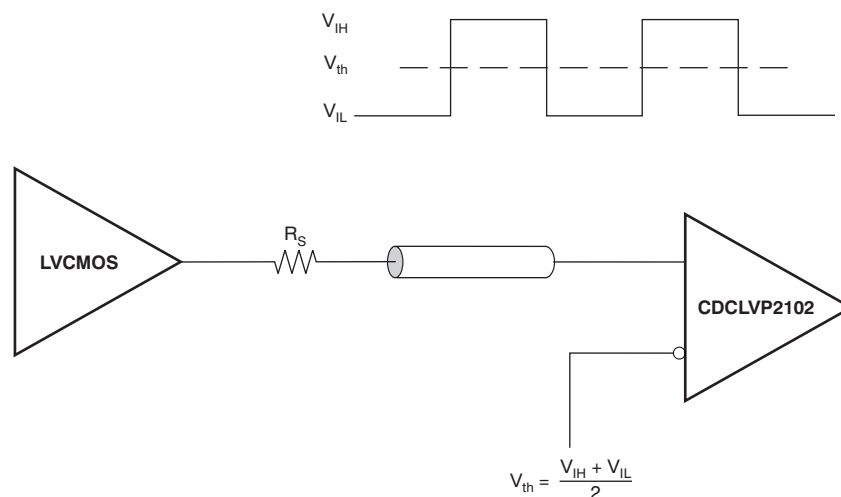
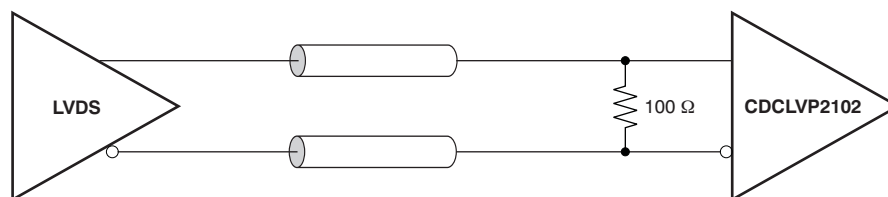


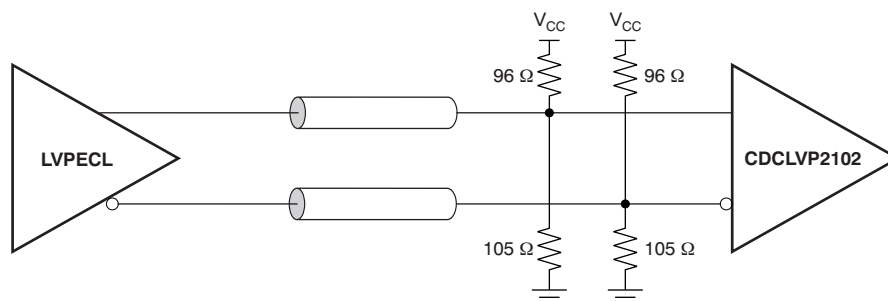
Figure 16. DC-Coupled LVC MOS Input to CDCLVP2102

[查看CDCLVP2102 快速指南](#)

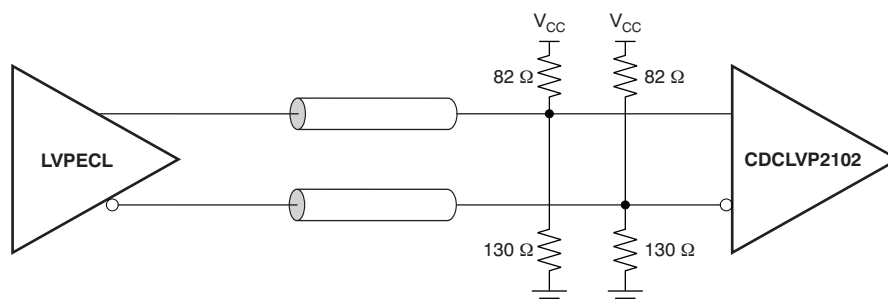
Figure 17 shows how to dc couple LVDS inputs to the CDCLVP2102. Figure 18 and Figure 19 describe the method of dc coupling LVPECL inputs to the CDCLVP2102 for  $V_{CC} = 2.5\text{ V}$  and  $V_{CC} = 3.3\text{ V}$ , respectively.



**Figure 17. DC-Coupled LVDS Inputs to CDCLVP2102**



**Figure 18. DC-Coupled LVPECL Inputs to CDCLVP2102 ( $V_{CC} = 2.5\text{ V}$ )**



**Figure 19. DC-Coupled LVPECL Inputs to CDCLVP2102 ( $V_{CC} = 3.3\text{ V}$ )**

Figure 20 and Figure 21 show the technique of ac coupling differential inputs to the CDCLVP2102 for  $V_{CC} = 2.5$  V and  $V_{CC} = 3.3$  V, respectively. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, ac coupling is required.

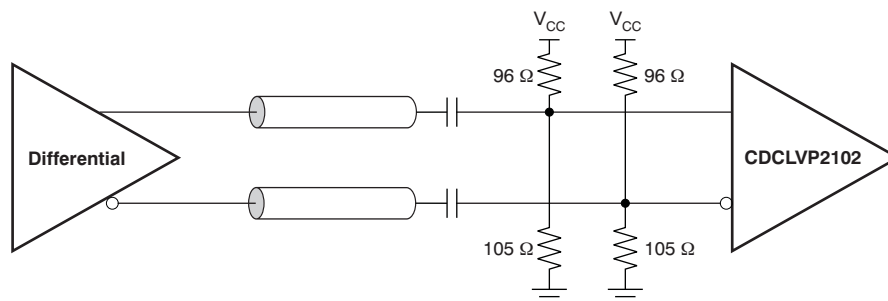


Figure 20. AC-Coupled LVPECL Inputs to CDCLVP2102 ( $V_{CC} = 2.5$  V)

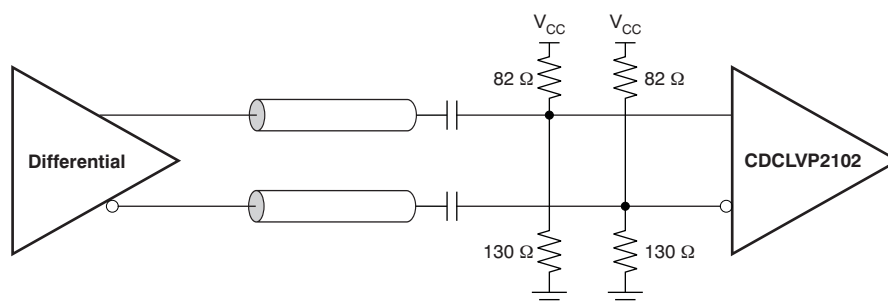


Figure 21. AC-Coupled LVPECL Inputs to CDCLVP2102 ( $V_{CC} = 3.3$  V)

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CDCLVP2102RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCLVP2102RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVP2102RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
CDCLVP2102RGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



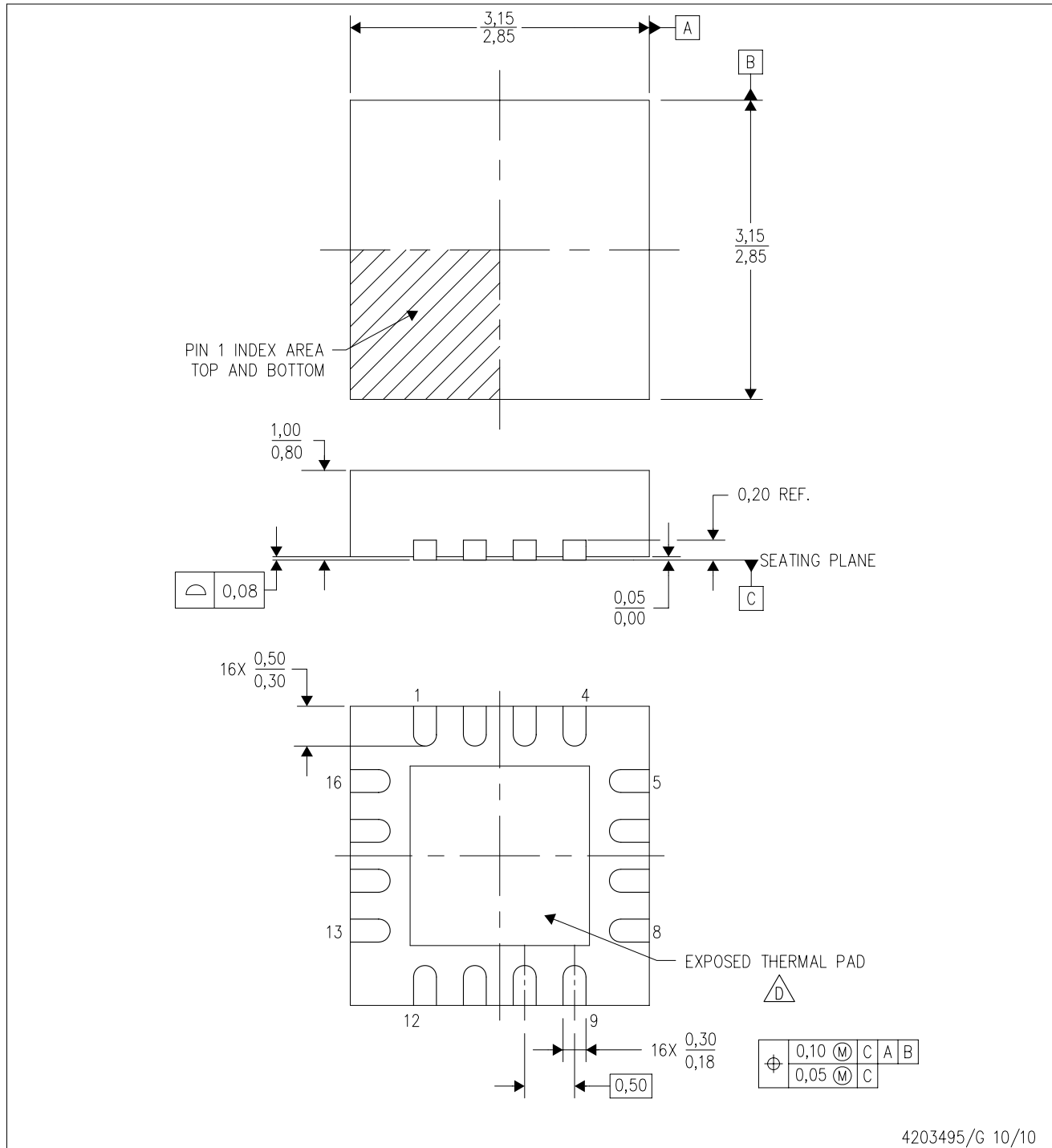
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVP2102RGTR	QFN	RGT	16	3000	340.5	333.0	20.6
CDCLVP2102RGTT	QFN	RGT	16	250	340.5	333.0	20.6


[查询"CDCLVP2102"供应商](#)

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/G 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

PLASTIC QUAD FLATPACK NO-LEAD

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

The exposed thermal pad dimensions for this package are shown in the following illustration.

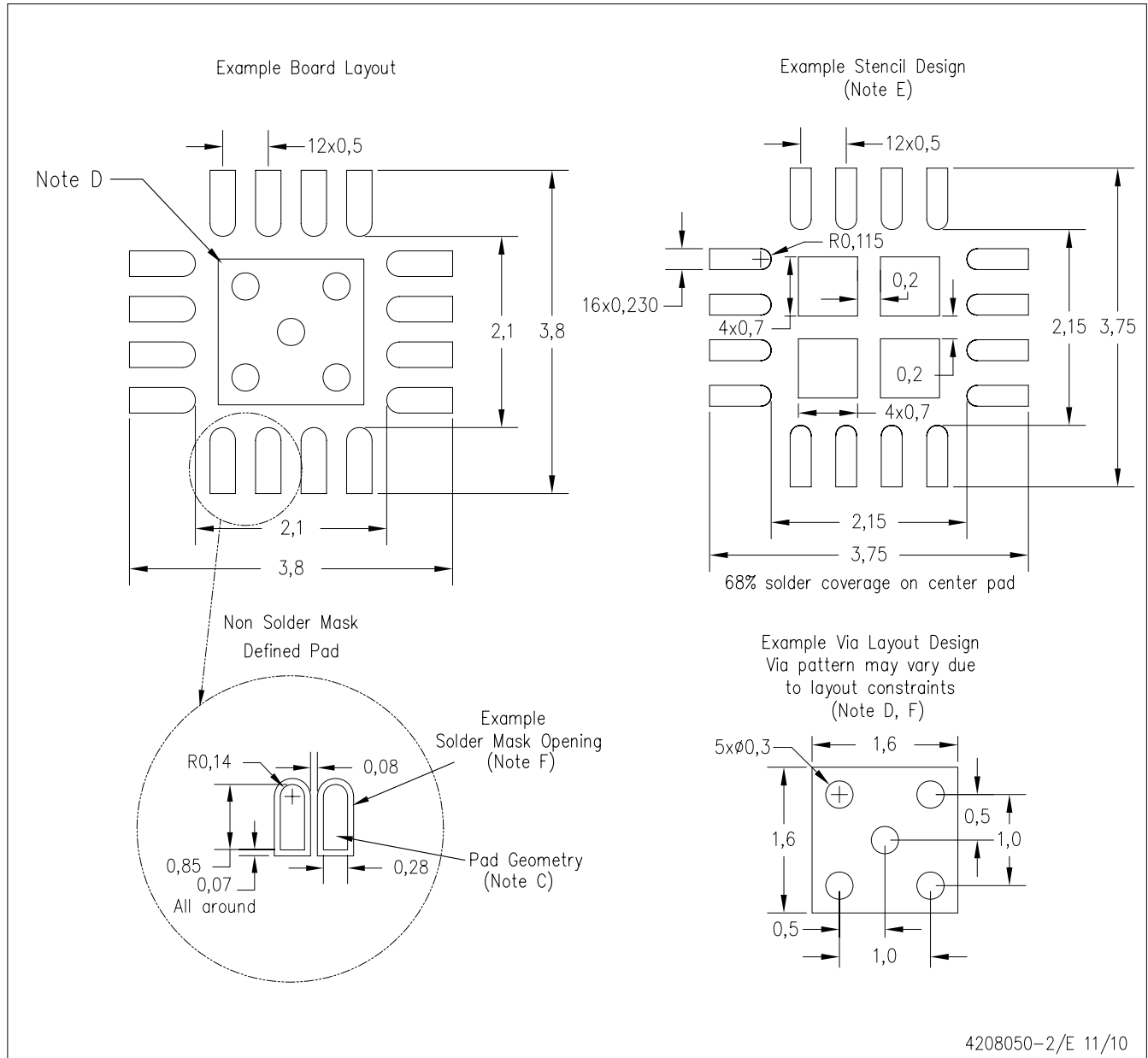


### Exposed Thermal Pad Dimensions

NOTE: A. All linear dimensions are in millimeters

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>	Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Energy	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Space, Avionics & Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>	Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>