REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23										

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
98-06-03

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, MEMORY, DIGITAL, RADIATION-HARDENED, CMOS, LOW VOLTAGE, 128K X 8-BIT STATIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-98615**

SHEET 1 OF 23

DSCC FORM 2233
APR 97

5962-E349-98

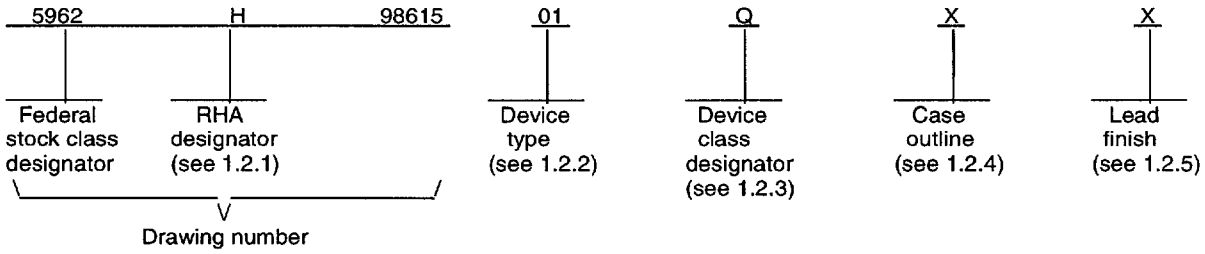
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0037008 938

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Input/output levels	Access time
01	1M8C3V	128K X 8 Rad-Hard CMOS SRAM	CMOS	30 ns
02	1M8C3V	128K X 8 Rad-Hard CMOS SRAM	CMOS	35 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	40	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range (V_{DD})	-0.5 V dc to +5.5 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{DD} + 0.5 V 4/
DC output voltage range(V_{OUT})	-0.5 V dc to V_{DD} + 0.5 V 4/
Storage temperature range	-65°C to +150°C
Case operating temperature range	-55°C to +125°C
Lead temperature (soldering 5 seconds)	+250°C
Thermal resistance, junction-to-case (θ_{JC})	3.5°C/W
Maximum power dissipation	1.3 W
Maximum junction temperature	+150°C

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{DD})	+3.14 V dc to +3.46 V dc
Supply voltage reference (GND)	0.0 V
High level input voltage range (V_{IH})	2.2 V dc to V_{DD}
Low level input voltage range (V_{IL})	0.0 V dc to 0.8 V dc
Case operating temperature range	-55°C to +125°C

1.5 Radiation features

Total dose irradiation	$\geq 1 \times 10^6$ Rads(Si)
Dose rate upset	$\geq 1 \times 10^9$ Rads(Si)/sec
Dose rate survivability	$\geq 1 \times 10^{12}$ Rads(Si)/sec
Single event phenomenon (SEP) effective linear energy threshold (LET) with no upsets	≥ 84 MEV-cm^2/mg
Neutron irradiation	1×10^{14} neutrons/cm^2

1.6 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device.
3/ All voltage are referenced to GND.
4/ Maximum applied voltage shall not exceed +5.5 V.

STANDARDIZATION

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 6.

3.2.7 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.14\ V \le V_{DD} \le 3.46\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage	V_{IH}		1, 2, 3	All	2.2		V
		M,D,L,R,F,G,H	1 1/		2/		
Low level input voltage	V_{IL}		1, 2, 3	All		0.8	V
		M,D,L,R,F,G,H	1 1/			2/	
High level output voltage	V_{OH}	I_{OH} = -4mA	1, 2, 3	All	2.4		V
		I_{OH} = -200µA	1, 2, 3	All	V_{DD} - 0.1 V		
		M,D,L,R,F,G,H	1 1/		2/		
Low level output voltage	V_{OL}	I_{OH} = 8mA	1, 2, 3	All		0.4	V
		I_{OH} = 200µA	1, 2, 3			0.05	
		M,D,L,R,F,G,H	1 1/			2/	
Input leakage current	I_{ILK}	$0\ V \le V_{IN} \le 3.46\ V$	1, 2, 3	All	-5	5	µA
		M,D,L,R,F,G,H	1 1/		2/	2/	
Output leakage current	I_{OLK}	$0\ V \le V_{OUT} \le 3.46\ V$	1, 2, 3	All	-10	10	µA
		M,D,L,R,F,G,H	1 1/		2/	2/	
Operating supply current	I_{DD1}	f= f_{MAX} 3/, $\overline{S}$ = V_{IL} = GND, E = V_{IH} = V_{DD}, I_{OUT} = 0 mA	1, 2, 3	All		180	mA
		M,D,L,R,F,G,H	1 1/			2/	
Supply current (deselected)	I_{DD2}	f= f_{MAX} 3/, $\overline{S}$ = V_{IH} = V_{DD}, E = V_{IL} = GND	1, 2, 3	All		3	mA
		M,D,L,R,F,G,H	1 1/			2/	
Supply current (standby)	I_{DD3}	f= 0Mhz 3/, $\overline{S}$ = V_{IH} = V_{DD}, E = V_{IL} = GND	1, 2, 3	All		3	mA
		M,D,L,R,F,G,H	1 1/			2/	
Data retention current	I_{DR}	V_{DD} = 1.5 V	1, 2, 3	All		1.8	mA
		M,D,L,R,F,G,H	1 1/			2/	
Input capacitance 2/ 4/	C_{IN}	V_{IN} = 0.0 V, f = 1.0 Mhz, T_A = 25°C, see 4.4.1e	4	All		7	pF
Output capacitance 2/ 4/	C_{OUT}	V_{OUT} = 0.0 V, f = 1.0 Mhz, T_A = 25°C, see 4.4.1e	4	All		10	pF
Functional tests		See 4.4.1c	7,8A,8B	All			
		M,D,L,R,F,G,H	7 1/		2/	2/	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.14\ V \le V_{DD} \le 3.46\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle time	t_{AVAV}	See figures 4 and 5 5/	9,10,11	01	30		ns
				02	35		
		M,D,L,R,F,G,H	9 1/	All	2/		
Address access time	t_{AVQV}		9,10,11	01		30	ns
				02		35	
		M,D,L,R,F,G,H	9 1/	All		2/	
Chip select access time	t_{SLQV}		9,10,11	01		30	ns
				02		35	
		M,D,L,R,F,G,H	9 1/	All		2/	
Chip enable access time	t_{EHQV}		9,10,11	01		30	ns
				02		35	
		M,D,L,R,F,G,H	9 1/	All		2/	
Output enable access time	t_{GLQV}		9,10,11	01		12	ns
				02		15	
		M,D,L,R,F,G,H	9 1/	All		2/	
Chip select to output active	t_{SLQX}		9,10,11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Chip enable to output active	t_{EHQX}		9,10,11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Output enable to output active	t_{GLQX}		9,10,11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Output hold after address change	t_{AXQX}		9,10,11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Chip select to output disable	t_{SHQZ}		9,10,11	All		10	ns
		M,D,L,R,F,G,H	9 1/			2/	
Chip disable to output disable	t_{ELQZ}		9,10,11	All		10	ns
		M,D,L,R,F,G,H	9 1/			2/	
Output enable to output disable	t_{GHQZ}		9,10,11	All		10	ns
		M,D,L,R,F,G,H	9 1/			2/	
Write cycle time	t_{AVAV}	See figures 4 and 5 5/ 6/ 7/ 8/	9,10,11	01	30		ns
				02	35		
		M,D,L,R,F,G,H	9 1/	All	2/		
Address setup to end of write	t_{AVWH}		9,10,11	01	25		ns
				02	30		
		M,D,L,R,F,G,H	9 1/	All	2/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.14\ V \le V_{DD} \le 3.46\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip select to end of write	t_{SLWH}	See figures 4 and 5 5/ 6/ 7/ 8/	9,10,11	01	25		ns
				02	30		
		M,D,L,R,F,G,H	9 1/	All	2/		
Chip enable to end of write	t_{EHWH}		9,10,11	01	25		ns
				02	30		
		M,D,L,R,F,G,H	9 1/	All	2/		
Write pulse width access time	t_{WLWH}		9,10,11	01	25		ns
				02	30		
		M,D,L,R,F,G,H	9 1/	All	2/		
Data setup to end of write	t_{DVWH}		9,10,11	01	25		ns
				02	30		
		M,D,L,R,F,G,H	9 1/	All	2/		
Data hold after end of write	t_{WHDX}		9,10,11	All	5		ns
		M,D,L,R,F,G,H	9 1/		2/		
Address setup to start of write	t_{AVWL}		9,10,11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Address hold after end of write	t_{WHAX}		9,10,11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Output active after end of write	t_{WHQX}		9,10,11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Write enable to output disable	t_{WLQZ}		9,10,11	All		10	ns
		M,D,L,R,F,G,H	9 1/			2/	
Write disable pulse width	t_{WHWL}		9,10,11	All	5		ns
		M,D,L,R,F,G,H	9 1/		2/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

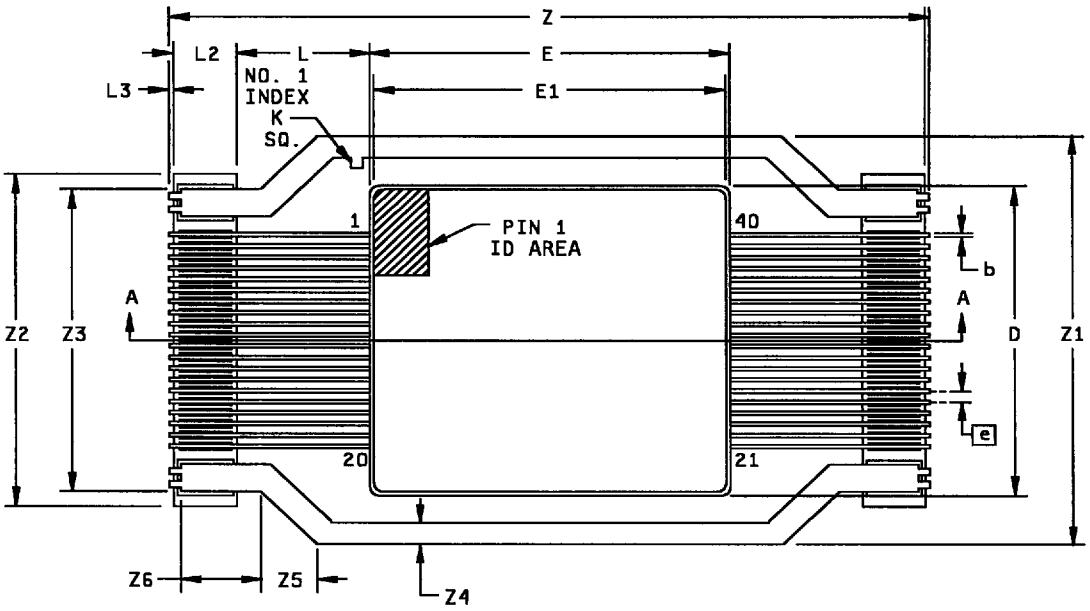
1/ When performing postirradiation electrical measurements for any RHA level T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ± 5°C. The M, D, L, R, F, G, and H in the test condition column are the postirradiation limits for the device types specified in the device types column.
2/ Preirradiation values for RHA marked devices shall also be the postirradiation values unless otherwise specified.
3/ $f_{MAX} = 1/t_{AVAV(min)}$.
4/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ Timing parameters assume input levels from 0 V to V_{DD}, input rise and fall times ≤ 2.0 ns/volt, input and output timing reference levels (except for tristate parameters) of 1.5 V, and input and output timing reference levels for tristate parameters of V_{OL} = 1.23 V and V_{OH} = 2.23 V. See figure 4 for output loading.
6/ $\overline{S}$ high, $\overline{W}$ high, or E low must occur while address transitions.
7/ The worst case timing sequence of $t_{WLQZ} + t_{DVWH} + t_{WHWL} = t_{AVAV}$ (write cycle time).
8/ $\overline{G}$ high will eliminate the I/O output from becoming active (t_{WLQZ}).

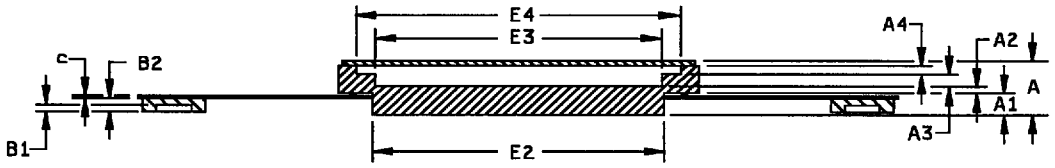
TABLE IB. SEP test limits. 1/ 2/

Device types	T_A = Temperature ±10°C 3/	Memory pattern	V_{DD} = 3.14 V for devices 01,02		Bias for latch-up test V_{DD} = 5.5 V no latch-up LET = 3/
			Effective LET no upsets [MEV/(mg/cm^2)]	Maximum device cross section (cm^2) (LET = 25)	
All	+125°C	4/	≥60	≤ 2E^{-6}	≥177

1/ For SEP test conditions, see 4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature T_A = +125°C.
4/ Testing shall be performed using checkerboard and checkerboard bar test patterns.

Case X





SECTION A-A

FIGURE 1. Case outlines.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316-5000	SIZE A		5962-98615
		REVISION LEVEL	SHEET 10

DSCC FORM 2234
APR 97

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Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.76	3.43	.109	.135
A1	1.27 REF		.050 REF	
A2	0.33	0.43	.013	.017
A3	0.56	0.71	.022	.028
A4	0.46	0.56	.018	.022
b	0.15	0.25	.006	.010
B1	0.38 REF		.015 REF	
B2	0.76 REF		.030 REF	
c	0.10	0.15	.004	.006
D	---	16.76	---	.660
e	0.64 BSC		.025 BSC	
E	19.48	19.89	.767	.783
E1	18.97	19.38	.747	.763
E2	15.88	16.38	.625	.645
E3	13.72 REF		.540 REF	
E4	15.60	15.90	.614	.625
K	0.51 REF		.020 REF	
L	6.86	7.62	.270	.300
L2	3.43 REF		.135 REF	
L3	0.25 REF		.010 REF	
Z	41.53 REF		1.635 REF	
Z1	23.50	24.00	.925	.945
Z2	19.10	19.51	.752	.768
Z3	17.78 REF		.700 REF	
Z4	1.27 REF		.050 REF	
Z5	3.05 REF		.120 REF	
Z6	3.96 REF		.156 REF	

NOTE: Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.

FIGURE 1. Case outlines - continued.

Device types	All
Case outline	X
Terminal no.	Terminal symbol
1	A_0
2	GND
3	V_{DD}
4	A_{12}
5	A_{11}
6	A_9
7	A_{10}
8	A_2
9	A_1
10	A_{13}
11	A_{14}
12	A_{15}
13	A_{16}
14	DQ_0
15	DQ_1
16	DQ_2
17	NC
18	V_{DD}
19	GND
20	NC
21	NC
22	GND
23	V_{DD}
24	DQ_3
25	DQ_4
26	DQ_5
27	DQ_6
28	DQ_7
29	$\overline{S}$
30	A_4
31	$\overline{G}$
32	A_8
33	A_7
34	A_6
35	A_5
36	$\overline{E}$
37	$\overline{W}$
38	V_{DD}
39	GND
40	A_3

FIGURE 2. Terminal connections.

Mode	Inputs 1/ 2/					Power
	E	$\overline{S}$	$\overline{W}$	$\overline{G}$	I/O	
Write	High	Low	Low	X	Data in	Active
Read	High	Low	High	Low	Data out	Active
Standby	X	High	X	X	High Z	Standby
Standby 3/	Low	X	X	X	High Z	Standby

1/ V_{IN} for Don't care (X) inputs = V_{IL} or V_{IH}.
2/ When $\overline{G}$ = high, I/O is high Z.
3/ To dissipate the minimum amount of standby power when in standby mode: $\overline{S} = V_{DD}$ and E = GND. All other input levels may float.

FIGURE 3. Truth table.

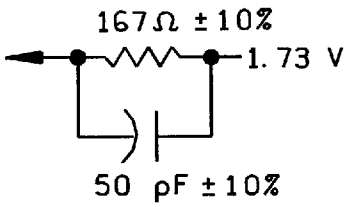


FIGURE 4. Output load circuit.

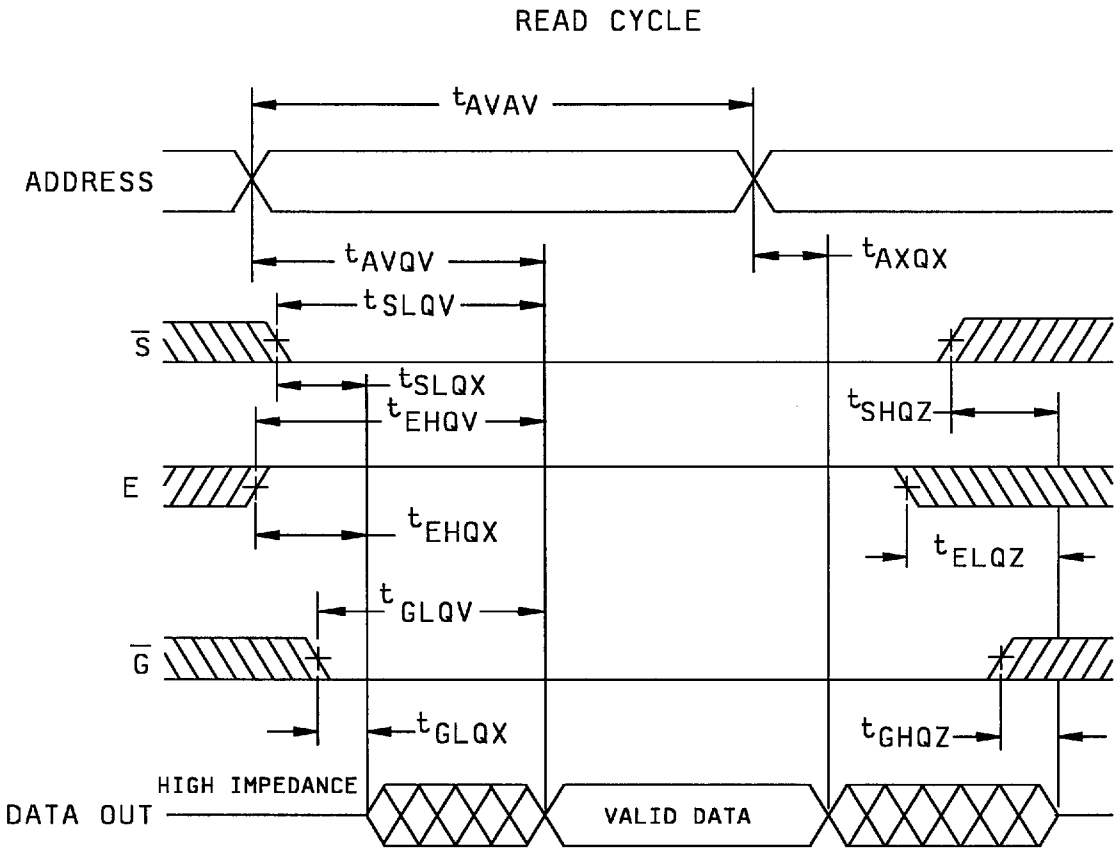


FIGURE 5. Timing waveforms.

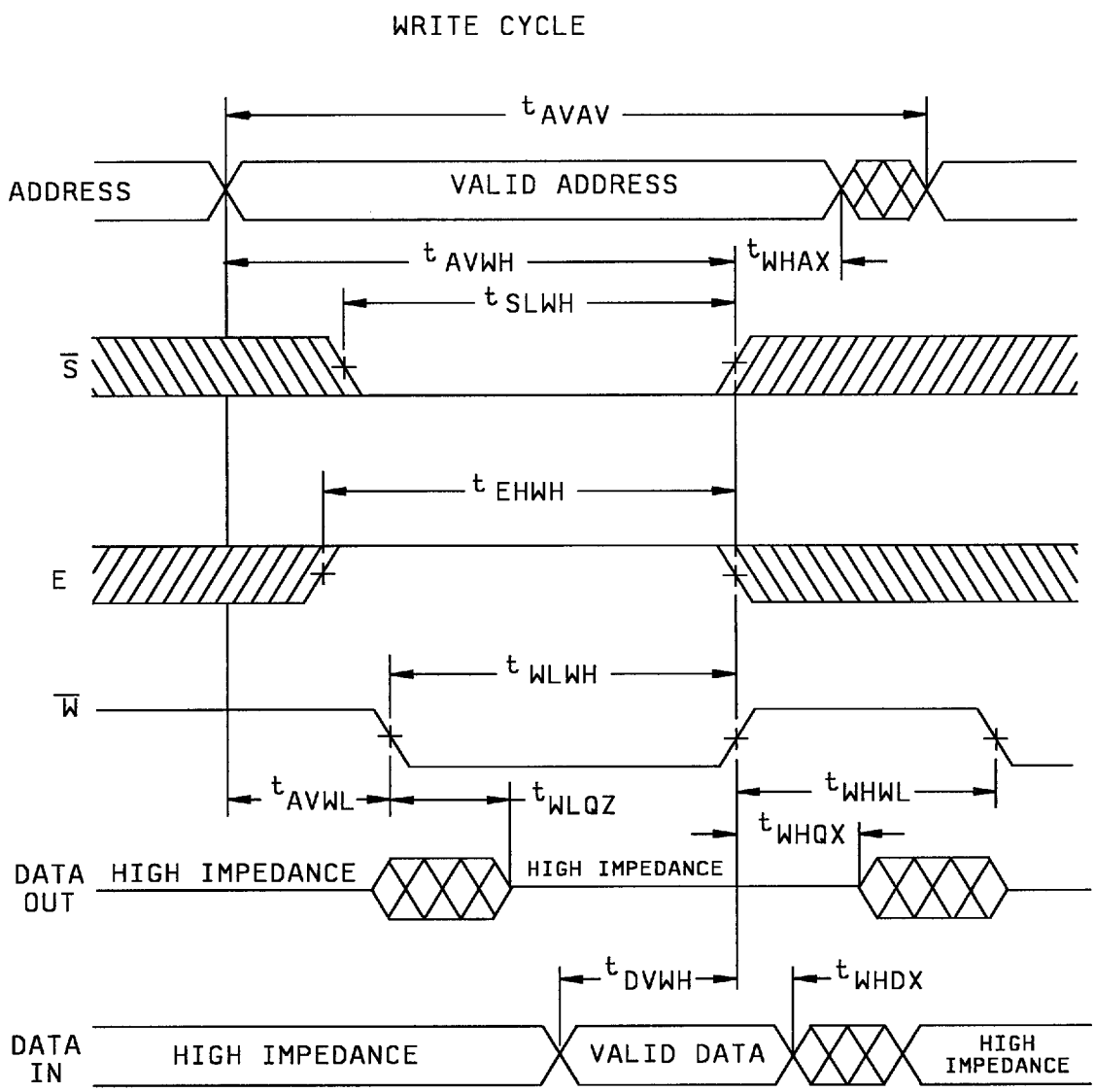
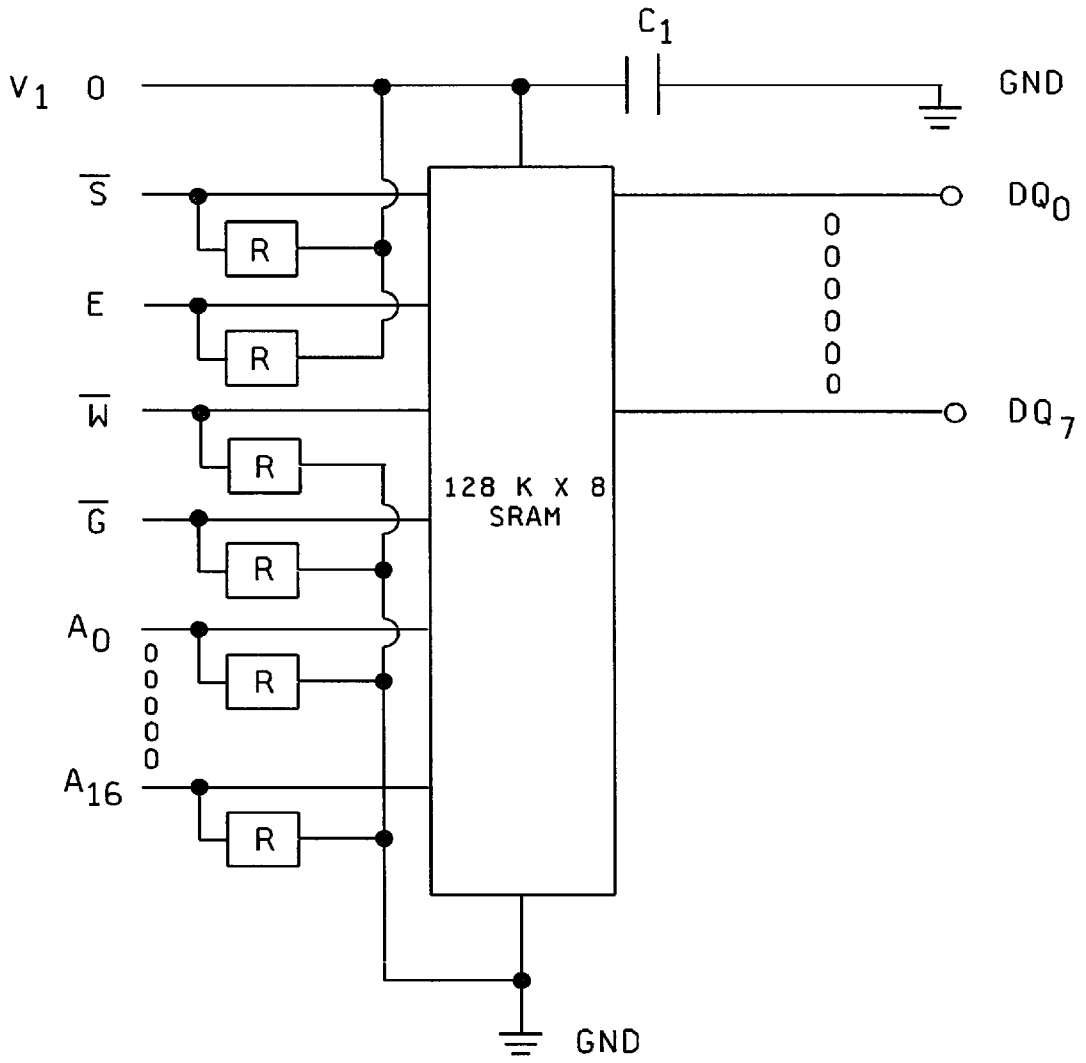


FIGURE 5. Timing waveforms - continued.



NOTE: C_1 = 0.1 µF, R = 1.6 kΩ.

FIGURE 6. Radiation exposure circuit - continued.

Table IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table IA)	Subgroups (per MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I and II method 1015	Not required	Not required	Not required
3	Same as line 1			1*,7* Δ*
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ*
6	Final electrical parameters	1*,2,3,7*,8A, 8B,9,10,11	1*,2,3,7*,8A, 8B,9,10,11	1*,2,3,7*,8A, 8B,9,10,11
7	Group A test requirements	1,2,3,4**,7,8A, 8B,9,10,11	1,2,3,4**,7,8A, 8B,9,10,11	1,2,3,4**,7,8A, 8B,9,10,11
8	Group C end-point electrical parameters	1,2,3,7,8A,8B	1,2,3,7,8A,8B	1,2,3,7,8A, 8B,9,10,11 Δ
9	Group D end-point electrical parameters	1,7,9	1,7,9	1,7,9
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate test are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * Indicates PDA applies to subgroups 1, 7, and Δ.
5/ ** See 4.4.1e.
6/ Δ Indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.5.

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I_{DD2} standby	±10% of specified value in table IA
I_{ILK}, I_{OLK}	±10% of specified value in table IA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4. QUALITY ASSURANCE REQUIREMENTS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

Q/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters shall be as specified in table IIA herein. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters for class T devices shall be as specified in the table I, Group A subgroups, or as modified in the QM plan.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein. Test shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Transient dose rate upset testing. Transient dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be greater than 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{DD} = 3.14 V dc for the upset measurements and V_{DD} = 3.46 V dc for the latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits see table IB herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

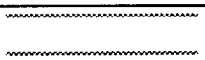
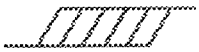
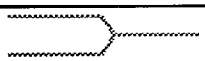
6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

30.3 Algorithm C (pattern 3).

30.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-06-03

Approved sources of supply for SMD 5962-98615 are listed below for immediate acquisition only and shall be added to QML-38535 and MIL-HDBK-103 during the next revision. QML-38535 and MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38535 and MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9861501QXC 5962H9861501VXC	52088	LM1M8C3VRH-Q30X LM1M8C3VRH-V30X
5962H9861502QXC 5962H9861502VXC	52088	LM1M8C3VRH-Q35X LM1M8C3VRH-V35X

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
52088	Lockheed Martin Federal Systems, Incorporated 9500 Godwin Drive Manassas, VA 20110-4157

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.