MOTOROLA

MC34062
MC35062

Advance Information

3

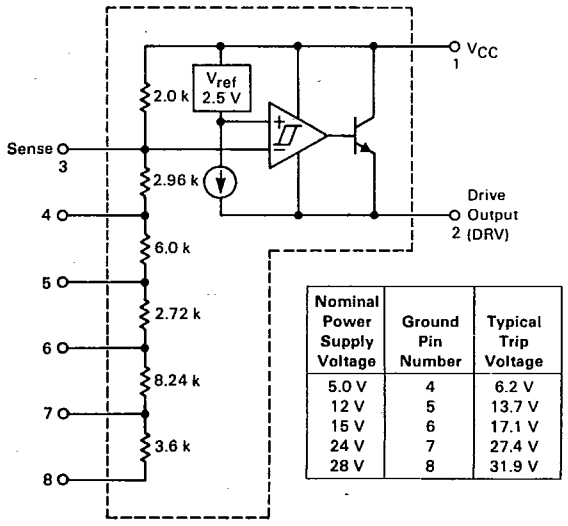
PIN-PROGRAMMABLE OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

The MC34062/35062 overvoltage protection (OVP) circuits require only an external "crowbar" SCR to protect sensitive electronic circuitry from overvoltage damage. They sense an overvoltage condition and quickly "crowbar", or short circuit, the supply. An on-chip, tapped resistor network allows the device to be programmed for trip voltages ranging from 3.5 to 40 V. Each of the five programming pins provides one standard overvoltage trip point for nominal power supply voltages of 5.0, 12, 15, 24 or 28 V. Many other trip voltages may be programmed by interconnecting and grounding various combinations of these programming pins. Tables are provided in the Applications Information which show connection schemes for 120 trip voltages.

These circuits provide a cost-effective means of protecting either positive or negative power supplies. In addition, an external capacitor may be used to program a minimum overvoltage duration before tripping, thus providing noise immunity. The unique design of the MC34062/35062 eliminates voltage and temperature drift errors due to SCR gate variations.

- Unique Pin-Programmable Trip Voltage from 3.5 to 40 V
- One-Pin Programming for 5.0, 12, 15, 24 and 28 V Power Supplies
- SCR Gate Drive Output of 200 mA
- Built-In Hysteresis Voltage
- Wide Supply Range: 4.0 V ≤ V_{CC} ≤ 40 V

FUNCTIONAL BLOCK DIAGRAM



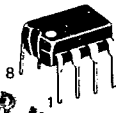
Nominal Power Supply Voltage	Ground Pin Number	Typical Trip Voltage
5.0 V	4	6.2 V
12 V	5	13.7 V
15 V	6	17.1 V
24 V	7	27.4 V
28 V	8	31.9 V

Pins 4 through 8 are used to program the Trip Voltage, V_{trip}

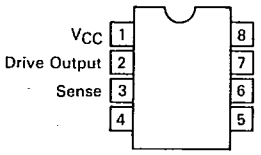
PIN-PROGRAMMABLE OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
(MC34062 only)



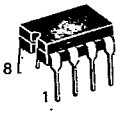
"NOT FOR NEW DESIGN-INS"



Note: Pins 4 thru 8 are used to program the Trip Voltage, V_{trip}

(Top View)

U SUFFIX
CERAMIC PACKAGE
CASE 693-02



ORDERING INFORMATION

Device	Temperature Range	Package
MC35062U	-55 to +125°C	Ceramic DIP
MC34062P1	0 to +70°C	Plastic DIP
MC34062U		Ceramic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC34062, MC35062

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating Voltage	$V_{CC} - V_{DRV}$	40	Vdc
Voltage Across Any Internal Resistor In Network	V_{RN}	40	Vdc
Current Through Any Resistor In Network	I_{RN}	10	mA
Sense Voltage	V_{Sense}	40	Vdc
Drive Output Current	I_{DRV}	Internally Limited	mA
Operating Ambient Temperature MC34062 MC35062	T_A	 0 to +70 -55 to +125	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-65 to +150°C	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V; V_{DRV} = 0 V; T_A = T_{low} to T_{high} unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage Range	$V_{CC} - V_{DRV}$	3.0	—	40	Vdc
Sense Trip Voltage T_A = 25°C T_{low} to T_{high}	V_{Sense}	 2.425 2.375	 2.5 2.5	 2.575 2.625	Vdc
Line Regulation, V_{Sense} (3.0 V ≤ $V_{CC} - V_{DRV}$ ≤ 40 V) T_A = 25°C T_{low} to T_{high}	Reg_{line}	 — —	 0.001 0.001	 0.01 0.02	%/V
Trip Voltage (Pin 4 = Gnd; V_{DRV} = 0 V) T_A = 25°C T_{low} to T_{high}	$V_{trip(4)}$	 6.01 5.89	 6.2 6.2	 6.39 6.51	V
Hysteresis Voltage (Pin 4 = Gnd; V_{DRV} = 0 V)	$V_{H(4)}$	—	0.62	—	V
Trip Voltage (Pin 5 = Gnd; V_{DRV} = 0 V) T_A = 25°C T_{low} to T_{high}	$V_{trip(5)}$	 13.3 13.0	 13.7 13.7	 14.1 14.4	V
Hysteresis Voltage (Pin 5 = Gnd; V_{DRV} = 0 V)	$V_{H(5)}$	—	1.37	—	V
Trip Voltage (Pin 6 = Gnd; V_{DRV} = 0 V) T_A = 25°C T_{low} to T_{high}	$V_{trip(6)}$	 16.6 16.2	 17.1 17.1	 17.6 18.0	V
Hysteresis Voltage (Pin 6 = Gnd; V_{DRV} = 0 V)	$V_{H(6)}$	—	1.71	—	V
Trip Voltage (Pin 7 = Gnd; V_{DRV} = 0 V) T_A = 25°C T_{low} to T_{high}	$V_{trip(7)}$	 26.6 26.0	 27.4 27.4	 28.2 28.8	V
Hysteresis Voltage (Pin 7 = Gnd; V_{DRV} = 0 V)	$V_{H(7)}$	—	2.74	—	V
Trip Voltage (Pin 8 = Gnd; V_{DRV} = 0 V) T_A = 25°C T_{low} to T_{high}	$V_{trip(8)}$	 30.9 30.3	 31.9 31.9	 32.9 33.5	V
Hysteresis Voltage (Pin 8 = Gnd; V_{DRV} = 0 V)	$V_{H(8)}$	—	3.19	—	V
Resistor Network Current at Nominal Power Supply Voltage V_{CC} = 28 V; V_{DRV} = 0 V; Pin 8 = Gnd	I_{RN}	0.5	1.1	2.0	mA
Drive Output Current, ON State T_J = 25°C T_{low} to T_{high}	$I_{DRV(on)}$	 130 90	 200 —	 300 350	mA
Drive Output Current, OFF State V_{CC} = 5.0 V; V_{DRV} = 0 V 3.0 V ≤ $V_{CC} - V_{DRV}$ ≤ 40 V	$I_{DRV(off)}$	 0.2 0.2	 0.6 0.6	 1.0 1.5	mA
Drive Output Current Slew Rate (T_A = 25°C)	di/dt	—	2.0	—	A/μs
Drive Output V_{CC} Transient Rejection V_{CC} = 0 V to 15 V at dV/dt = 200 V/μs; V_{DRV} = 0 V; V_{Sense} = 0 V; T_A = 25°C	$\Delta I_{DRV(trans)}$	—	1.0	—	mA (Peak)
Propagation Delay Time (T_A = 25°C; 500 mV Overdrive)	t_{PLH}	—	500	—	ns

T_{low} = -55°C for MC35062 = 0°C for MC34062 T_{high} = +125°C for MC35062 = + 70°C for MC34062

MC34062, MC35062

3

FIGURE 1 — STANDARD TEST CIRCUIT

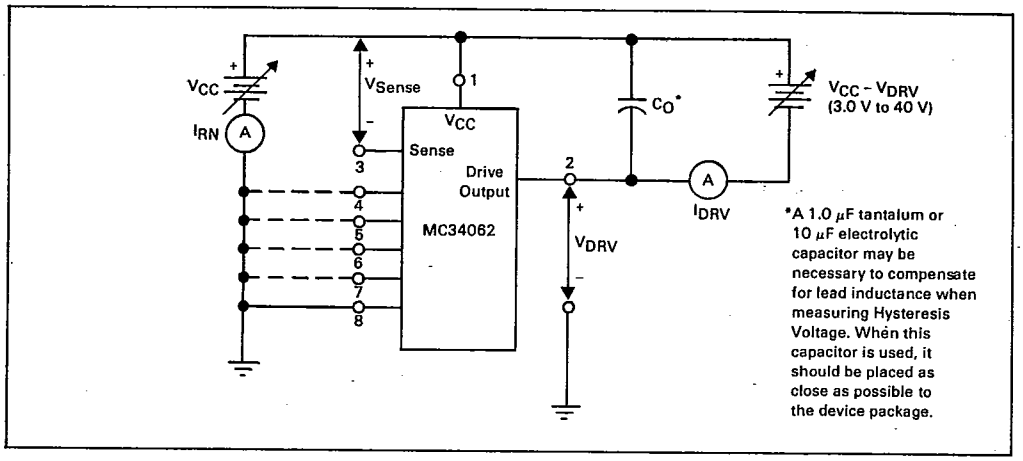


FIGURE 2 — DRIVE CURRENT versus NORMALIZED RESISTOR DIVIDER VOLTAGE
(Normalized to V_{trip} at T_A = 25°C)

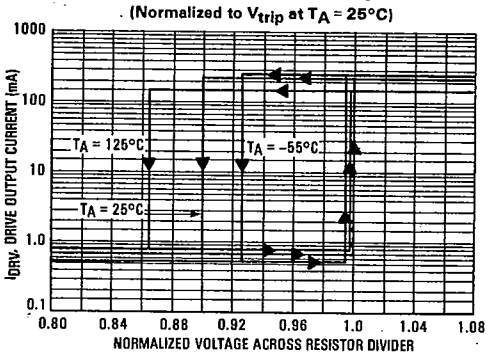


FIGURE 3 — NORMALIZED TRIP VOLTAGE versus TEMPERATURE
(Normalized to T_A = 25°C)

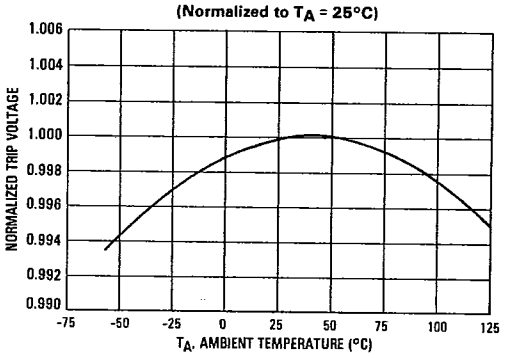


FIGURE 4 — OFF STATE DRIVE CURRENT versus SUPPLY VOLTAGE

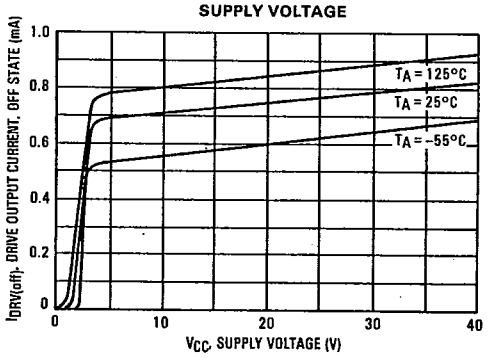
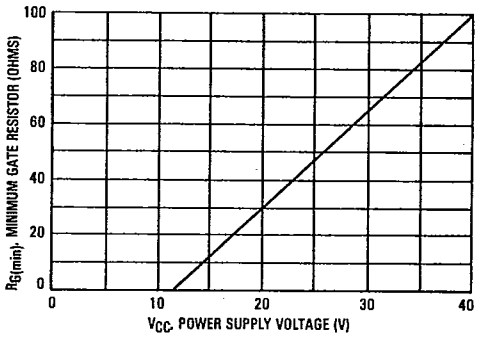


FIGURE 5 — MINIMUM R_G versus SUPPLY VOLTAGE



查询"MC34062"供应商

FIGURE 6 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 5.0 V POWER SUPPLY

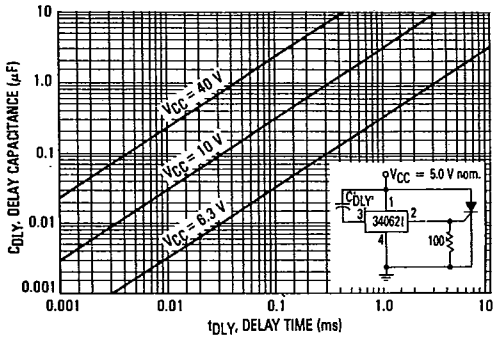


FIGURE 7 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 12 V POWER SUPPLY

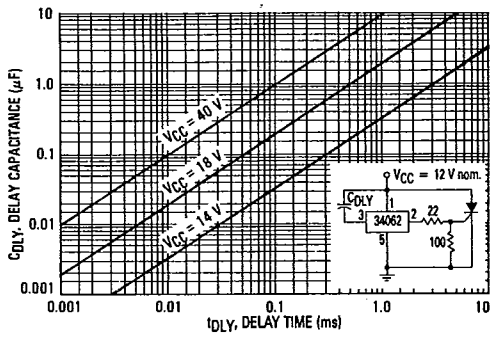


FIGURE 8 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 15 V POWER SUPPLY

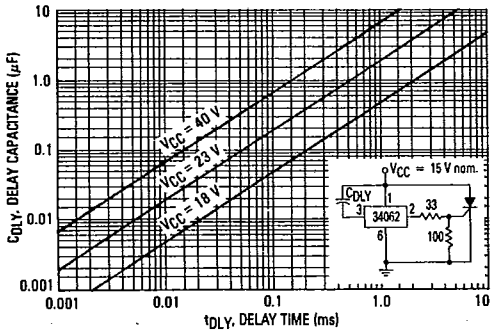


FIGURE 9 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 24 V POWER SUPPLY

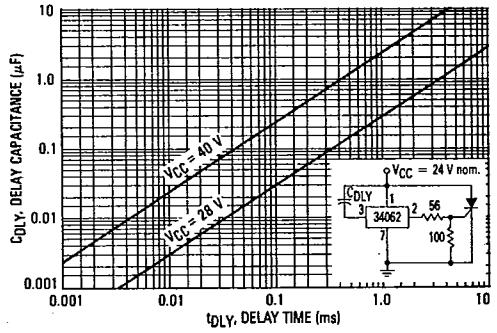
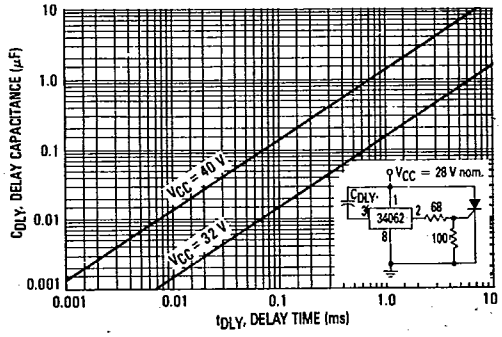


FIGURE 10 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 28 V POWER SUPPLY



APPLICATIONS INFORMATION

BASIC CIRCUIT CONFIGURATION

The MC34062 and MC35062 each consist of a 2.5 V shunt reference, a comparator with built-in hysteresis, a power output transistor, and an on-chip, tapped resistor network. In the typical application of Figure 11 the voltage at the inverting input of the comparator is $\frac{V_{CC} R_2}{R_1 + R_2}$, while the voltage at the non-inverting input is $V_{CC} - 2.5$ V. Thus, for a given (R_1, R_2) voltage divider, the comparator's output state is a function of V_{CC}. The following table applies:

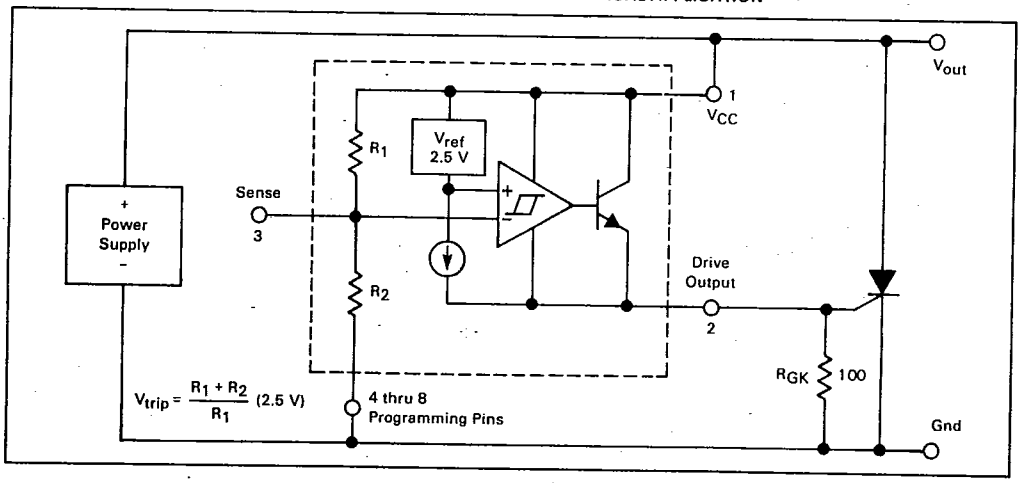
V_{CC}	Drive Output
$< \frac{R_1 + R_2}{R_1}$ (2.5 V)	OFF State
$> \frac{R_1 + R_2}{R_1}$ (2.5 V)	ON State

By making the proper choice of R_1 and R_2, a level detector for any voltage from 3.5 to 40 V may be realized.

The on-chip resistor network is configured as shown in the Functional Block Diagram on the front page of this data sheet. Each of the five programming pins (4 through 8) provides one standard overvoltage trip point for nominal power supply voltages of 5.0, 12, 15, 24 or 28 V. These standard trip points are implemented by grounding one of the five programming pins, and are summarized in the following table:

Nominal Power Supply Voltage	Ground Pin Number	Typical Trip Voltage
5.0 V	4	6.2 V
12 V	5	13.7 V
15 V	6	17.1 V
24 V	7	27.4 V
28 V	8	31.9 V

FIGURE 11 — BLOCK DIAGRAM AND TYPICAL APPLICATION



Many other trip voltages may be programmed by interconnecting and grounding various combinations of the programming pins. Table 1 provides connection schemes for 120 nominal Trip Voltages (V_{trip}). Additional Trip Voltages may also be implemented with other pin connections. All of these Trip Voltages will be within ±3.0% of the nominal value at $T_A = 25°C$ and within ±5.0% over the operating temperature range.

The hysteresis built into the comparator is 250 mV at the inverting input. This comparator hysteresis voltage is multiplied by the ratio $\frac{R_1 + R_2}{R_1}$, just as the 2.5 V Sense Trip Voltage (V_{Sense}) is multiplied by the same ratio to define the Trip Voltage (V_{trip}). Thus, the Hysteresis Voltage (V_H) is approximately 10% of the Trip Voltage for any Trip Voltage.

Some precautions are necessary in the operation of the protection circuit shown in Figure 11. Note that even in the OFF State, a minimum drive output current, equal to the sum of the reference and comparator supply currents, is available. Therefore, a means of shunting this current away from the driven circuit is necessary. In the example of Figure 11; a 100 Ω resistor (R_{GK}) is used, producing a voltage at the Drive Output of approximately 60 mV in the OFF State.

In the ON State the MC34062 becomes a current source capable of saturating to within 2.0 V of V_{CC}. Therefore, when driving a high impedance load, it may be desirable to clamp the drive output to at least 3.0 V below V_{CC} ($V_{CC} - V_{DRV} \geq 3.0$ V) if it is important that the reference continue to regulate.

PROGRAMMING A MINIMUM OVERVOLTAGE DURATION BEFORE TRIPPING

A time delay may be programmed into the operation of the MC34062/35062 to provide noise immunity. This time delay is implemented by adding a capacitor (C_{DLY}) between the V_{CC} and Sense leads as shown in Figure 12. The time delay obtained by this technique is a function of the internal resistors (R_1, R_2) and C_{DLY}, as well as the nominal supply voltage, $V_{CC(nom)}$, and the overvoltaged supply voltage V_{CC}. The nominal supply voltage determines the initial charge on C_{DLY}, while the magnitude of the overvoltage condition determines the rate at which C_{DLY} charges to the reference voltage, $V_{ref} = 2.5$ V. Thus, for a given R_1, R_2 and C_{DLY}, the time delay is reduced as the overvoltage is increased. The expression for the time delay, t_{DLY} is:

$$t_{DLY} = \frac{R_1 R_2 C_{DLY}}{R_1 + R_2} \ln \left[\frac{V_{CC} - V_{CC(nom)}}{V_{CC} - V_{trip}} \right]$$

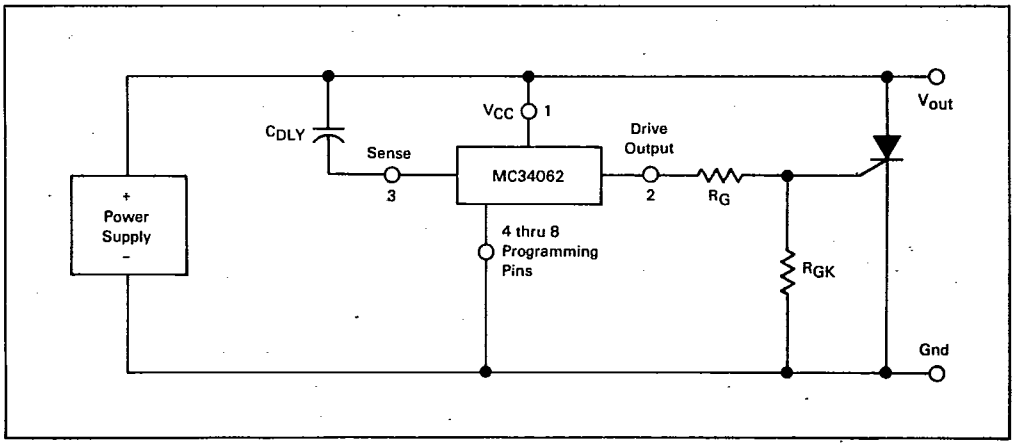
where: $V_{trip} = \frac{R_1 + R_2}{R_1}(2.5\ V)$

Figures 6 through 10 show the C_{DLY} values versus delay time (t_{DLY}) for nominal 5.0, 12, 15, 24 and 28 V power supply protection circuits, each using a one-pin MC34062/35062 programming scheme. These figures also show the change in t_{DLY} with variations in the overvoltaged supply, V_{CC}.

THE NEED FOR A GATE RESISTOR

For power supplies above 11 V, a gate resistor, R_G, in series with the SCR gate is recommended to limit the power dissipated by the IC to approximately 2.0 W. This resistor will protect the MC34062/35062 in the event of a defective or missing SCR, while allowing the maximum drive output current to the gate of the SCR. Figure 5 shows the minimum recommended gate resistor, $R_{G(min)}$, versus the power supply voltage, V_{CC}. A larger value of R_G may be used if less drive current is needed.

FIGURE 12 — OVERVOLTAGE PROTECTION WITH TIME DELAY



MC34062, MC35062

3

TABLE 1 — PIN-PROGRAMMING OF RESISTOR NETWORK FOR NOMINAL TRIP VOLTAGES

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
3.483		Gnd		Gnd		Gnd
3.632		Gnd	Gnd		Gnd	
3.768		Gnd		Gnd		
3.807		Gnd		Gnd		
3.883		Gnd			Gnd	
3.923			Gnd		Gnd	
4.012		Gnd	Gnd		Gnd	
4.098		Gnd				Gnd
4.130				Gnd		Gnd
4.196		Gnd		Gnd		Gnd
4.272		Gnd	Gnd			
4.353		Gnd				Gnd
4.407			Gnd		Gnd	
4.520			Gnd			Gnd
4.598		Gnd			Gnd	
4.673				Gnd		Gnd
4.709			Gnd	Gnd		Gnd
4.845		Gnd		Gnd		
4.947			Gnd	Gnd		Gnd
4.996			Gnd		Gnd	

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
5.101			Gnd			Gnd
5.222		Gnd		Gnd		
5.328		Gnd				
5.413		Gnd	Gnd			
5.563		Gnd				
5.673		Gnd				
5.734		Gnd				
5.887					Gnd	
5.900				Gnd		
5.991			Gnd			
6.092					Gnd	
6.200		Gnd				
6.311					Gnd	
6.610					Gnd	
6.703				Gnd		
6.840			Gnd	Gnd		
7.000						Gnd
7.132			Gnd			
7.298				Gnd		
7.347			Gnd			

TABLE 1 — (Continued)

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
7.478			Gnd	Gnd		
7.799			Gnd			
8.106			Gnd		Gnd	
8.220			Gnd			Gnd
8.409			Gnd	Gnd		Gnd
8.539			Gnd			
8.633				Gnd		Gnd
8.756				Gnd		
8.870			Gnd	Gnd		
8.906						Gnd
9.013			Gnd		Gnd	
9.178						Gnd
9.331		V_{CC}		Gnd		
9.377			Gnd			
9.385				Gnd	Gnd	
9.433			Gnd			
9.600				Gnd		
9.826				Gnd		
9.912					Gnd	
10.000			Gnd			

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
10.400						Gnd
10.540			Gnd	Gnd		
10.700						Gnd
11.047			Gnd			
11.178			Gnd	Gnd		
11.496				Gnd		
11.630				Gnd		Gnd
11.895				Gnd		V_{CC}
11.937				Gnd	Gnd	
12.086			Gnd			V_{CC}
12.477				Gnd		
12.556				Gnd		
12.732					Gnd	
12.800					Gnd	
13.387					Gnd	
13.400				Gnd		
13.700			Gnd			
14.233					Gnd	
14.500						Gnd
15.330				Gnd		Gnd

TABLE 1 — (Continued)

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
15.637				Gnd	Gnd	
16.200					Gnd	
16.256				Gnd		
16.465				Gnd		
16.500					Gnd	
16.532					Gnd	
16.832					Gnd	
17.087					Gnd	
17.100				Gnd		
17.300						Gnd
17.900						Gnd
18.200						Gnd
18.733						Gnd
19.900					Gnd	
20.232					Gnd	
20.300					Gnd	
20.700						Gnd
21.000						Gnd
21.600						Gnd
22.122		V_{CC}			Gnd	

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
22.673			V_{CC}		Gnd	
23.700					Gnd	
23.807			V_{CC}		Gnd	
24.000					Gnd	
24.283			V_{CC}			Gnd
24.400						Gnd
24.800						Gnd
25.211				Gnd	V_{CC}	
27.333		V_{CC}	V_{CC}		Gnd	
27.400					Gnd	
28.200						Gnd
28.500						Gnd
30.023		V_{CC}			Gnd	
30.694		V_{CC}				Gnd
31.486			V_{CC}			Gnd
31.900						Gnd
32.233		V_{CC}				Gnd
33.116			V_{CC}			Gnd
38.182		V_{CC}	V_{CC}			Gnd
39.064		V_{CC}				Gnd

CROWBAR SCR CONSIDERATIONS

Referring to Figure 13, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 13A, the supply's input filter capacitors. This surge current is illustrated in Figure 14, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 $A/\mu s$, assuming a gate current of five times I_{GT} and $<1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 15. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 13 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS

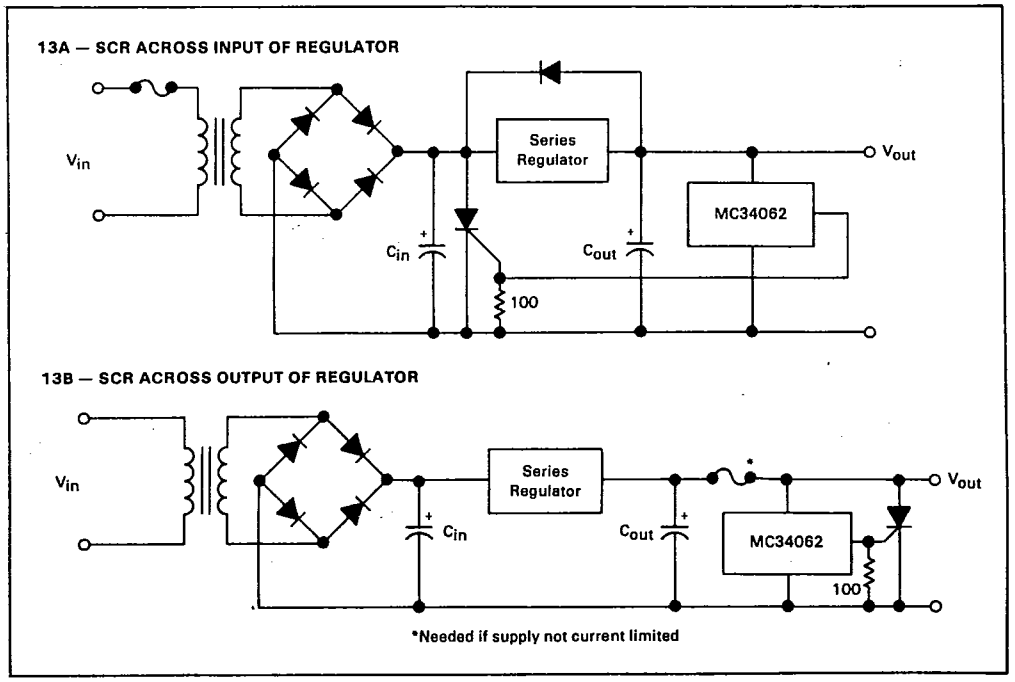
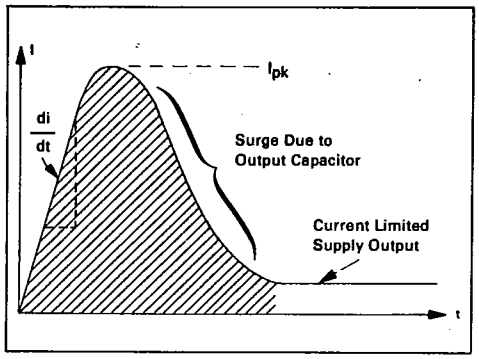


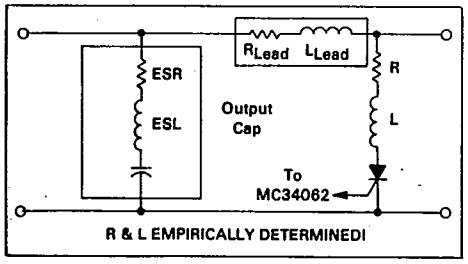
FIGURE 14 — CROWBAR SCR SURGE CURRENT WAVEFORM



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 15) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 15 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 13A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 13B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.