Power MOSFET

-30 V, -4.7 A, Single P-Channel, TSOP-6

Features

- Leading -30 V Trench Process for Low R_{DS(on)}
- Low Profile Package Suitable for Portable Applications
- Surface Mount TSOP-6 Package Saves Board Space
- Improved Efficiency for Battery Applications
- Pb-Free Package is Available

Applications

- Battery Management and Switching
- Load Switching
- Battery Protection

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

INAMINOM TIATITICO (1) = 25 O unicos outerwise noted)						
Rating	Symbol	Value	Unit			
Drain-to-Source Voltage			V_{DSS}	-30	V	
Gate-to-Source Voltage			V_{GS}	±20	V	
Continuous Drain			I _D	-3.7	Α	
Current (Note 1)	State	T _A = 85°C		-2.7		
	t ≤ 5 s	T _A = 25°C		-4.7		
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.25	W	
	t ≤ 5 s			2.0		
Continuous Drain	Steady	T _A = 25°C	I _D	-2.6	Α	
Current (Note 2)	State	T _A = 85°C		-1.9		
Power Dissipation (Note 2)	T _A = 25°C		P _D	0.63	W	
Pulsed Drain Current tp = 10 μs			I_{DM}	-15	Α	
Operating Junction and Storage Temperature			T _J , T _{STG}	–55 to 150	°C	
Source Current (Body Diod	I _S	-1.7	Α			
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C	

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	100	°C/W
Junction-to-Ambient – $t \le 5$ s (Note 1)	$R_{\theta JA}$	62.5	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	200	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.006 in sq).

1

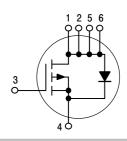


ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX	
-30 V	38 mΩ @ –10 V	-4.7 A	
	68 mΩ @ -4.5 V		

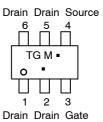
P-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



TSOP-6 CASE 318G STYLE 1



TG = Specific Device Code

M = Date Code*

= Pb-Free Package

(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping [†]
NTGS4111PT1	TSOP-6	3000 / Tape & Reel
NTGS4111PT1G	TSOP-6 (Pb-Free)	3000 / Tape& Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTGS4111P

ELECTRICAL 4CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D$	= -250 μA	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				-17		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{G9} = 0 V.	T _J = 25°C			-1.0	μΑ
		$V_{GS} = 0 \text{ V},$ $V_{DS} = -24 \text{ V}$	T _J = 125°C			-100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V				±100	nA
ON CHARACTERISTICS (Note 3)	•				-	•	•
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _E	₎ = -250 μA	-1.0		-3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				5.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = -10 \text{ V},$	I _D = -3.7 A		38	60	mΩ
		$V_{GS} = -4.5 \text{ V},$	$I_D = -2.7 \text{ A}$		68	110	┦
Forward Transconductance	9FS	$V_{DS} = -10 \text{ V},$	I _D = -3.7 A		6.0		S
CHARGES, CAPACITANCES AND GATE RE	SISTANCE						
Input Capacitance	C _{ISS}				750		pF
Output Capacitance	C _{OSS}	$V_{GS} = 0 \text{ V, f} = V_{DS} = 0$			140		1
Reverse Transfer Capacitance	C _{RSS}	V _{DS} = −15 V			105		1
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = -10 \text{ V}, V_{DD} = -15 \text{ V},$ $I_{D} = -3.7 \text{ A}$			15.25	32	nC
Threshold Gate Charge	Q _{G(TH)}				0.8		1
Gate-to-Source Charge	Q _{GS}				2.6		
Gate-to-Drain Charge	Q_{GD}				3.4		
SWITCHING CHARACTERISTICS, VGS = -1	0 V (Note 4)						
Turn-On Delay Time	t _{d(ON)}				9.0	17	ns
Rise Time	t _r	$V_{GS} = -10 \text{ V}, V_{DD} = -15 \text{ V},$ $I_{D} = -1.0 \text{ A}, R_{G} = 6.0 \Omega$			9.0	18	
Turn-Off Delay Time	t _{d(OFF)}				38	85	
Fall Time	t _f				22	45	
SWITCHING CHARACTERISTICS, VGS = -4	I.5 V (Note 4)						
Turn-On Delay Time	t _{d(ON)}				11	20	ns
Rise Time	t _r	V _{GS} = -4.5 V, \	/nn = -15 V.		15	28	
Turn-Off Delay Time	t _{d(OFF)}	$I_D = -1.0 \text{ A}, R_G = 6.0 \Omega$			28	56	
Fall Time	t _f				22	50	
DRAIN - SOURCE DIODE CHARACTERIST	ics				-	•	•
Characteristic	Symbol	Test Condition		Min	Тур	Max	Unit
Forward Diode Voltage	V _{DS}	V _{GS} = 0 V,	T _J = 25°C		-0.76	-1.2	V
		$I_{S} = -1.0 \text{ A}$	T _J = 125°C		-0.60		1
Reverse Recovery Time	t _{RR}		•		17	40	ns
	ł — — — — — — — — — — — — — — — — — — —				1	ł	-1

Charge Time

Discharge Time

Reverse Recovery Charge

ta

 t_{b}

Q_{RR}

 $\begin{aligned} V_{GS} &= 0 \ V \\ dI_S/dt &= 100 \ A/\mu s, \ I_S &= -1.0 \ A \end{aligned}$

9.0

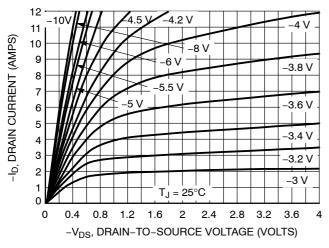
8.0

8.0

nC

Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

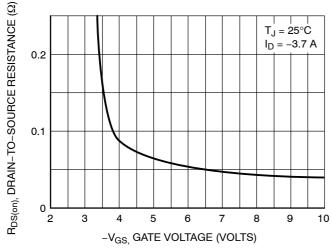
查询"NTGS4111P-D"供应的 PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)



 $V_{DS} \ge -10 \text{ V}$ 11 (AMPS) ID, DRAIN CURRENT 10 8 7 6 3 2 $T_J = -55^{\circ}C$ 0 1.5 3 3.5 4 4.5 -V_{GS}, GATE-TO-SOURCE VOLTAGE (VOLTS)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



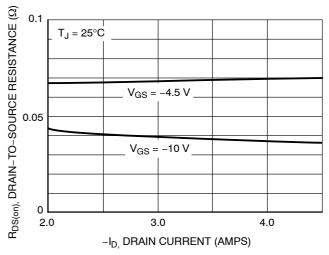
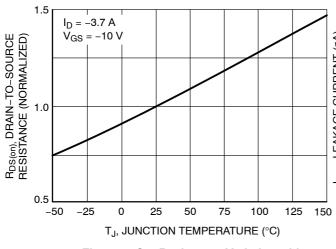


Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



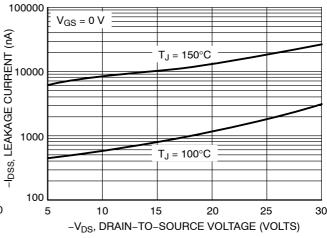
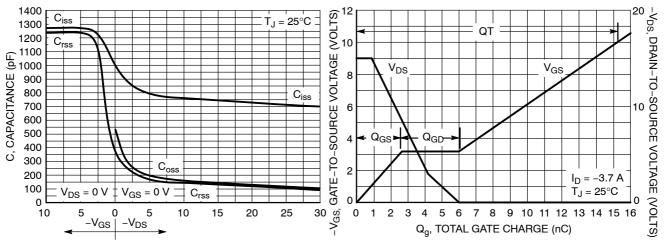


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

查询"NTGS4111P-D"共见的 PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)



-GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source Voltage vs. Total **Gate Charge**

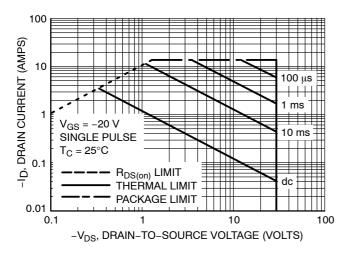


Figure 9. Maximum Rated Forward Biased Safe Operating Area

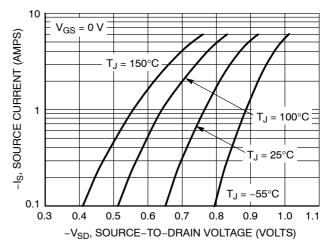


Figure 10. Diode Forward Voltage vs. Current

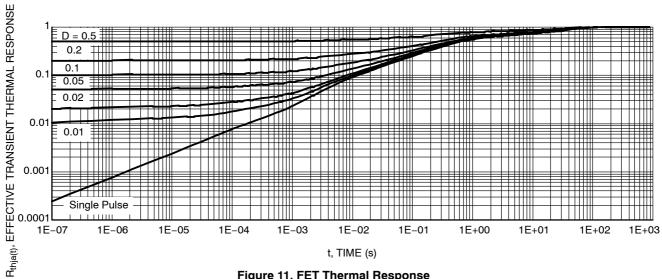
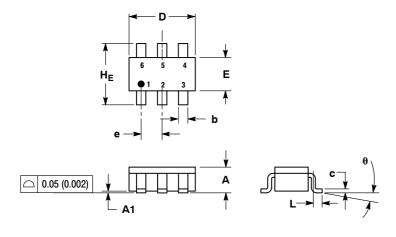


Figure 11. FET Thermal Response

查询"NTGS4111P-D"供应商

PACKAGE DIMENSIONS

TSOP-6 CASE 318G-02 **ISSUE T**



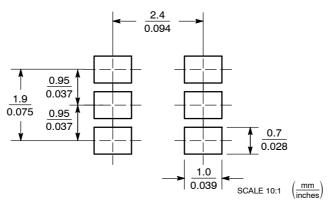
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH
 THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH,
- PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
С	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
е	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	_	10°	0°	_	10°

- STYLE 1: PIN 1. DRAIN
 - 2. DRAIN 3. GATE

 - DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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