Link Replicator for Fibre Channel, Gigabit Ethernet, and HDTV Data Rates

FEATURES

- Replicates Serial Links Such as Fibre Channel, Gigabit Ethernet, and HDTV Links
- T11 Fibre Channel Compliant at 1.0634 Gb/s
- IEEE802.3-2005 Gigabit Ethernet Compliant at 1.25 Gb/s (1000Base-X)
- Support for SMPTE-292M Data Rate at 1.485 Gb/s
- Compatible With VSC7132-01
- No External Components Required
- 0.455 W Maximum Power Dissipation
- 3.3 V Power Supply
- 28-Pin, 4,4 mm × 9,7 mm TSSOP Package
- Footprint Compatible with VSC7132

APPLICATIONS

- Test Equipment
- Gigabit Ethernet and Fibre Channel Switches/Repeaters

DESCRIPTION

The SN65LVCP15 is a high performance serial link mux for use in Fibre Channel (1.0625 Gb/s), Gigabit Ethernet (1.25 Gb/s), and other high speed interface applications. A common application involves a serializer/deserializer (SerDes), such as the TLK2201B, which would normally be connected to the IN± and OUT± ports in order to provide duplicate set of links on the IN0/OUT0 and IN1/OUT1 ports. This type of application is often used to implement high speed test ports that can be monitored without affecting the serial data stream of the application. A popular application is in Line Cards, that use serial links from a SerDes like TLK2201B (SLLS585), where the SN65LVCP15 provides redundant, hot-swappable links to redundant Switch Fabric Cards.

During normal operation, IN is sent to both OUT0 and OUT1 whose buffers are enabled when OE0 and OE1 are HIGH. OUT0 can select between IN and IN1. OUT1 can select between IN and IN0. OUT can select between IN0 and IN1.

In Link Replicator applications, such as the Line Card to Switch Card links, IN is transmitted to both OUT0 and OUT1 which either IN0 or IN1 is selected at OUT. In host Adapter applications, IN goes to OUT0 (an internal connector) which returns data and IN0. IN0 is looped to OUT1 (an external connector) which returns data on IN1 and then back to the SerDes on OUT.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

ORDERABLE PART NUMBER	DESCRIPTION
SN65LVCP15PW(1)	28-Pin TSSOP, 4,4 mm × 9,7 mm Body

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
V_{DD}	Power supply voltage, TTL	0.5 to 4.0	V
$V_{IN(P)}$	DC input voltage, PECL	–0.5 to V_{DD} +0.5	V
$V_{IN(T)}$	DC input voltage, TTL	–0.5 to +5.5	V
$V_{IN(TTL)}$	DC voltage applied to outputs for high output state	–0.5 to V_{DD} +0.5	V
ESD	Electrostatic discharge voltage (human body model)	2	kV
T_{JA}	Junction to Ambient Thermal Resistance (Assumes High K Board)	61.7	°C/W

(1) Stresses listed under absolute maximum ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to theses values for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{DD}	Power supply voltage	3.14	3.47	V
T_C	Case operating temperature	0	85	°C

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f	Operating frequency range		1		1.5	Gb/s
t_1	Flow-through propagation delay	Delay from any input to any output			1	ns
t_r, t_f	Serial data rise and fall time	20% to 80%			300	ps
t_{DJ}	Deterministic jitter added to serial input	1 Gb/s to 1.25 Gb/s. Measured on K28.5+, K28.5– pattern			35	ps pp
		1.25 Gb/s to 1.5 Gb/s. Measured on K28.5+, K28.5– pattern			45	

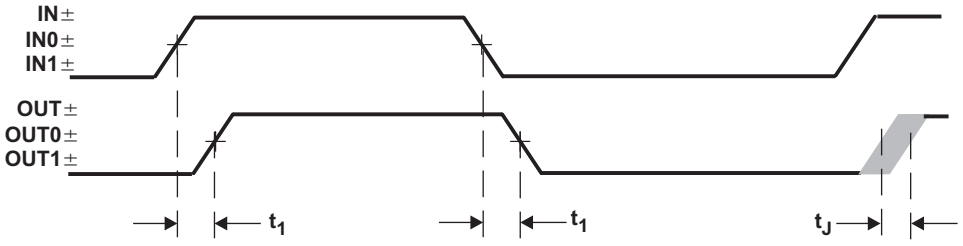


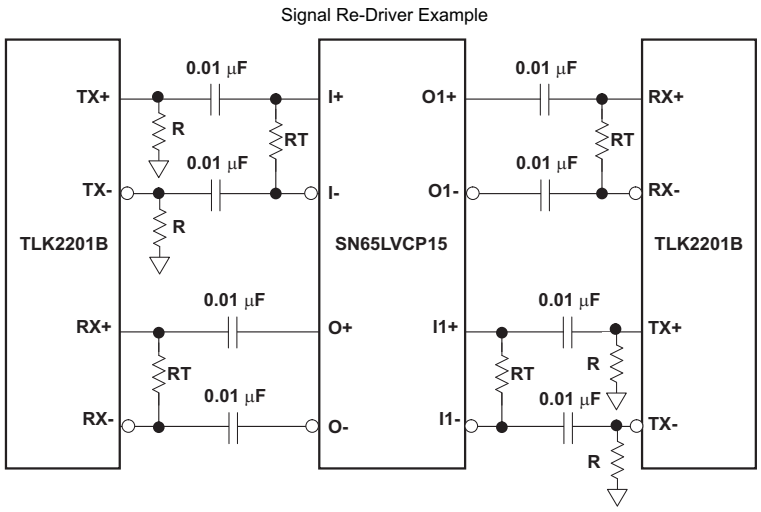
Figure 1. Timing Waveforms

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH(TTL)}$	Input HIGH voltage		2		5.5	V
$V_{IL(TTL)}$	Input LOWS voltage		0		0.8	V
$I_{IH(TTL)}$	Input HIGH current	V_{IN} = 2.4 V	-100		100	µA
$I_{IL(TTL)}$	Input HIGH current	V_{IN} = 0.5 V	–100		100	µA
V_{DD}	Supply voltage	V_{DD} = 3.30 V ±5%	3.14		3.47	V
I_{DD}	Supply current	Outputs open, V_{DD} = V_{DD} max			131	mA
P_D	Power dissipation	Outputs open, V_{DD} = V_{DD} max			455	mW
ΔV_{IN}	Receiver differential peak-to-peak input sensitivity (IN, IN0, IN1)	AC coupled, Internally biased at V_{DD}/2	300		2600	mV_{PP}
ΔV_{OUT50}	Output differential peak-to-peak voltage swing (OUT, OUT0, OUT1)	50 Ω to V_{DD} – 2 V	1000		2200	mV_{PP}
ΔV_{OUT75}		75 Ω to V_{DD} – 2 V	1200		2200	mV_{PP}

APPLICATION EXAMPLE



R is 150 Ω for both 100 Ω differential or 150 Ω differential traces.

RT matches the differential impedance of the link.

For optimal signal integrity performance, A/C coupling is recommended.

Figure 2. TLK2201B and SN65LVCP15 Interconnect

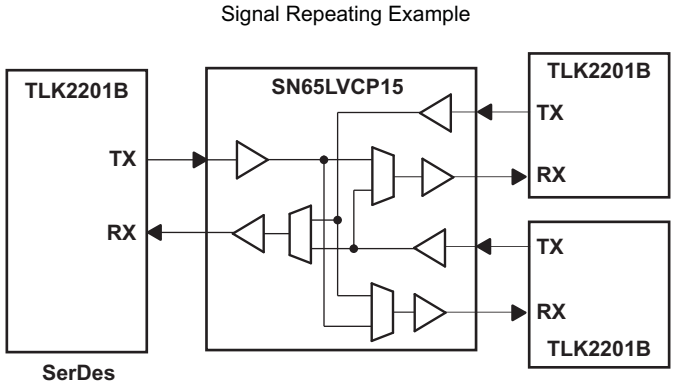
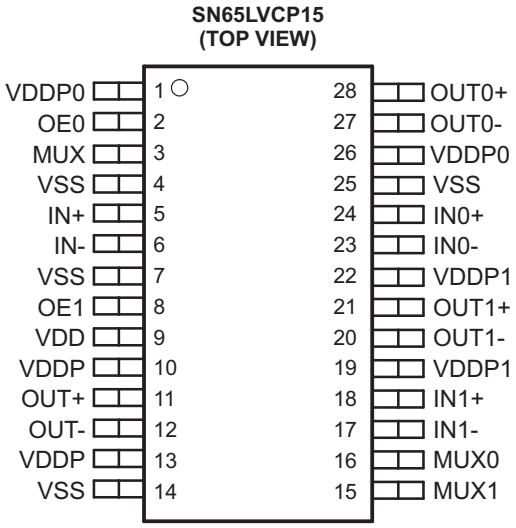


Figure 3.

PACKAGE INFORMATION – PIN DIAGRAM



PIN FUNCTIONS

PIN		TYPE	LEVEL	DESCRIPTION
NO.	NAME			
5, 6 24, 23 18, 17	IN+, IN– IN0+, IN0– IN1+, IN1–	I	PECL	Differential (biased to V_{DD}/2) High-speed serial inputs
11, 12 28, 27 21, 20	OUT+, OUT– OUT0+, OUT0– OUT1+, OUT1–	O	PECL	Differential high-speed serial outputs
2 8	OE0 OE1	I	TTL	OE0/OE1 enables OUT0/OUT1 when HIGH. When LOW, OUTx is powered down and both OUTx+ and OUTx– float HIGH.
3	MUX	I	TTL	Determines source of OUT. Selects either IN0 (LOW) or IN1 (HIGH).
15	MUX1	I	TTL	Determines source of OUT1. Selects either IN (HIGH) or IN0 (LOW).
16	MUX0	I	TTL	Determines source of OUT0. Selects either IN (LOW) or IN1 (HIGH).
9	VDD	Pwr		3.3 V power supply for digital logic
10, 13 1, 26 19, 22	VDDP VDDP0 VDDP1	Pwr		High-speed output power supply: 3.3 V supply for PECL drivers. VDDP0 is for OUT0, VDDP is for OUT, and VDDP1 is for OUT1.
4, 7 14, 25	VSS	Pwr		Ground

MOISTURE SENSITIVITY LEVEL

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standards.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVCP15PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP15PWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

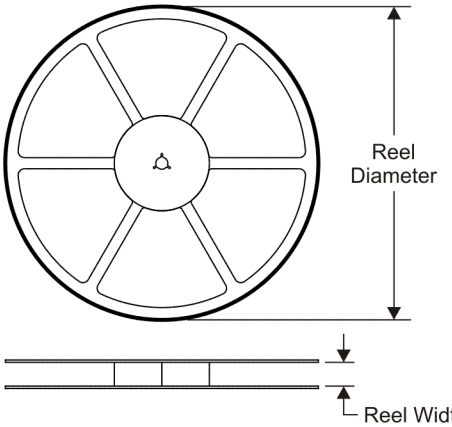
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

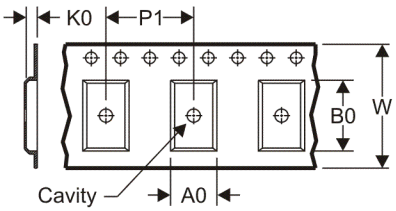
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

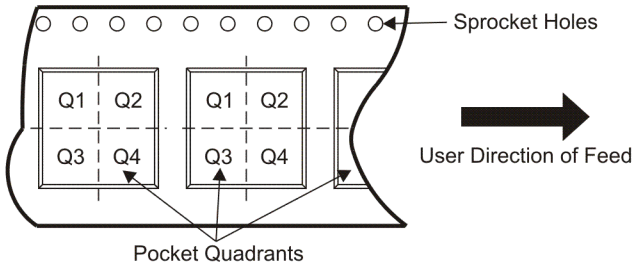


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

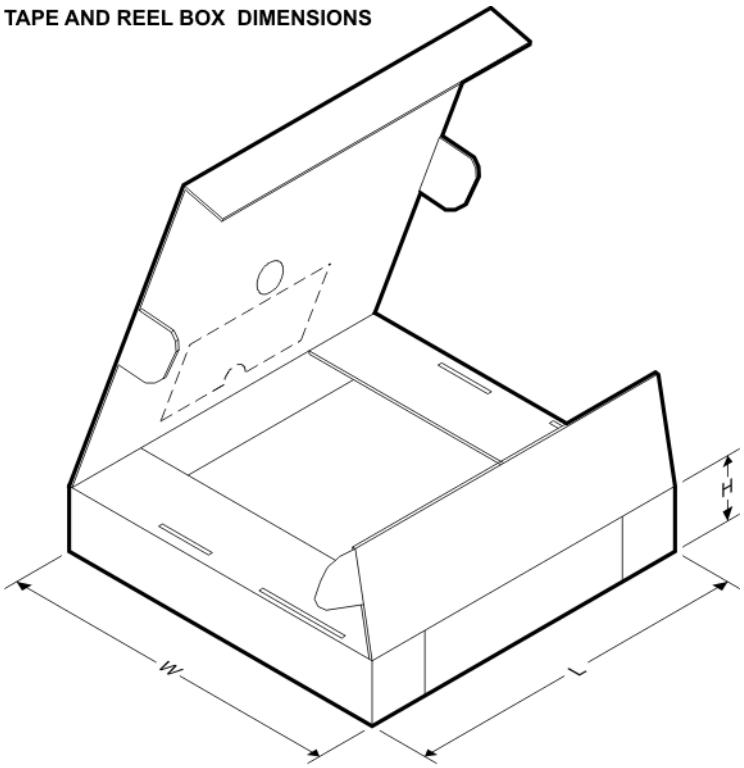
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVCP15PWR	TSSOP	PW	28	2000	330.0	16.4	7.1	10.4	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

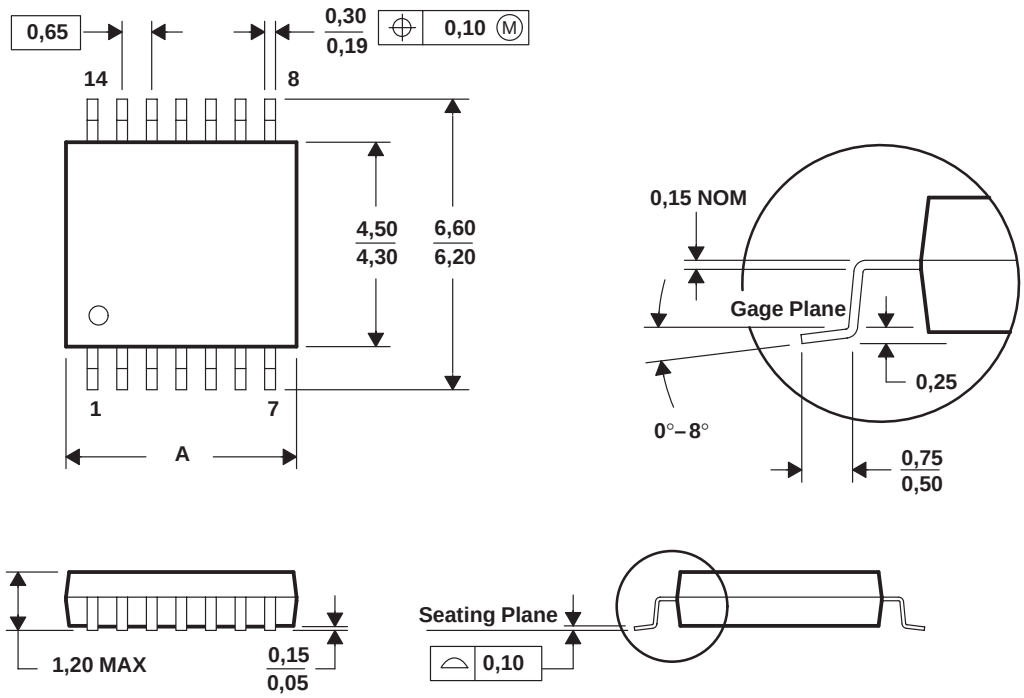


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVCP15PWR	TSSOP	PW	28	2000	346.0	346.0	33.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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