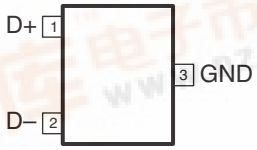
2-CHANNEL ESD SOLUTION FOR HIGH-SPEED (6 GBPS) DIFFERENTIAL INTERFACE

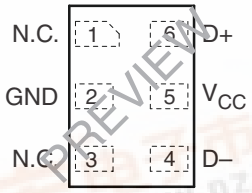
FEATURES

- **0.05-pF Matching Capacitance Between the Differential Signal Pair**
- **Single-Pair Differential Lines to Protect the Differential Data and Clock Lines of the LVDS, SATA, Ethernet, or USB High-Speed (HS) Interface**
- **Flow-Through Pin Mapping for the High-Speed Lines Ensures Zero Additional Skew Due to Board Layout While Placing ESD-Protection Chip Near the Connector**
- **Supports Data Rates in Excess of 6 Gbps**
- **ESD Protection Meets or Exceeds IEC61000-4-2 (Level 4)**
- **5-A Peak Pulse Current (8/20 μs Pulse) for V_{BUS} and D+, D–, and ID Lines**
- **Industrial Temperature Range: –40°C to 85°C**
- **Multiple Space-Saving Package Options**

DBZ/DRT PACKAGE
(TOP VIEW)



DRY PACKAGE
(TOP VIEW)



N.C. – No internal connection

APPLICATIONS

- **Notebooks**
- **Set-Top Boxes**
- **DVD Players**
- **Media Players**
- **Portable Computers**

DESCRIPTION/ORDERING INFORMATION

The TPD2E009 provides 2 ESD clamp circuits with flow-through pin mapping for ease of board layout. This device has been designed to protect sensitive components which are connected to ultra high-speed data and transmission lines. The TPD2E009 offers protection from stress caused by ESD (electrostatic discharge). This device also offers 5 A (8/20 μs) peak pulse current ratings per IEC 61000-4-5 (lightning) specification.

The monolithic silicon technology allows matching between the differential signal pairs. The less than differential 0.05-pF capacitance ensures that the differential signal distortion due to added ESD clamp remains minimal. The 0.7-pF line capacitance is suitable for high-speed data rate (in excess of 6 Gbps).

The TPD2E009 conforms to IEC61000-4-2 (Level 4) ESD protection. The DRT (1 mm × 1 mm) package is offered for space-saving portable applications. The industry standard DBZ (2.4 mm × 2.9 mm) package offers additional flexibility in the board layout for the system designer.

The TPD2E009 is characterized for operation over ambient air temperature range of –40°C to 85°C.

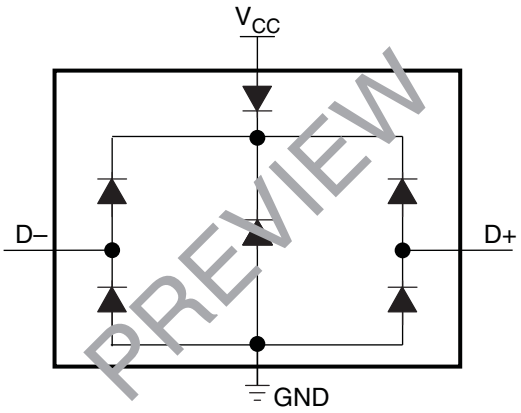
ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SON – DRY	Tape and reel	TPD2E009DRYR	PREVIEW
	SOP – DBZ	Tape and reel	TPD2E009DBZR	NFLR
	SOT– DRT	Tape and reel	TPD2E009DRTR	4T

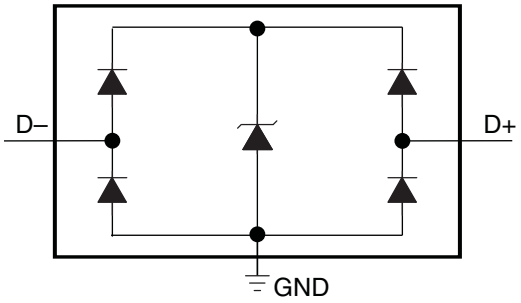
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

CIRCUIT DIAGRAMS

DRY Circuit



DBZ/DRT Circuit



TERMINAL FUNCTIONS

TERMINAL			TYPE	DESCRIPTION
NAME	DBZ/DRT PIN NO.	DRY(1) PIN NO.		
D+, D-	1, 2	4, 6	ESD port	High-speed ESD clamp, provides ESD protection to the high-speed differential data lines
V_{CC}	–	5	Supply	Power supply
GND	3	3	GND	Ground

(1) Product Preview

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
	IO voltage tolerance		D+, D– pins	0	6	
T_A	Operating free-air temperature range			–40	85	°C
T_{stg}	Storage temperature range			–65	125	°C
	ESD protection	IEC 61000-4-2 Contact Discharge	D+, D– pins		±8	kV
		IEC 61000-4-2 Air-Gap Discharge	D+, D– pins		±8	kV
	Peak pulse current (t_p = 8/20 µs)		D+, D– pins		5	A
	Peak pulse power (t_p = 8/20 µs)		D+, D– pins		45	W

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	D+,D– pins to ground				5.5	V
V_{clamp}	Clamp voltage	D+,D– pins to ground,	I_{IO} = 1 A			8	V
I_{IO}	Current from IO port to supply pins	V_{IO} = 2.5 V, I_D = 8 mA			0.01	0.1	µA
V_D	Diode forward voltage	D+,D– pins, lower clamp diode,	V_{IO} = 2.5 V, I_D = 8 mA	0.6	0.8	0.95	V
		D+,D– pins, upper clamp diode, DRY package	V_{CC} = 0 V, I_D = –8 mA	0.6	0.8	0.95	
R_{dyn}	Dynamic resistance	D+,D– pins,	I = 1 A		1		Ω
C_{IO}	IO capacitance	D+,D– pins, DBZ Package	V_{IO} = 2.5 V		0.9		pF
		D+,D– pins, DRT Package	V_{IO} = 2.5 V		0.7		pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA		7			V

TYPICAL OPERATING CHARACTERISTICS

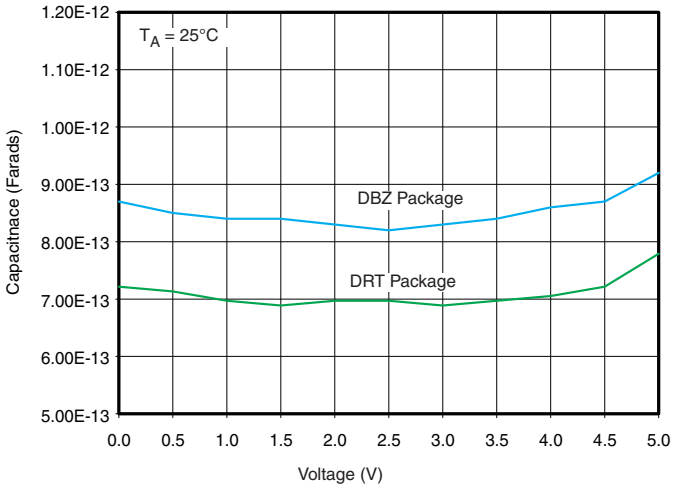


Figure 1. IO Capacitance vs IO Voltage

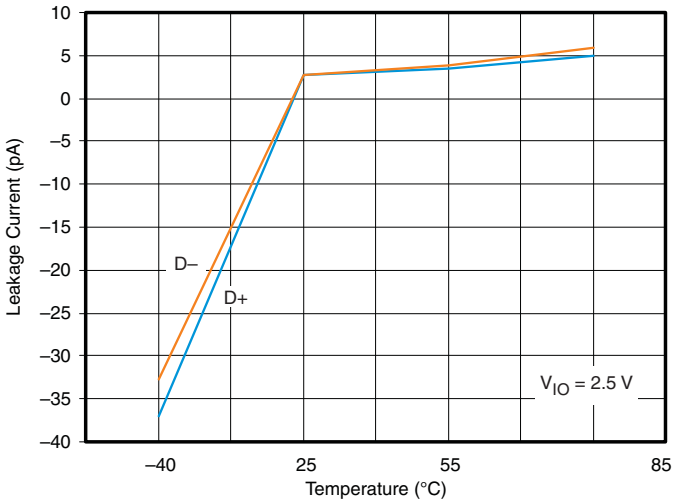


Figure 2. Leakage Current vs Temperature

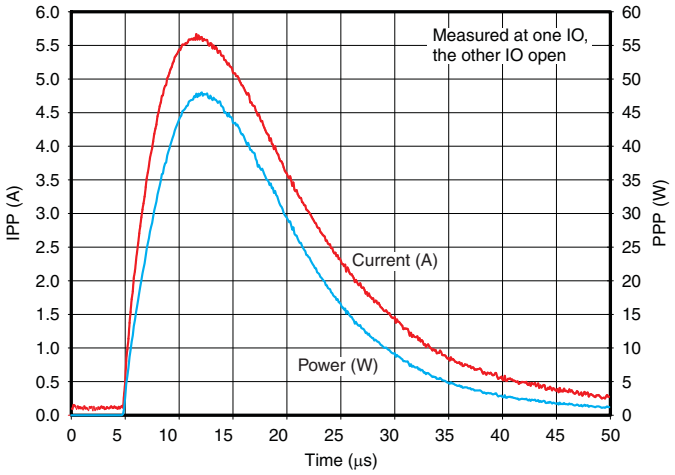


Figure 3. Peak Pulse Waveforms

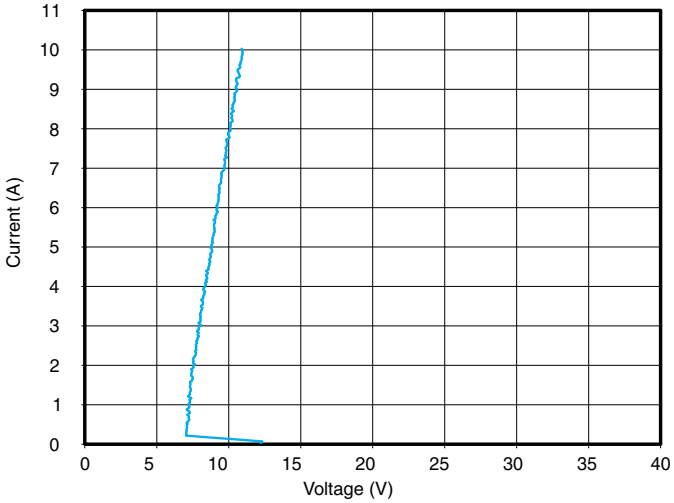


Figure 4. D+,D– Transmission Line Pulser Plot (100 ns Pulse, 10 ns Rise Time)

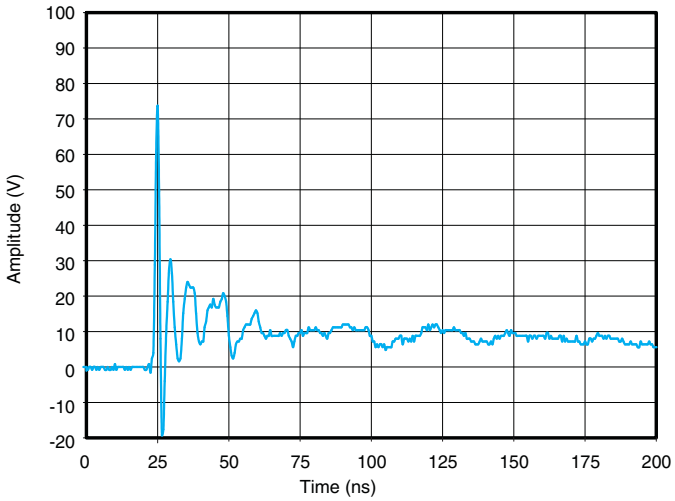


Figure 5. IEC Clamping Waveforms (8 kV Contact)

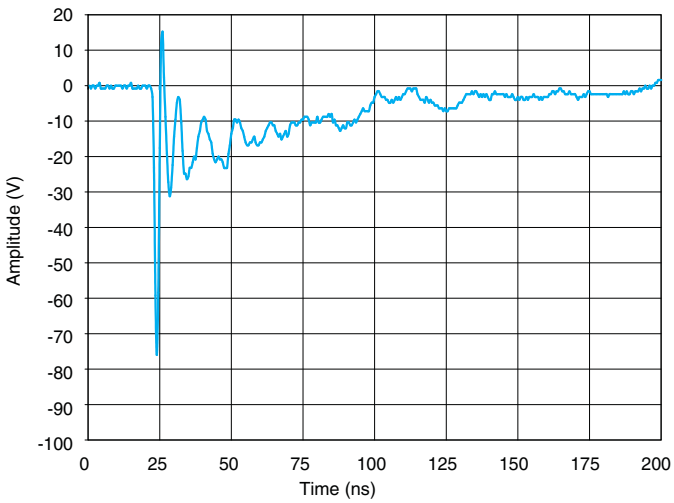


Figure 6. IEC Clamping Waveforms (–8 kV Contact)

TYPICAL OPERATING CHARACTERISTICS (continued)

Eye Diagrams

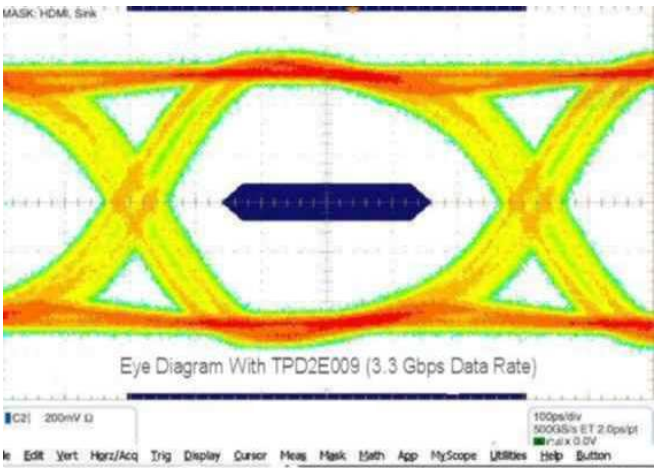


Figure 7. Eye Diagram With TPD2E009 (3.3 Gbps Data Rate) (3-Pin DBZ Package)

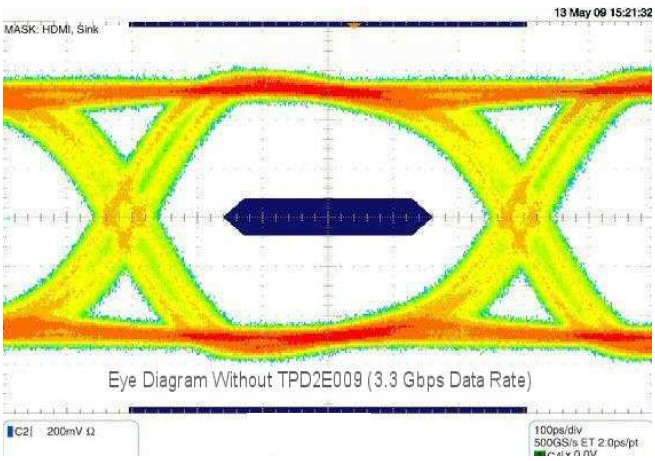


Figure 8. Eye Diagram Without TPD2E009 (3.3 Gbps Data Rate) (3-Pin DBZ Package)

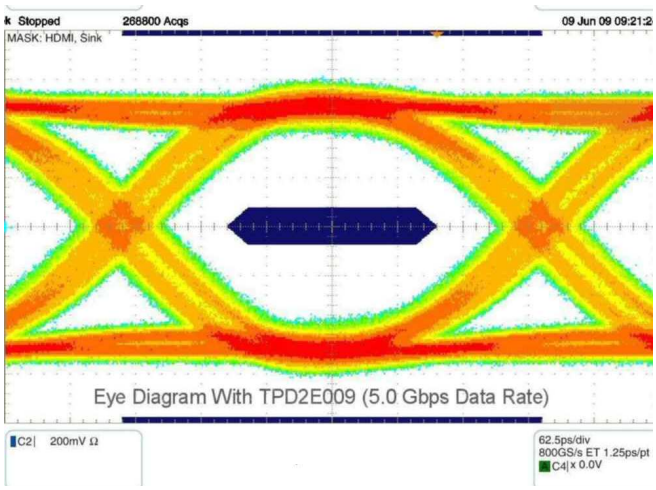


Figure 9. Eye Diagram With TPD2E009 (5.0 Gbps Data Rate) (3-Pin DBZ Package)

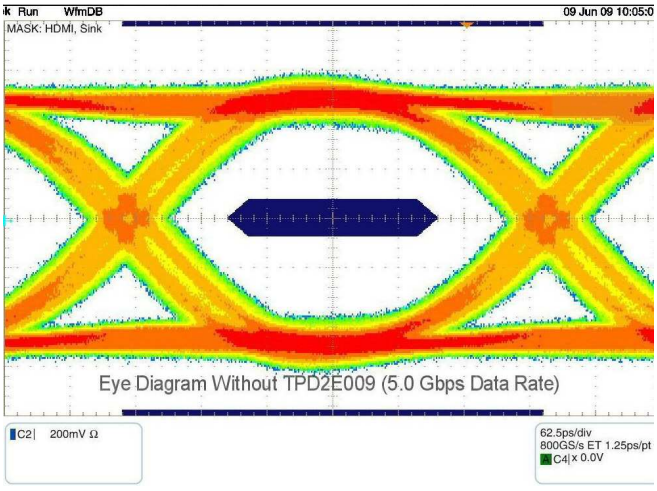


Figure 10. Eye Diagram Without TPD2E009 (5.0 Gbps Data Rate) (3-Pin DBZ Package)

TYPICAL OPERATING CHARACTERISTICS (continued)

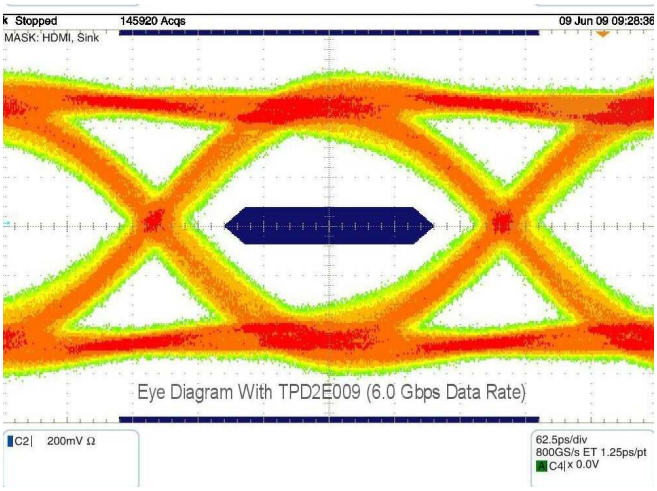


Figure 11. Eye Diagram With TPD2E009 (6.0 Gbps Data Rate) (3-Pin DBZ Package)

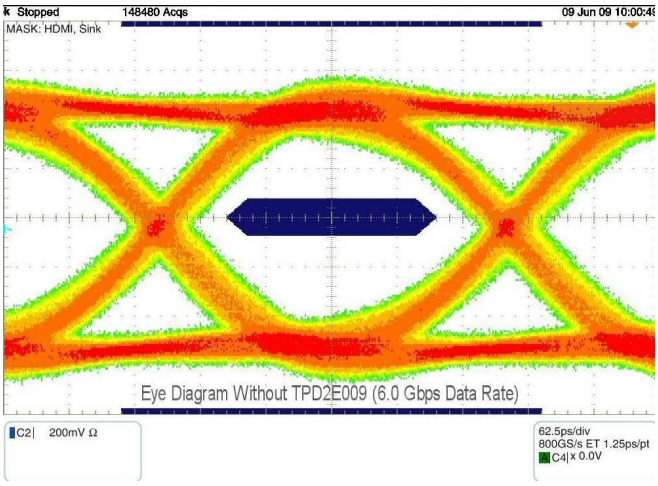


Figure 12. Eye Diagram Without TPD2E009 (6.0 Gbps Data Rate) (3-Pin DBZ Package)

APPLICATION INFORMATION

Typical Application

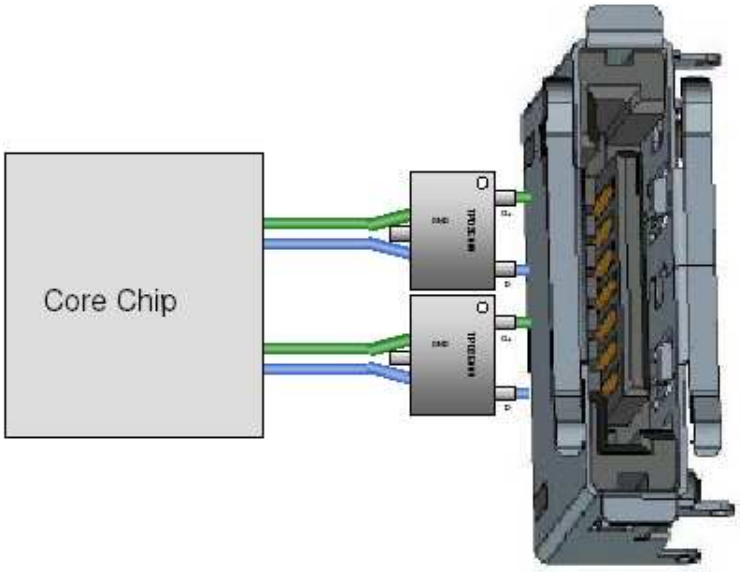


Figure 13. TPD2E009 in Differential eSATA Interface

Figure 13 shows the board layout scheme for the D+/D– lines of a single differential pair. It allows the differential signal pairs couple together right after they touch the ESD ports (pin 1 and pin 2) of the TPD2E009.

Designing with High-Speed Differential Signals

Layout considerations, such as package selection, trace routing, etc. must be taken into account while designing the ESD clamp circuit for high-speed interface. Difficult routing can lead the designer to use vias or stubs in the board traces, creating significant disruption in the line impedance in the high-speed signal path. Poor package choice can force designer to route differential traces with unequal lengths and add the skew in the signals. It is recommended to closely couple the differential traces to reduce the EMI interference.

The TPD2E009 can provide system level ESD protection to the high-speed differential ports (>6 Gbps data rate). The flow-through package offers flexibility for board routing with traces up to 15 mills wide. Figure 14 and Figure 15 show the board layout scheme for the D+/D– lines of a single differential pair. It allows the differential signal pairs couple together right after they touch the ESD ports (pin 1 and pin 2) of the TPD2E009.

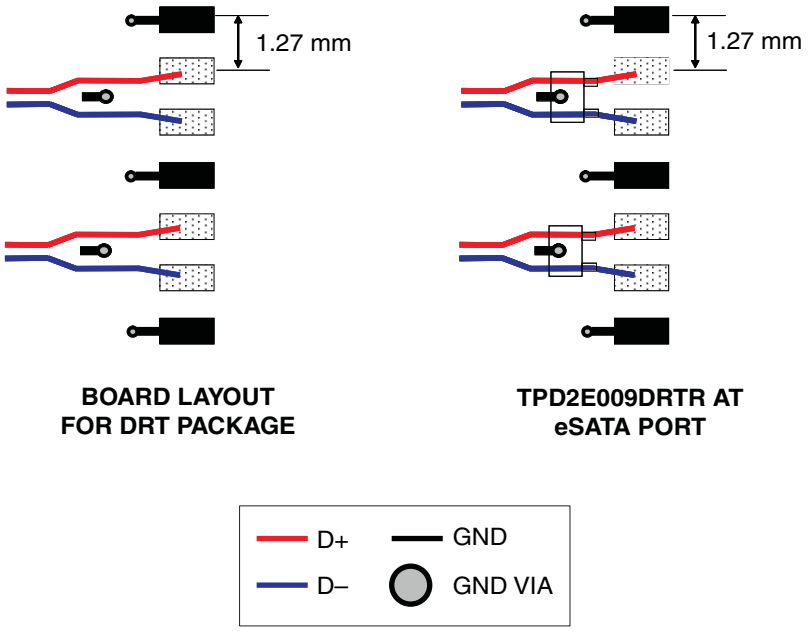


Figure 14. TPD2E009DRTR at eSATA Connector Interface

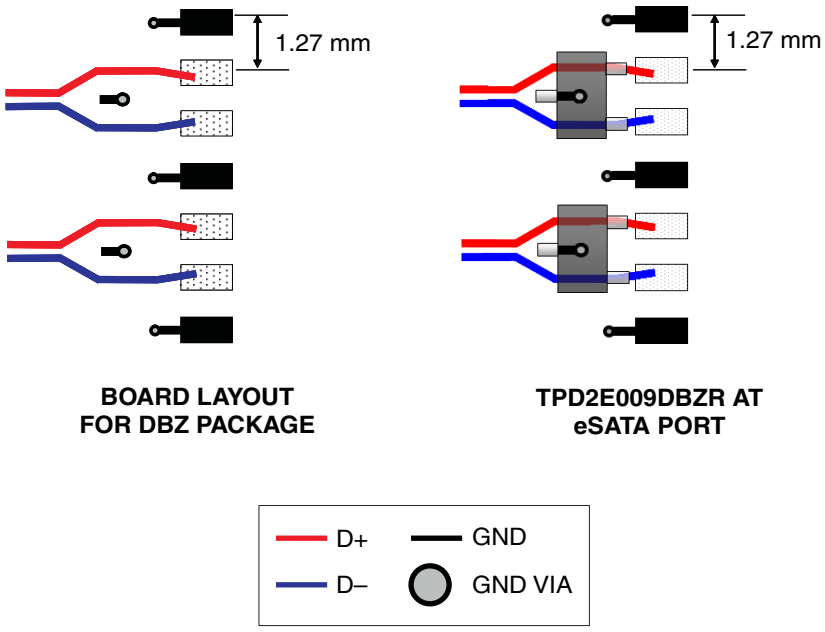
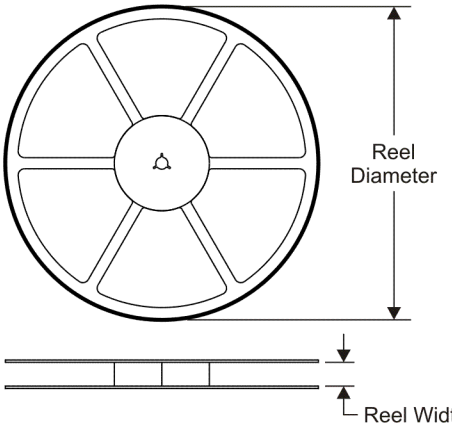


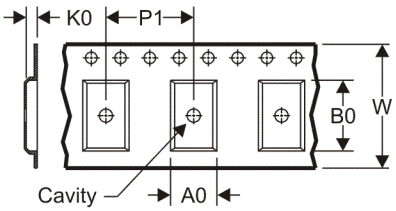
Figure 15. TPD2E009DBZR at eSATA Connector Interface

TAPE AND REEL INFORMATION

REEL DIMENSIONS

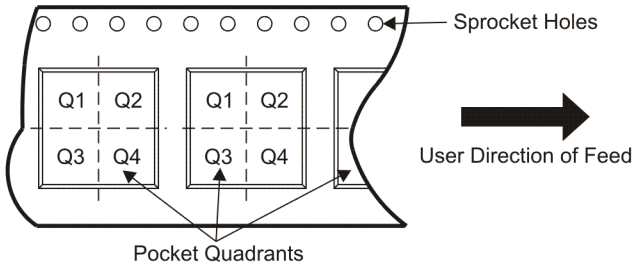


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

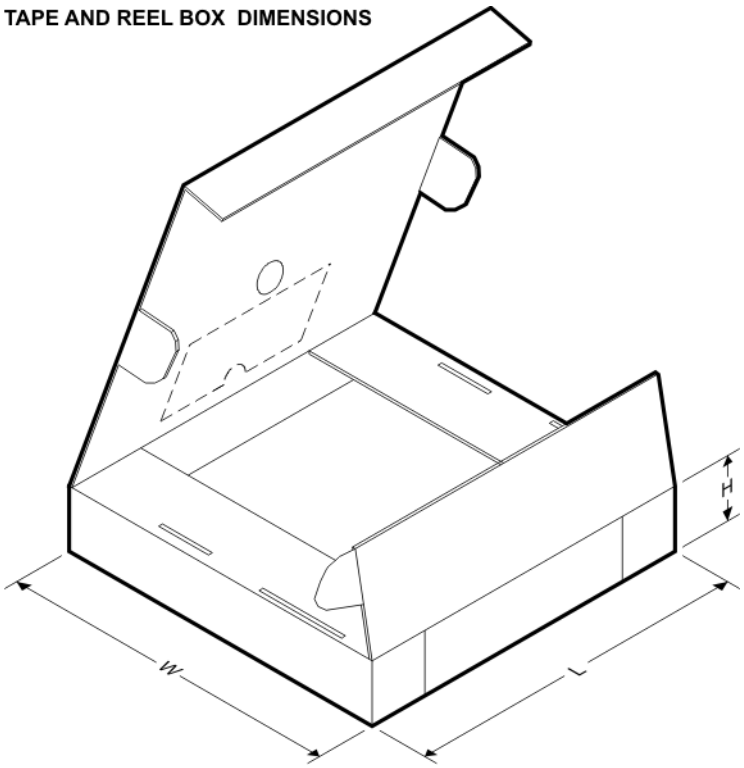
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E009DBZR	SOT-23	DBZ	3	3000	180.0	9.2	3.18	3.28	1.32	4.0	8.0	Q3
TPD2E009DRTR	SOT	DRT	3	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q3

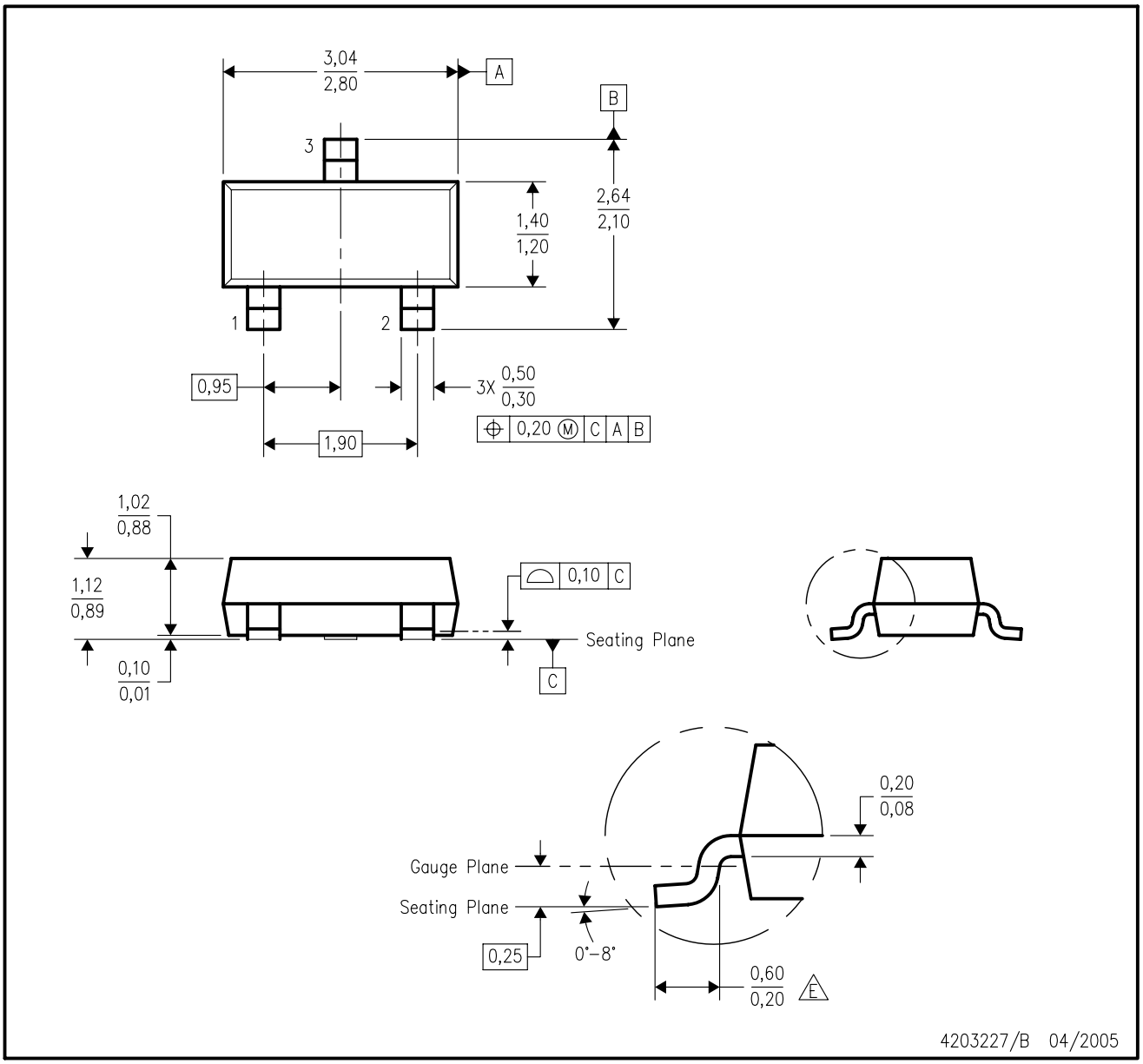
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

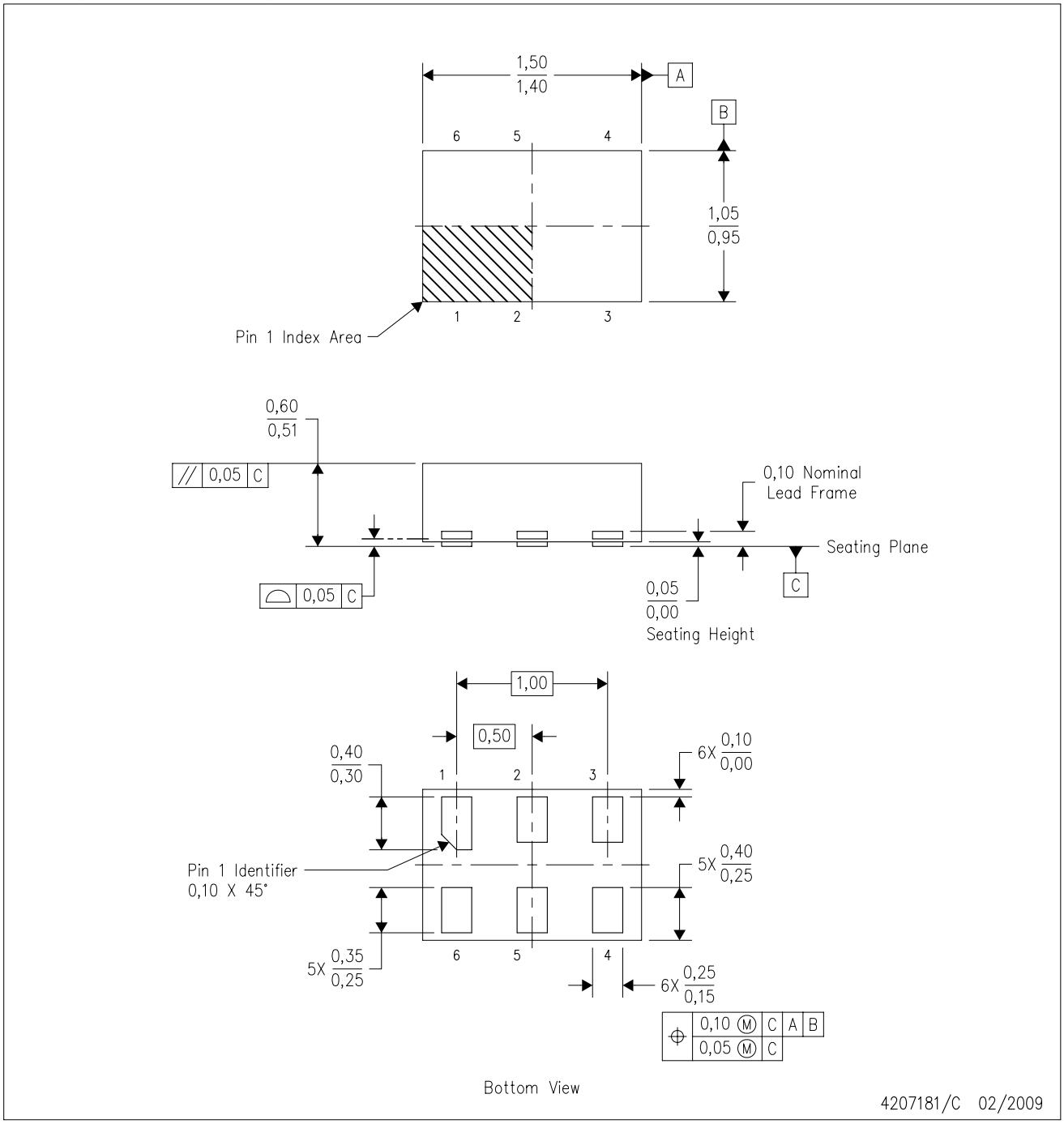
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E009DBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0
TPD2E009DRTR	SOT	DRT	3	3000	202.0	201.0	85.0

DBZ (R–PDSO–G3) PLASTIC SMALL–OUTLINE



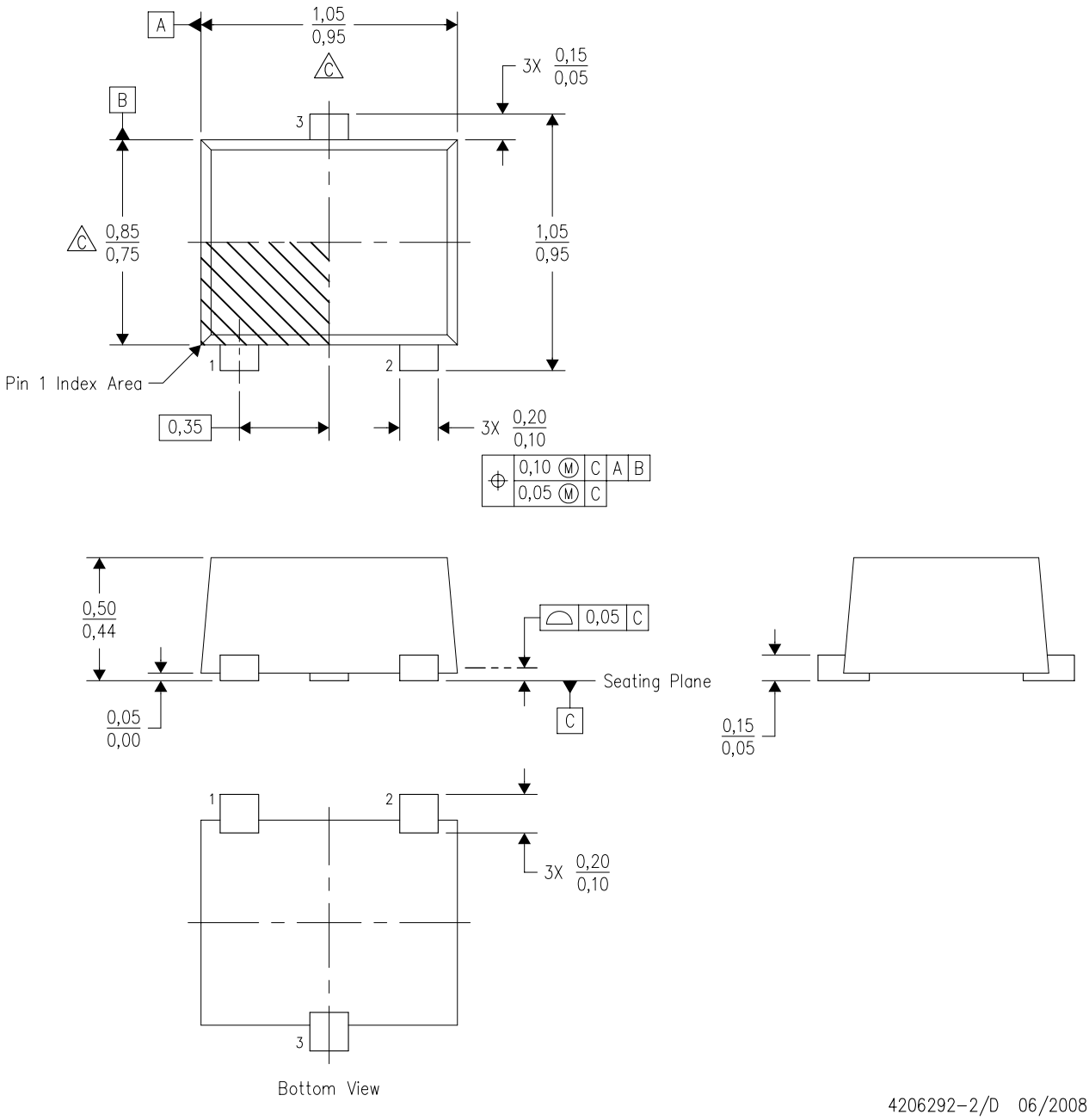
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Lead dimensions are inclusive of plating.
D. Body dimensions are exclusive of mold flash and protrusion. Mold flash and protrusion not to exceed 0.25 per side.
E. Falls within JEDEC TO–236 variation AB, except minimum foot length.

DRY (R–PDSO–N6) PLASTIC SMALL OUTLINE



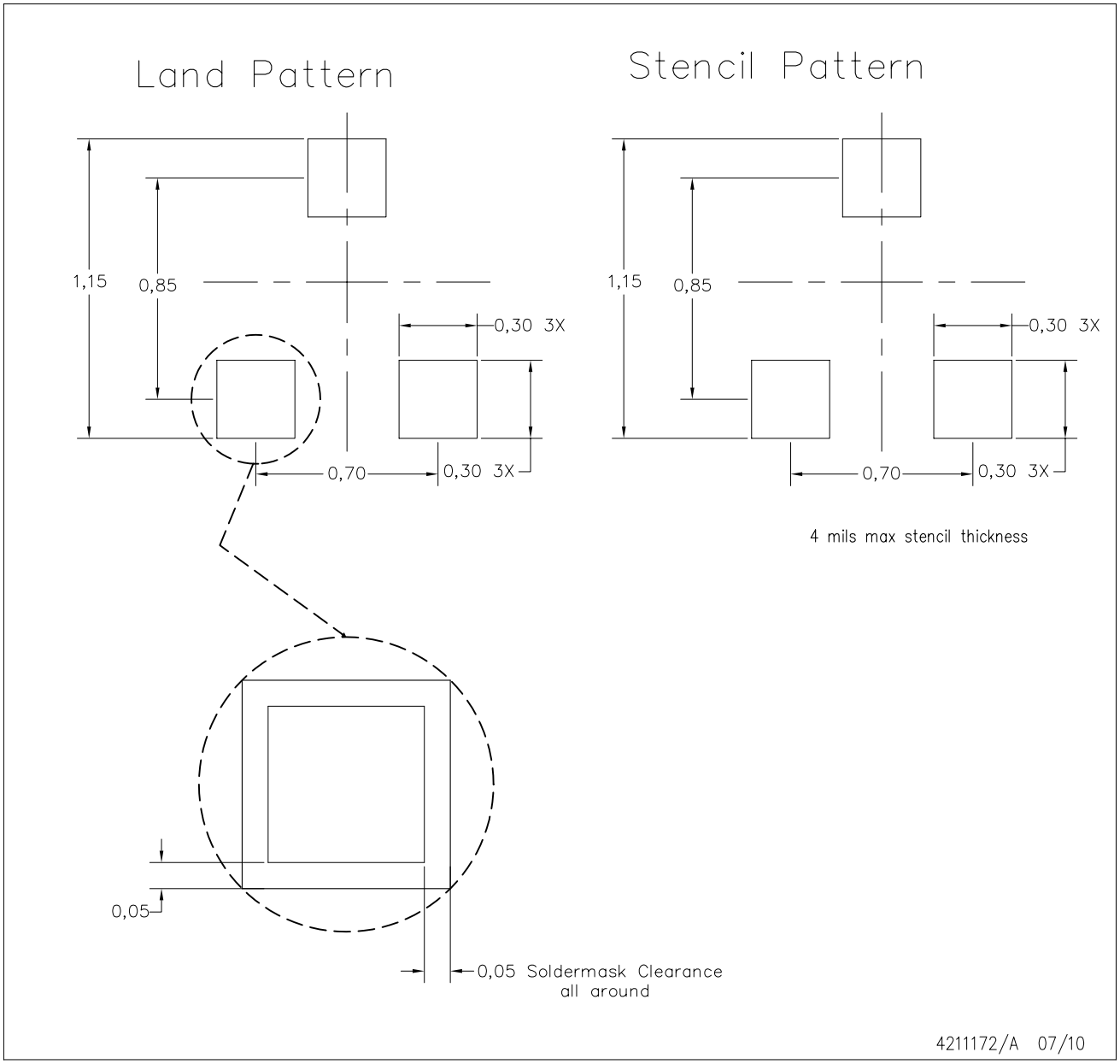
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. This package complies to JEDEC MO–287 variation UFAD.

DRT (R–PDSO–N3) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,10 per end or side.
D. JEDEC package registration is pending.

DRT (S–PDSO–N3) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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