National Semiconductor

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# 54AC377 • 54ACT377 Octal D Flip-Flop with Clock Enable

### **General Description**

The 'AC/'ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable  $(\overline{CE})$  is LOW.

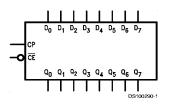
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding filp-flop's Q output. The  $\overline{\text{CE}}$  input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

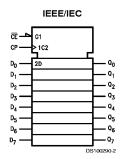
### **Features**

■ I<sub>CC</sub> reduced by 50%

- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See '273 for master reset version
- See '373 for transparent latch version
- See '374 for TRI-STATE® version
- 'ACT377 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  - 'AC377: 5962-88702
  - 'ACT377: 5962-87697

### **Logic Symbols**





Pin	Description				
Names					
D <sub>0</sub> –D <sub>7</sub>	Data Inputs				
CE	Clock Enable (Active LOW)				
Q <sub>0</sub> –Q <sub>7</sub>	Data Outputs				
СР	Clock Pulse Input				

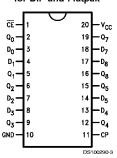
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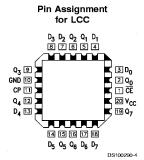
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DS100290

### **Connection Diagrams**

#### Pin Assignment for DIP and Flatpak





### **Mode Select-Function Table**

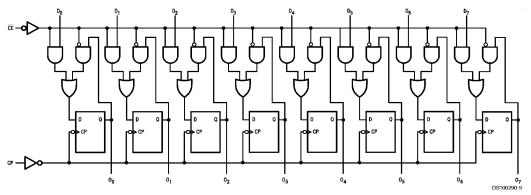
Operating Mode		Inputs	Outputs	
	CP	CE	D <sub>n</sub>	Q <sub>n</sub>
Load '1'	~	L	Н	Н
Load '0'	_	L	L	L
Hold (Do Nothing)		Н	Х	No Change
	Х	Н	X	No Change

- H = HIGH Voltage Level
  L = LOW Voltage Level

- X = Immaterial

  ✓ = LOW-to-HIGH Clock Transition

### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V <sub>CC</sub> )	-0.5V to +7.0V
DC Input Diode Current (IIK)	
$V_1 = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V <sub>I</sub> )	$-0.5V$ to $V_{CC}$ + $0.5V$
DC Output Diode Current (IOK)	
$V_{O} = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (Vo)	$-0.5V$ to $V_{CC}$ + $0.5V$
DC Output Source	

or Sink Current (I<sub>O</sub>) ±50 mA

 $\begin{array}{lll} \text{DC V}_{\text{CC}} \text{ or Ground Current} \\ \text{per Output Pin (I}_{\text{CC}} \text{ or I}_{\text{GND}}) & \pm 50 \text{ mA} \\ \text{Storage Temperature (T}_{\text{STG}}) & -65^{\circ}\text{C to } +150^{\circ}\text{C} \end{array}$ 

Junction Temperature (T<sub>J</sub>)
CDIP 175°C

# Recommended Operating Conditions

Supply Voltage  $(V_{CC})$ 

 $\begin{tabular}{lll} 'AC & 2.0V to 6.0V \\ 'ACT & 4.5V to 5.5V \\ Input Voltage (V_i) & 0V to V_{CC} \\ Output Voltage (V_O) & 0V to V_{CC} \\ \end{tabular}$ 

Operating Temperature (T<sub>A</sub>)

Minimum Input Edge Rate (ΔV/Δt)

'AC Devices

 $V_{\text{IN}}$  from 30% to 70% of  $V_{\text{CC}}$ 

V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices

 $V_{\text{IN}}$  from 0.8V to 2.0V

 $V_{CC}$  @ 4.5V, 5.5V 125 mV/ns Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

Note 2: See individual datasheets for those devices which differ from the

**Note 2:** See individual datasheets for those devices which differ typical input rise and fall times noted here.

### DC Characteristics for 'AC Family Devices

			54AC		
Symbol	Parameter	v <sub>cc</sub>	T <sub>A</sub> =	Units	Conditions
		(V)	-55°C to +125°C		
			Guaranteed Limits	1	
V <sub>IH</sub>	Minimum High Level	3.0	2.1		V <sub>OUT</sub> = 0.1V
	Input Voltage	4.5	3.15	V	or V <sub>CC</sub> – 0.1V
		5.5	3.85		
V <sub>IL</sub>	Maximum Low Level	3.0	0.9		$V_{OUT} = 0.1V$
	Input Voltage	4.5	1.35	V	or V <sub>CC</sub> – 0.1V
		5.5	1.65		
V <sub>OH</sub>	Minimum High Level	3.0	2.9		I <sub>OUT</sub> = -50 μA
	Output Voltage	4.5	4.4	V	
		5.5	5.4		
					(Note 3)
					$V_{IN} = V_{IL}$ or $V_{IH}$
		3.0	2.4		I <sub>OH</sub> = -12 mA
		4.5	3.7	V	$I_{OH} = -24 \text{ mA}$
		5.5	4.7		I <sub>OH</sub> = -24 mA
V <sub>OL</sub>	Maximum Low Level	3.0	0.1		I <sub>OUT</sub> = 50 μA
	Output Voltage	4.5	0.1	V	
		5.5	0.1		
					(Note 3)
					$V_{IN} = V_{IL}$ or $V_{IH}$
		3.0	0.50		$I_{OL}$ = 12 mA
		4.5	0.50	V	$I_{OL} = 24 \text{ mA}$
		5.5	0.50		$I_{OL} = 24 \text{ mA}$
I <sub>IN</sub>	Maximum Input	5.5	±1.0	μА	$V_I = V_{CC}$ , GND
	Leakage Current				

### DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V <sub>cc</sub> (V)	54AC T <sub>A</sub> = -55°C to +125°C	Units	Conditions
			Guaranteed Limits		
I <sub>OLD</sub>	(Note 4)	5.5	50	mA	V <sub>OLD</sub> = 1.65V Max
	Minimum Dynamic				
I <sub>OHD</sub>	Output Current	5.5	-50	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>cc</sub>	Maximum Quiescent	5.5	80.0	μΑ	V <sub>IN</sub> = V <sub>CC</sub>
	Supply Current				or GND

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

### DC Characteristics for 'ACT Family Devices

			54ACT		
Symbol	Parameter	v <sub>cc</sub>	T <sub>A</sub> =	Units	Conditions
		(v)	-55°C to +125°C		
			Guaranteed Limits		
V <sub>IH</sub>	Minimum High Level	4.5	2.0	V	V <sub>OUT</sub> = 0.1V
	Input Voltage	5.5	2.0		or V <sub>CC</sub> – 0.1V
V <sub>IL</sub>	Maximum Low Level	4.5	0.8	V	V <sub>OUT</sub> = 0.1V
	Input Voltage	5.5	0.8		or V <sub>CC</sub> – 0.1V
V <sub>OH</sub>	Minimum High Level	4.5	4.4	V	I <sub>OUT</sub> = -50 μA
	Output Voltage	5.5	5.4		
					(Note 6)
					$V_{IN} = V_{IL} \text{ or } V_{IH}$
		4.5	3.70	V	$I_{OH} = -24 \text{ mA}$
		5.5	4.70		$I_{OH} = -24 \text{ mA}$
V <sub>OL</sub>	Maximum Low Level	4.5	0.1	V	I <sub>OUT</sub> = 50 μA
	Output Voltage	5.5	0.1		
					(Note 6)
					$V_{IN} = V_{IL} \text{ or } V_{IH}$
		4.5	0.50	V	$I_{OL} = 24 \text{ mA}$
		5.5	0.50		$I_{OL} = 24 \text{ mA}$
I <sub>IN</sub>	Maximum Input	5.5	±1.0	μА	$V_I = V_{CC}$ , GND
	Leakage Current				
I <sub>CCT</sub>	Maximum	5.5	1.6	mA	$V_{I} = V_{CC} - 2.1V$
	I <sub>co</sub> /Input				
I <sub>OLD</sub>	(Note 7)	5.5	50	mA	V <sub>OLD</sub> = 1.65V Max
	Minimum Dynamic				
I <sub>OHD</sub>	Output Current	5.5	-50	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>cc</sub>	Maximum Quiescent	5.5	80.0	μА	$V_{IN} = V_{CC}$
	Supply Current				or GND

Note 6: \*All outputs loaded; thresholds on input associated with output under test.

Note 7: †Maximum test duration 2.0 ms, one output loaded at a time.

Note 8: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics							
Symbol	Parameter	V <sub>cc</sub> (V) (Note 9)	54AC  T <sub>A</sub> = -55°C  to +125°C  C <sub>1</sub> = 50 pF		Units	Fig. No.	
		(14010-0)	Min	Max	1		
f <sub>max</sub>	Maximum Clock	3.3	75		MHz		
	Frequency	5.0	95				
t <sub>PLH</sub>	Propagation Delay	3.3	1.0	14.0	ns		
	CP to Q <sub>n</sub>	5.0	1.5	10.0			
t <sub>PHL</sub>	Propagation Delay	3.3	1.0	15.0	ns		
	CP to Q <sub>n</sub>	5.0	1.5	11.0			

Note 9: Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

# **AC Operating Requirements**

Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	54AC  T <sub>A</sub> = -55°C  to +125°C  C <sub>L</sub> = 50 pF  Guaranteed  Minimum	Units	Fig. No.
t <sub>s</sub>	Setup Time, HIGH or LOW	3.3	7.5	ns	
	D <sub>n</sub> to CP	5.0	6.0		
t <sub>h</sub>	Hold Time, HIGH or LOW	3.3	1.5	ns	
	D <sub>n</sub> to CP	5.0	2.5		
t <sub>s</sub>	Setup Time, HIGH or LOW	3.3	9.5	ns	
	CE to CP	5.0	6.0		
t <sub>h</sub>	Hold Time, HIGH or LOW	3.3	1.0	ns	
	CE to CP	5.0	2.0		
t <sub>w</sub>	CP Pulse Width	3.3	6.5	ns	
	HIGH or LOW	5.0	5.0		

Note 10: Voltage Range 3.3 is 3.0V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

### **AC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V) (Note 11)	54ACT  T <sub>A</sub> = -55°C  to +125°C  C <sub>L</sub> = 50 pF		Units	Fig. No.
			Min	Max		
f <sub>max</sub>	Maximum Clock	5.0	85		MHz	
	Frequency					
t <sub>PLH</sub>	Propagation Delay	5.0	1.5	11.0	ns	
	CP to Q <sub>n</sub>					
t <sub>PHL</sub>	Propagation Delay	5.0	1.5	12.0	ns	
	CP to Q <sub>n</sub>					

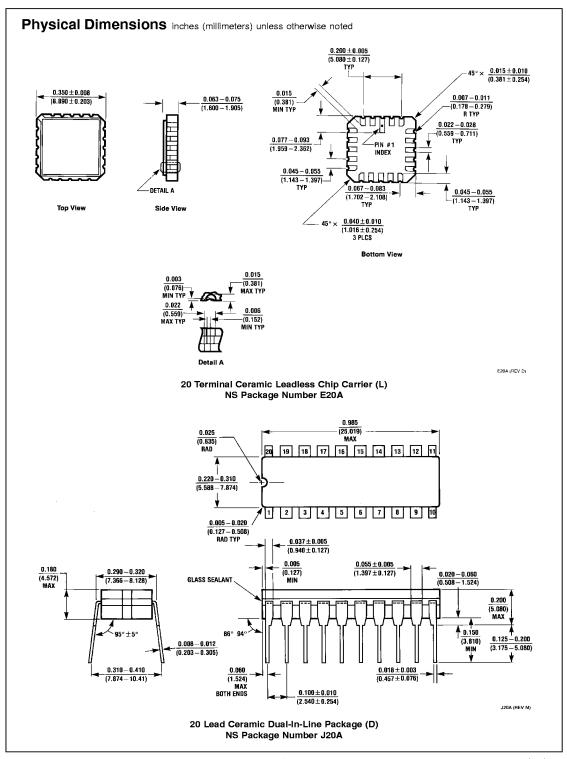
Note 11: Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

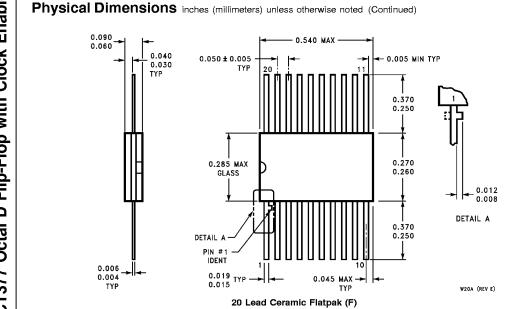
AC Operating Requirements							
			54ACT				
		v <sub>cc</sub>	T <sub>A</sub> = -55°C		Fig.		
Symbol	Parameter	(V)	to +125°C	Units	No.		
		(Note	C <sub>L</sub> = 50 pF				
		12)		4			
			Guaranteed				
			Minimum				
t <sub>s</sub>	Setup Time, HIGH or LOW	5.0	7.0	ns			
	D <sub>n</sub> to CP						
t <sub>h</sub>	Hold Time, HIGH or LOW	5.0	1.0	ns			
	D <sub>n</sub> to CP						
t <sub>s</sub>	Setup Time, HIGH or LOW	5.0	7.0	ns			
	CE to CP						
t <sub>h</sub>	Hold Time, HIGH or LOW	5.0	1.0	ns			
	CE to CP						
t <sub>w</sub>	CP Pulse Width	5.0	5.5	ns			
	HIGH or LOW						

Note 12: Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance

Symbol	Parameter	Тур	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation	90.0	pF	$V_{CC} = 5.0V$
	Capacitance			





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