

Silicon PNP Power Transistors

2SA882

DESCRIPTION

- With TO-3 package
- Excellent Safe Operating Area

APPLICATIONS

- For power and switching applications

PINNING

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

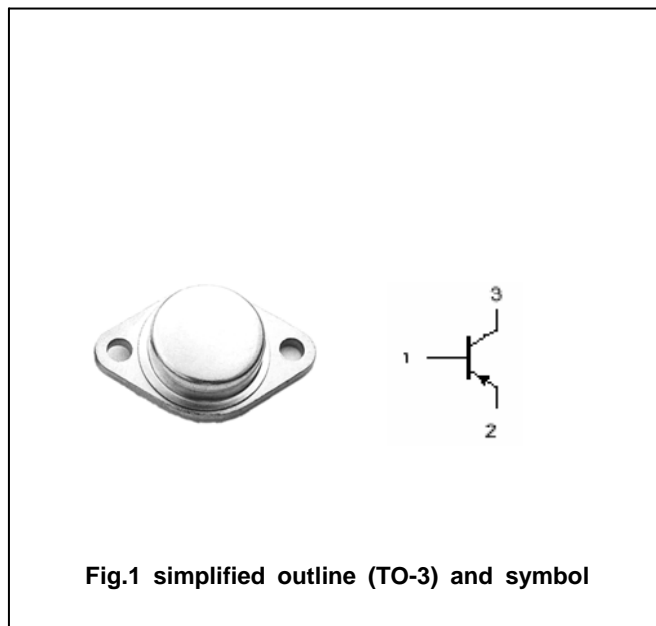


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CB0}	Collector-base voltage	Open emitter	-130	V
V _{CEO}	Collector-emitter voltage	Open base	-130	V
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current		-7	A
P _C	Collector power dissipation	T _C =25°C	100	W
T _j	Junction temperature		150	°C
T _{stg}	Storage temperature		-65~200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-c}	Thermal resistance junction to case	1.52	°C/W

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-30mA ; I _B =0	-130			V
V _{CEsat-1}	Collector-emitter saturation voltage	I _C =-3A; I _B =-0.3A			-1.0	V
V _{CEsat-2}	Collector-emitter saturation voltage	I _C =-7A ; I _B =-1.5A			-3.0	V
V _{BE}	Base-emitter on voltage	I _C =-3A ; V _{CE} =-4V			-1.6	V
I _{CBO}	Collector cut-off current	V _{CE} =-130V; I _B =0			-0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-0.1	mA
h _{FE-1}	DC current gain	I _C =-1A ; V _{CE} =-4V	40			
h _{FE-2}	DC current gain	I _C =-3A ; V _{CE} =-4V	20			

PACKAGE OUTLINE

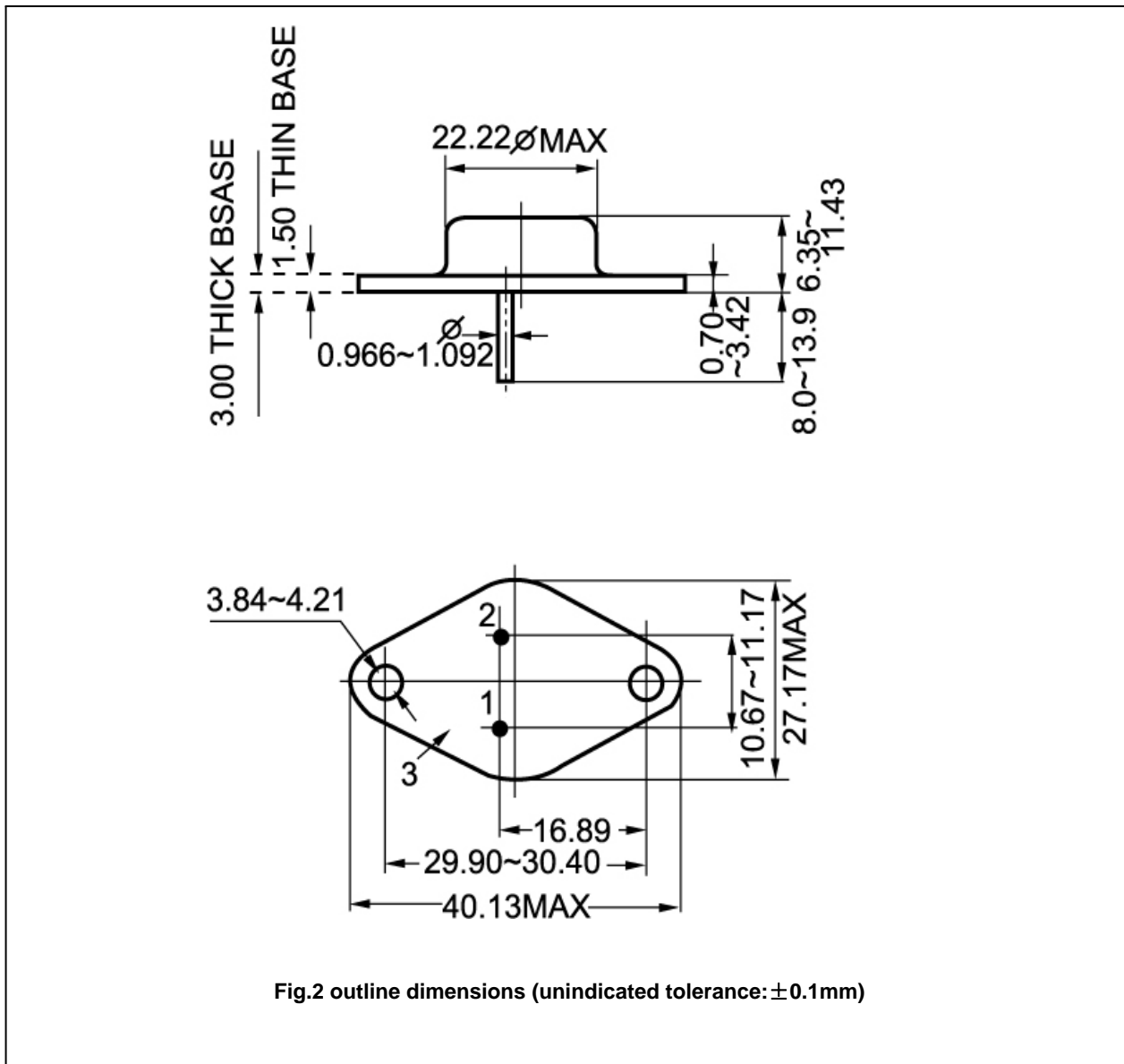


Fig.2 outline dimensions (unindicated tolerance: $\pm 0.1\text{mm}$)