National Semiconductor

October 4, 2010

LM4050QML

Precision Micropower Shunt Voltage Reference

General Description

The LM4050QML precision voltage reference is available in a 10 Lead Ceramic SOIC package. The LM4050QML's design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4050QML easy to use. The LM4050-2.5QML has a 60 µA minimum and 15 mA maximum operating current.

The LM4050QML utilizes fuse and zener-zap reverse breakdown voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

The LM4050QML operates over the temperature range of -55°C to +125°C.

Features

- Low Dose Rate Qualified 100 krad(Si)
- SEFI Immune
- SET Immune with 60µF C_{LOAD}
- C_{LOAD} 0µF to 100µF
- Fixed reverse breakdown voltage of 2.500V

Key Specifications LM4050-2.5QML

- Output voltage tolerance I_R = 100µA ±0.1% (max)
- Low temperature coefficient 17 ppm/°C
- Low output noise 50 μV_{rms}(typ)
- Wide operating current range 60 µA to 15 mA

Applications

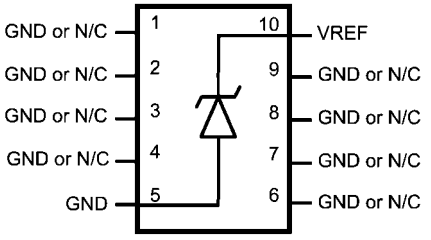
- Control Systems
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management

Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
LM4050WG2.5RLQV **Low Dose Rate Qualified**	5962R0923561VZA 100 krad(Si)	WG10A	10LD Ceramic SOIC
LM4050WG2.5-MPR **Pre-Flight Prototype**		WG10A	10LD Ceramic SOIC

Connection Diagram

10L Ceramic SOIC



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Top View
See NS Package Number WG10A

Pin Descriptions

Pin Number	Pin Name	Function
1	GND/NC	Ground or No Connect
2	GND/NC	Ground or No Connect
3	GND/NC	Ground or No Connect
4	GND/NC	Ground or No Connect
5	GND	Ground
6	GND/NC	Ground or No Connect
7	GND/NC	Ground or No Connect
8	GND/NC	Ground or No Connect
9	GND/NC	Ground or No Connect
10	VREF	Reference Voltage

Absolute Maximum Ratings (*Note 1*)

Reverse Current	20 mA
Forward Current	10 mA
Power Dissipation (T_A = 25°C) (*Note 2*)	
10LD Ceramic SOIC Package	467 mW
Lead Temperature (Soldering, 10 seconds)	
Ceramic SOIC	260°C
Storage Temperature	-65°C to +150°C
Package Weight (typical)	
Ceramic SOIC	241mg
ESD Tolerance (*Note 3*)	Class 2 (2000V)

Operating Ratings (*Note 2*)

Temperature Range	-55°C ≤ T_A ≤ +125°C
Reverse Current	
LM4050-2.5QML	60 µA to 15 mA

Package Thermal Resistance

Package	θ_{JA} (Still Air)	θ_{JA} (500LF/Min Air flow)	θ_{JC}
10L Ceramic SOIC Package on 2 layer, 1oz PCB	214°C/ W	147°C/ W	20.87°C/ W

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Setting time at	+25
13	Setting time at	+125
14	Setting time at	-55

LM4050-2.5QML Electrical Characteristics

The initial Reverse Breakdown Voltage tolerance is ±0.1% @ 100µA.

Symbol	Parameter	Conditions	Notes	Typical (*Note 4*)	Min	Max	Units	Sub-groups
V_R	Reverse Breakdown Voltage	I_R = 100 µA		2.500			V	
	Reverse Breakdown Voltage Tolerance	I_R = 60µA				±2.5	mV	1
		I_R = 100µA				±2.5		
		I_R = 1mA				±3.75		
		I_R = 10mA				±10		
		I_R = 15mA				±13		
		I_R = 60µA				**±5**	mV	2
		I_R = 100µA				**±5**		
		I_R = 1mA				**±6.25**		
		I_R = 10mA				**±12.5**		
		I_R = 15mA				**±14**		
		I_R = 60µA				**±4.5**	mV	3
		I_R = 100µA				**±4.5**		
		I_R = 1mA				**±5.75**		
		I_R = 10mA				**±13**		
		I_R = 15mA				**±17.5**		
I_{RMIN}	Minimum Operating Current			40.5		60	µA	1
						65	µA	2, 3
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient @ 25°C ≤ T_A ≤ 125°C	I_R = 60µA	(*Note 8*)	±3		**±17**	ppm/°C	2
		I_R = 100µA		±3		**±17**		
		I_R = 1mA		±3		**±20**		
		I_R = 10mA		±4		**±25**		
		I_R = 15mA		±6				
	Average Reverse Breakdown Voltage Temperature Coefficient @ −55°C ≤ T_A ≤ 25°C	I_R = 60µA	(*Note 8*)	±3		**±19**		3
		I_R = 100µA		±3		**±19**		
		I_R = 1mA		±3.5		**±22**		
		I_R = 10mA		±35		**±55**		
		I_R = 15mA		±60				
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, I_{AC} = 0.1 I_R		0.3			Ω	
V_N	Output Noise Voltage	0.1 Hz ≤ f ≤ 10 Hz		9			µVpp	
		10 Hz ≤ f ≤ 10KHz		50			µVrms	
C_{LOAD}	Load Capacitor	Stable Over Temperature	(*Note 6*)	60	0	100	µF	
V_{HYST}	Thermal Hysteresis	ΔT = −55°C to 125°C	(*Note 5*)	1			ppm	

Post Radiation @ 25°C (*Note 7*)

The initial Reverse Breakdown Voltage tolerance is ±0.1% @ 100µA.

Symbol	Parameter	Conditions		30 krad	50 krad	100 krad	Sub-groups
V_R	Reverse Breakdown Voltage Tolerance	I_R = 60µA	Max	+0.42%	+0.67%	+1.5%	1
		I_R= 100µA					
		I_R = 1mA					
		I_R = 10mA					
		I_R = 15mA					

Post Radiation Tempco (*Note 8*)

Symbol	Parameter	Conditions	TYPICALS			
			30 krad	50 krad	100 krad	Units
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient Drift @ 25°C ≤ T_A ≤ 125°C	60µA ≤ I_R ≤ 15mA	+41	+83	+144	ppm/°C
	Average Reverse Breakdown Voltage Temperature Coefficient Drift @ –55°C ≤ T_A ≤ 25°C	60µA ≤ I_R ≤ 15mA	+46	+87	+166	ppm/°C

Operational Life Test Delta Parameters

This table represents the drift seen from initial measurements post 1000hr Operational Life Burn-In. All units will remain within the electrical characteristics limits post 1000hr Operational Life Burn-In. Deltas required for QMLV product at Group B, Sub-Group 5.

Symbol	Parameter	Conditions	Note	Min	Max	Units	Temp
V_R	Reverse Breakdonwn Voltage Tolerance	I_R = 60µA		-0.873	0.873	mV	1
		I_R = 100µA		-0.873	0.873		
		I_R = 1mA		-0.998	0.998		
		I_R = 10mA		-3.93	3.93		
		I_R = 15mA		-5	5		
I_{RMIN}	Minimum Operating Current			-0.623	0.623	µA	1

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4050QML, T_{Jmax} = 125°C, and the typical thermal resistance (θ_{JA}), when board mounted, is 214°C/W for the 10 Lead Ceramic SOIC package.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Note 4: Typicals are at T_A = 25°C and represent most likely parametric norm.

Note 5: Thermal hysteresis is defined as the change in voltage measured at +25°C after cycling to temperature -55°C and the 25°C measurement after cycling to temperature +125°C.

$$V_{HYST} = \frac{|V_{R1} - V_{R2}|}{V_R} \times 10^6 \text{ ppm}$$

Where: V_{HYST} = Thermal hysteresis expressed in ppm

V_R = Nominal preset output voltage

V_{R1} = V_R before temperature fluctuation

V_{R2} = V_R after temperature fluctuation.

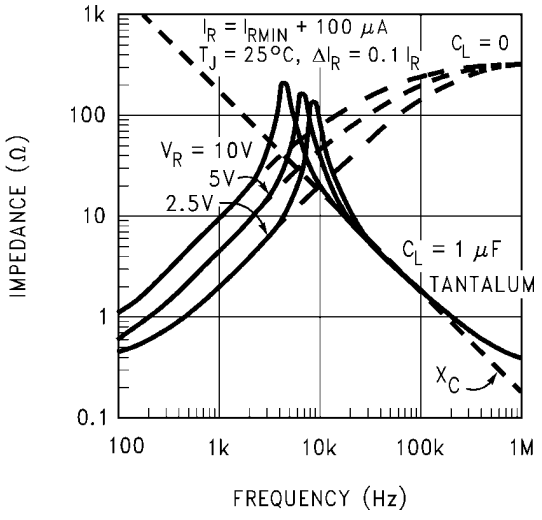
Note 6: Capacitive load not required but improves SET stability. This parameter is guaranteed by design and/or characterization and is not tested in production.

Note 7: Pre and post irradiation limits are identical to those listed under electrical characteristics except as listed in the post radiation table.

Note 8: Not tested post irradiation. Typical post irradiation values listed in the post radiation Tempco table.

Typical Performance Characteristics

Output Impedance vs Frequency



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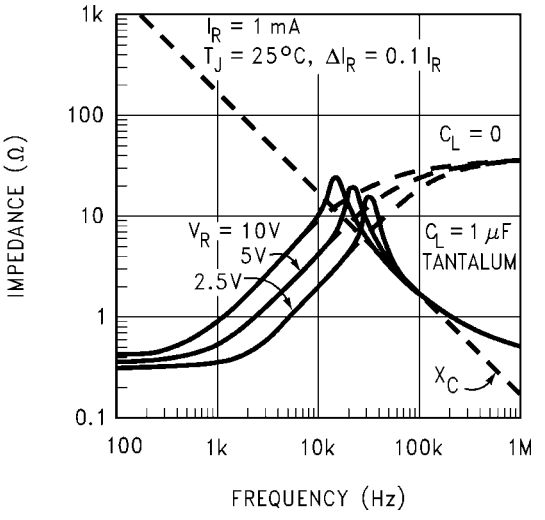
Output Impedance vs Frequency



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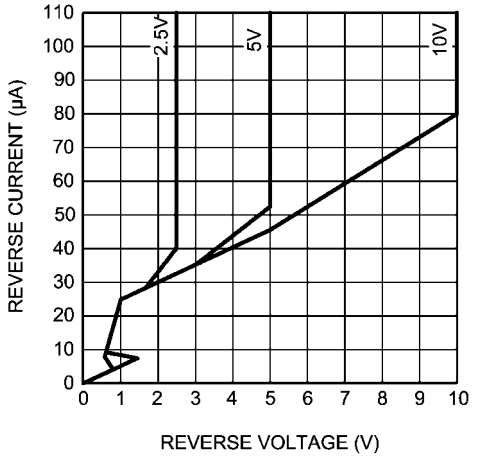
Reverse Characteristics and Minimum Operating Current



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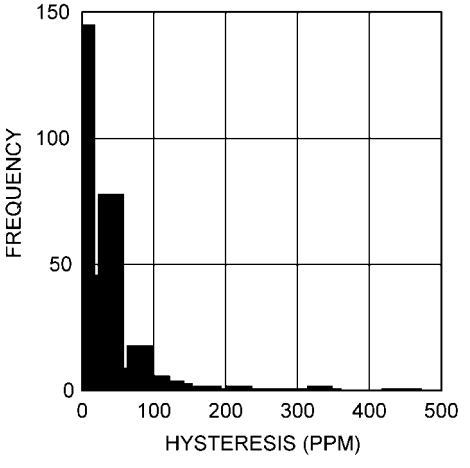
Thermal Hysteresis



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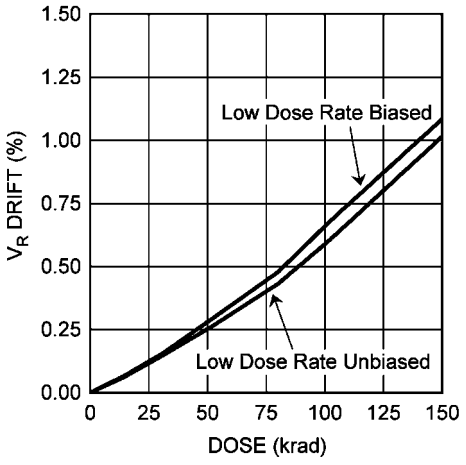
Typical Radiation Characteristics

Low Dose Rate Drift at 10 mrad(Si)/s



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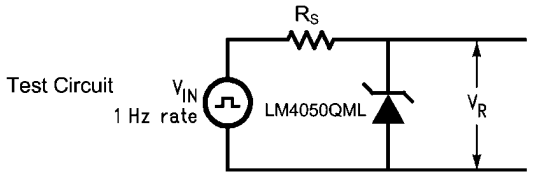
Start-Up Characteristics



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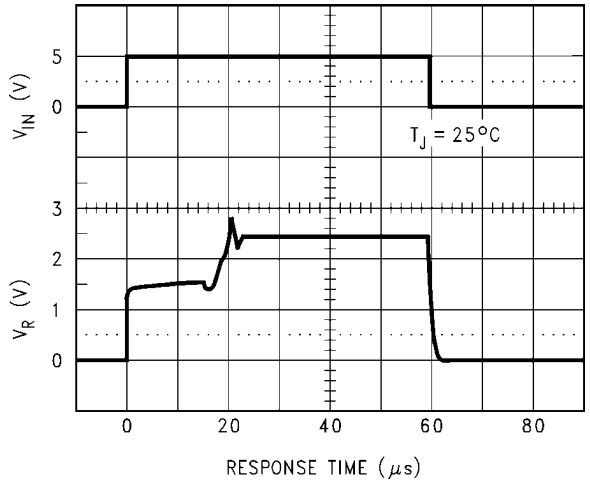
LM4050-2.5QML R_S = 30k



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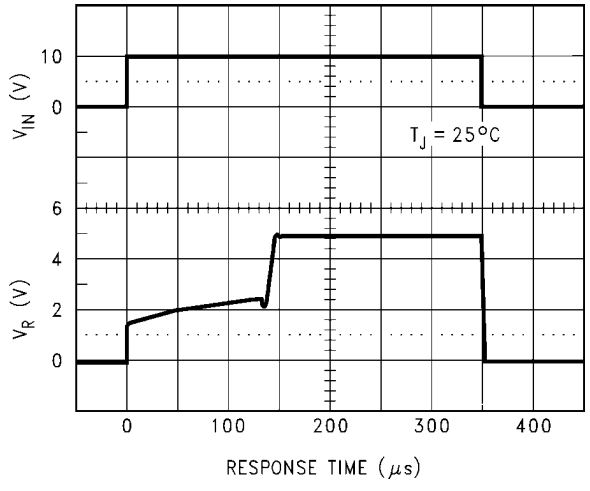
LM4050-5.0QML R_S = 30k



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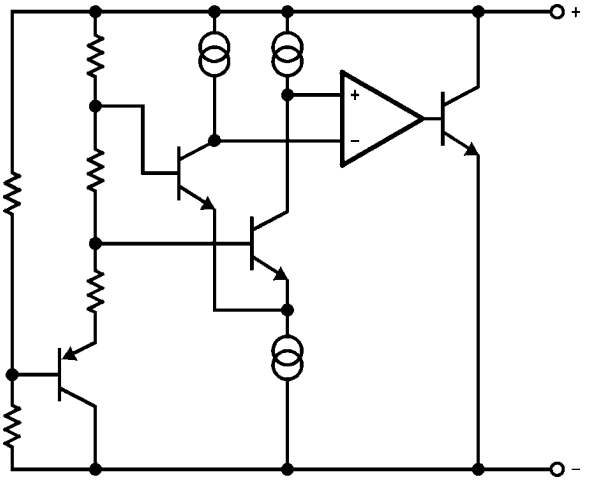
Functional Block Diagram



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Applications Information

The LM4050QML is a precision micro-power curvature-corrected bandgap shunt voltage reference. The LM4050QML is available in the 10 Lead Ceramic SOIC package. The LM4050QML has been designed for stable operation without the need of an external capacitor connected between the "+" pin and the "–" pin. If, however, a bypass capacitor is used, the LM4050QML remains stable. The LM4050-2.5QML has a 60 µA minimum and 15 mA maximum operating current.

The typical thermal hysteresis specification is defined as the change in +25°C voltage measured after thermal cycling. The device is thermal cycled to temperature -55°C and then measured at 25°C. Next the device is thermal cycled to temperature +125°C and again measured at 25°C. The resulting V_{OUT} delta shift between the 25°C measurements is thermal hysteresis. Thermal hysteresis is common in precision references and is induced by thermal-mechanical package stress. Changes in environmental storage temperature, operating temperature and board mounting temperature are all factors that can contribute to thermal hysteresis.

In a conventional shunt regulator application (*Figure 1*) , an external series resistor (R_S) is connected between the supply voltage and the LM4050QML. R_S determines the current that flows through the load (I_L) and the LM4050QML (I_Q). Since load current and supply voltage may vary, R_S should be small enough to supply at least the maximum guaranteed I_{RMIN} (spec. table) to the LM4050QML even when the supply voltage is at its minimum and the load current is at its maximum value. When the supply voltage is at its maximum and I_L is at its minimum, R_S should be large enough so that the current flowing through the LM4050QML is less than 15 mA.

R_S is determined by the supply voltage, (V_S), the load and operating current, (I_L and I_Q), and the LM4050QML's reverse breakdown voltage, V_R.

$$R_S = \frac{V_S - V_R}{I_L + I_Q}$$

Radiation Environments

Careful consideration should be given to environmental conditions when using a product in a radiation environment.

TOTAL IONIZING DOSE

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the Ordering Information table on the front page. Testing and qualification of these products is done on a wafer level according to MIL-STD-883, Test Method 1019. Wafer level TID data is available with lot shipments.

Testing and qualification is performed at the 30, 50 and 100 krad TID levels at a dose rate of 10 mrad/s, using a 1.5X overtest at each TID level. For the 30 krad level units are tested to 50 krad, for 50 krad units are tested to 80 krad and for 100 krad units are tested to 150 krad, with all parameters remaining inside the post irradiation test limits.

SINGLE EVENT EFFECTS (SEE)

One time single event effects characterization was performed according to EIA/JEDEC Standard, EIA/JEDEC57.

A test report is available upon request.

SINGLE EVENT TRANSIENTS (SET)

With a 60 µF capacitor on the output, no single event transients were seen at the highest linear energy transfer (LET) tested: 59 MeV-cm^2/mg.

SET characterization with other capacitor values is in the SEE report, available upon request.

SINGLE EVENT FUNCTIONAL INTERRUPT (SEFI)

No single event functional interrupts were detected to the highest linear energy transfer (LET) tested: 100 MeV-cm^2/mg.

Typical Applications

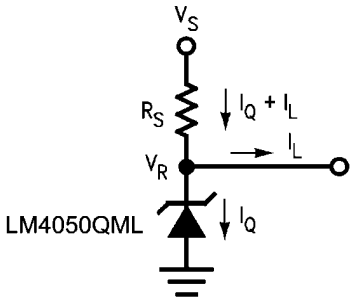


FIGURE 1. Shunt Regulator

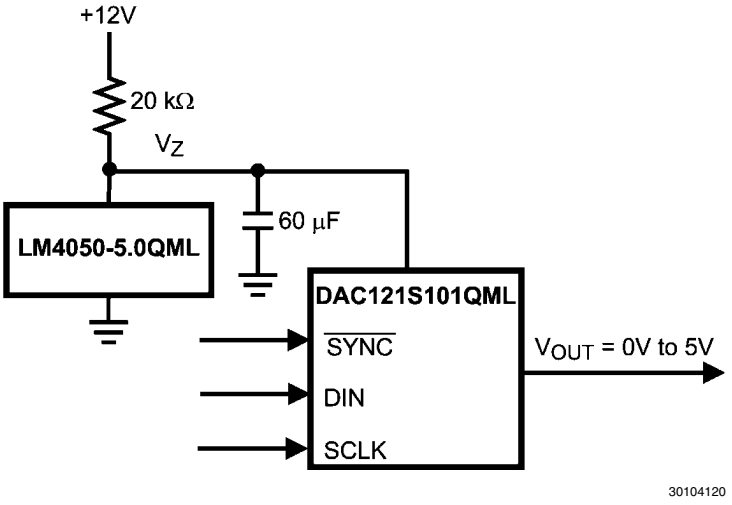


FIGURE 2. The LM4050QML as a power supply and reference

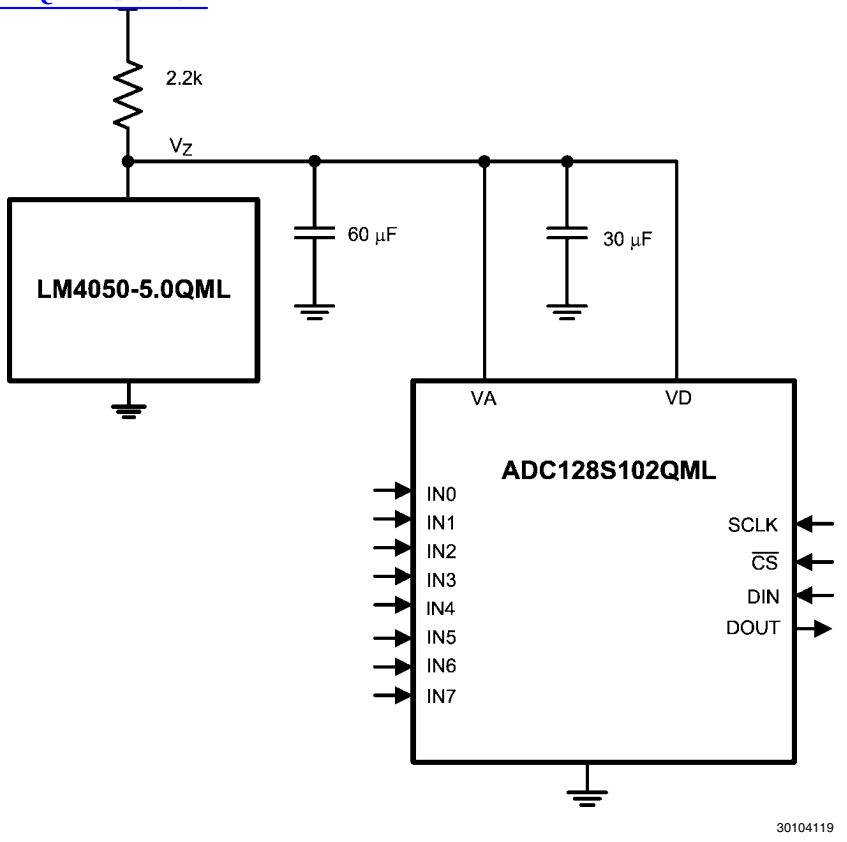


FIGURE 3. The LM4050QML as a power supply and reference

The LM4050QML is a good choice as a power regulator for the DAC121S101QML or ADC128S102QML. The minimum resistor value in the circuit of *Figure 2* or *Figure 3* should be chosen such that the maximum current through the LM4050QML does not exceed its 15 mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050QML voltage at its minimum, the resistor value at its minimum due to tolerance, and the DAC121S101QML or ADC128S102QML draws zero current. The maximum resistor value must allow the LM4050QML to draw more than its minimum current for regulation plus the maximum DAC121S101QML or ADC128S102QML current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050QML voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC121S101QML or ADC128S102QML draws its maximum current. These conditions can be summarized as

$$R(min) = (V_{IN}(max) - V_Z(min) / (I_A(min) + I_Z(max)$$

and

$$R(max) = (V_{IN}(min) - V_Z(max) / (I_A(max) + I_Z(min)$$

where $V_Z(min)$ and $V_Z(max)$ are the nominal LM4050QML output voltages ± the LM4050QML output tolerance over temperature, $I_Z(max)$ is the maximum allowable current through the LM4050QML, $I_Z(min)$ is the minimum current required by the LM4050QML for proper regulation, $I_A(max)$ is the maximum DAC121S101QML or ADC128S102QML supply current, and $I_A(min)$ is the minimum DAC121S101QML or ADC128S102QML supply current.

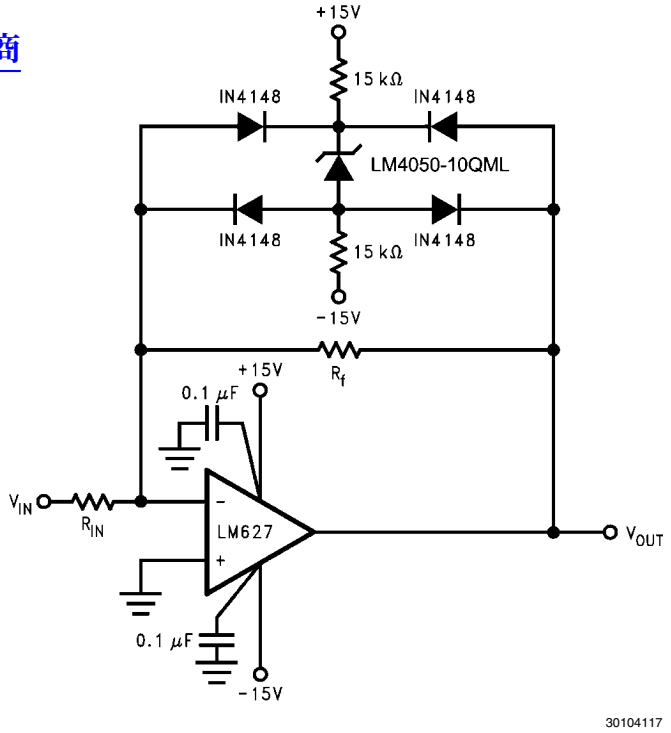


FIGURE 4. Bounded amplifier reduces saturation-induced delays and can prevent succeeding stage damage. Nominal clamping voltage is ±11.5V (LM4050QML's reverse breakdown voltage +2 diode V_F).

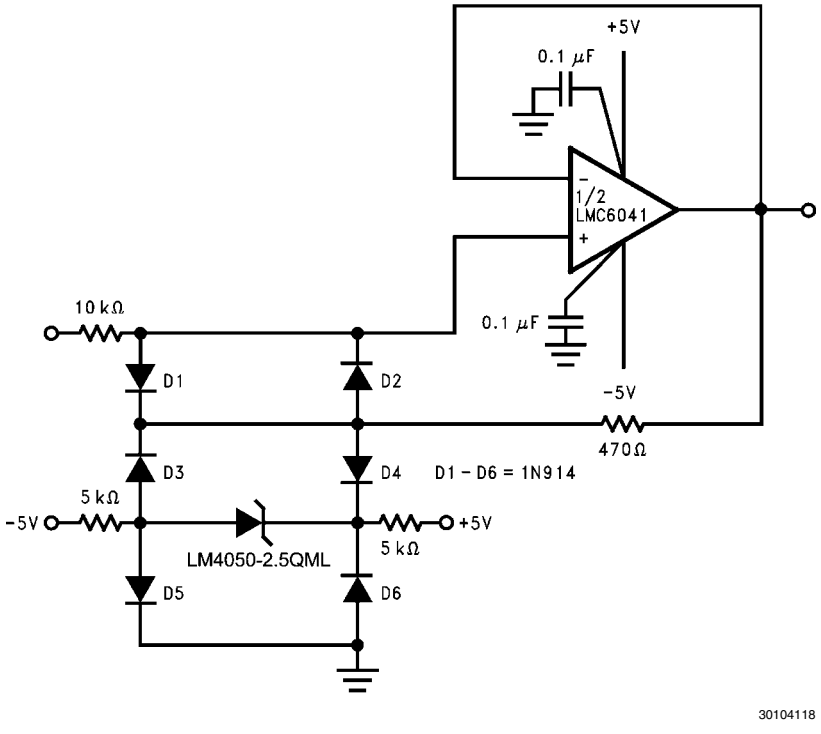
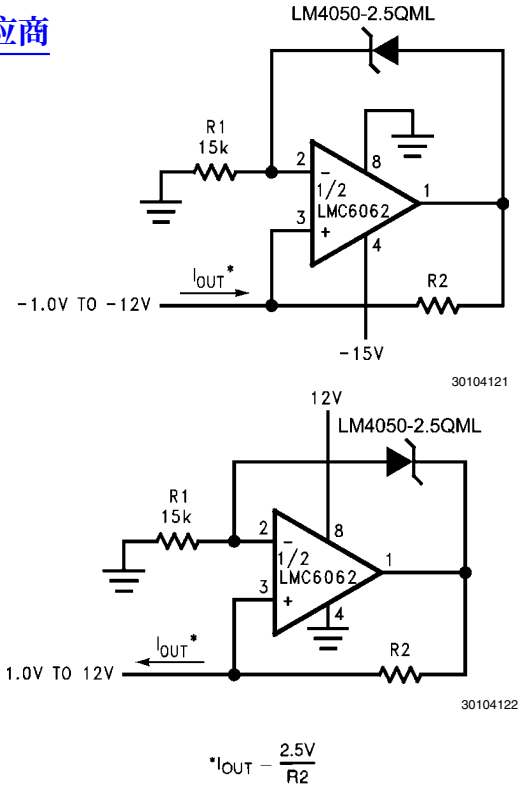


FIGURE 5. Protecting Op Amp input. The bounding voltage is ±4V with the LM4050-2.5QML (LM4050QML's reverse breakdown voltage + 3 diode V_F).



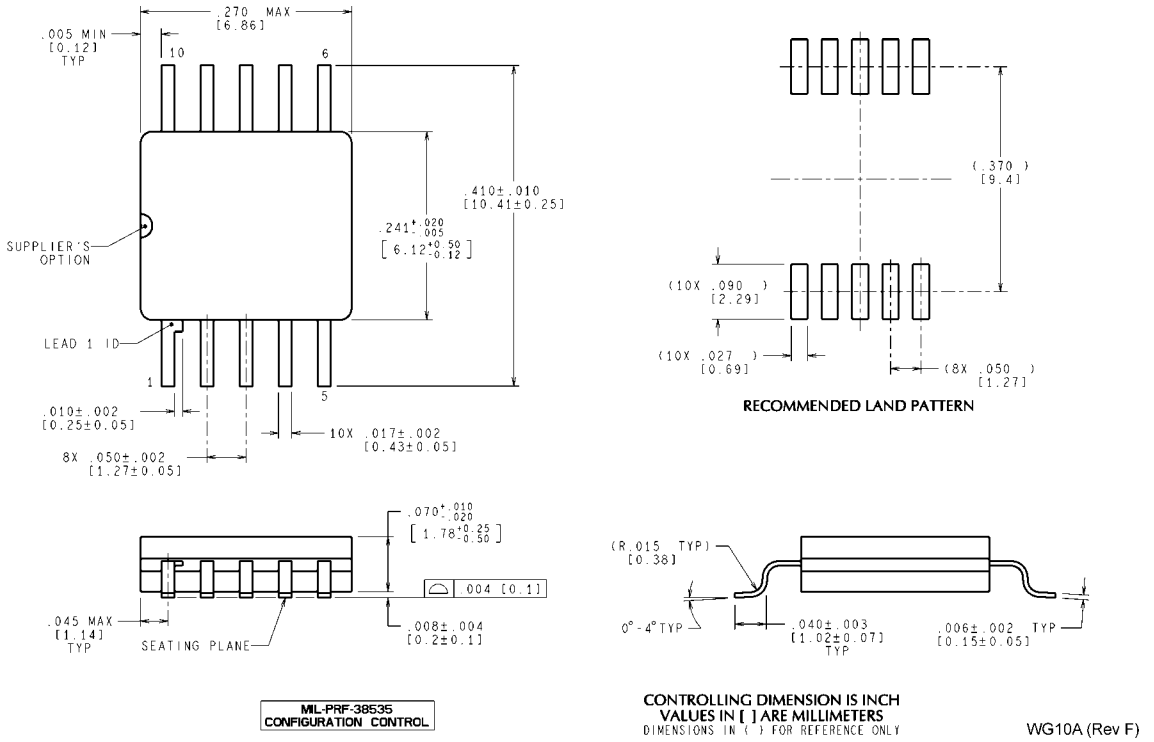
$$*I_{OUT} = \frac{2.5V}{R2}$$

FIGURE 6. Precision 1 µA to 1 mA Current Sources

Revision History

Date Released	Revision	Section	Changes
08/20/2010	A	Initial Release	New Product Low Dose Qualified LM4050WG2.5RLQV Initial Release

Physical Dimensions inches (millimeters) unless otherwise noted



ML-PRF-38535
CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

WG10A (Rev F)

10 Lead Ceramic SOIC
NS Package Number WG10A

Notes

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LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
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