FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27229-2E

ASSP

For Power Supply Applications (General Purpose DC/DC Converter)

2-Channel DC/DC Converter IC
with Overcurrent Protection Symmetrical-Phase Type

MB3889

■ DESCRIPTION

The MB3889 is a symmetrical-phase type of two-channel, DC/DC converter IC using pulse width modulation (PWM) , incorporating an overcurrent protection circuit (requiring no current sense resistor) and an overvoltage protection circuit. Providing high output driving capabilities, the MB3889 is suitable for down-conversion.
The MB3889 adopts both synchronous rectification to provide high efficiency and symmetrical phasing (two anti-phase triangular waves) which contributes to making the input capacitor small.
The MB3889 contains a 5-volt regulator resulting in a reduced number of components used. It also contains a variety of protection features which output the protection status upon detection of an overvoltage or overcurrent while reducing the number of external protective devices required.
The result is an ideal built-in power supply for driving products with high speed CPU's such as home TV game devices and notebook PC's.
This product is covered by US Patent Number 6,147,477.

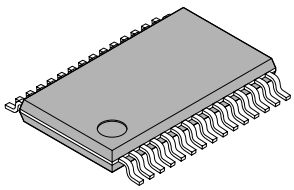
■ FEATURES

- Built-in timer-latch overcurrent protection circuit (requiring no current sense resistor)
- Built-in timer-latch overvoltage protection circuit
- Synchronous rectification system providing high efficiency
- Power supply voltage range: 5.5 V to 18 V
- PWRGOOD terminals (open-drain) to output the protection status
- Symmetrical-phase system reducing the input capacitor loss
- Built-in channel control function
- Reference voltage: 3.5 V ± 1 %

(Continued)

■ PACKAGE

30-pin plastic TSSOP



(FPT-30P-M04)

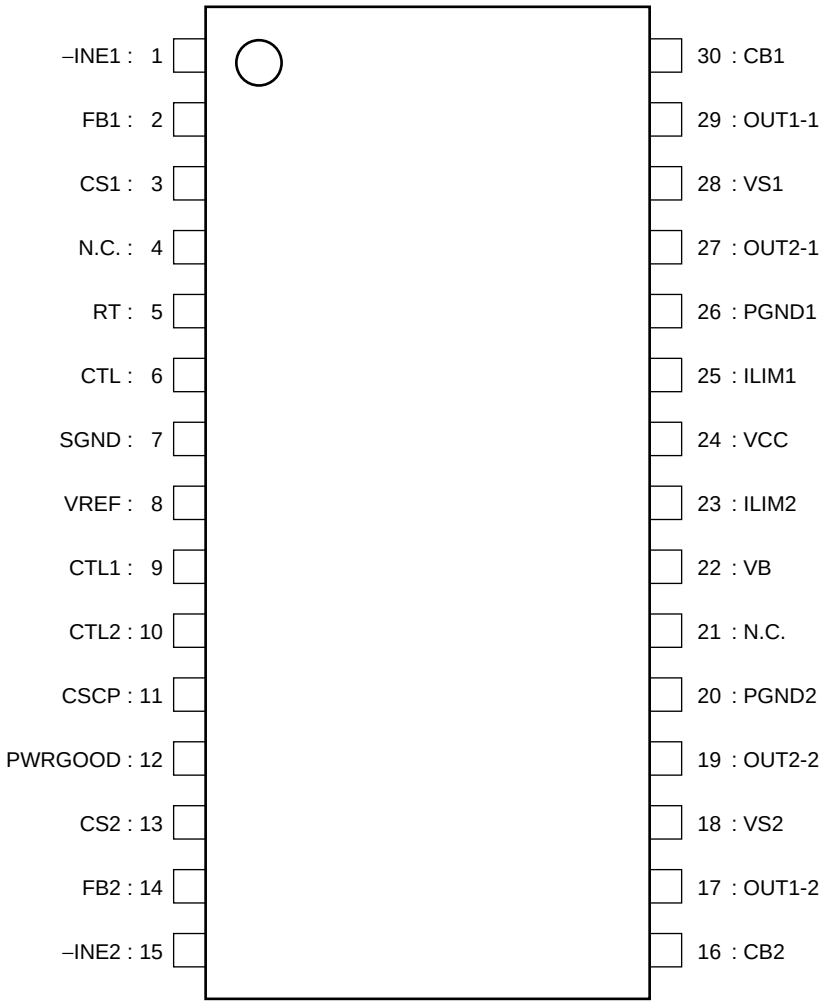
FUJITSU

(Continued)

- Error amplifier threshold voltage: 1.23 V ± 1 % (0 °C to + 85 °C)
- Support for frequency setting using an external resistor (Frequency setting capacitor integrated)
- Oscillation frequency range: 100 kHz to 500 kHz
- Built-in circuit for load-independent soft-start and discharge control
- Built-in totem-pole output for Nch MOS FET

■ PIN ASSIGNMENT

(TOP VIEW)

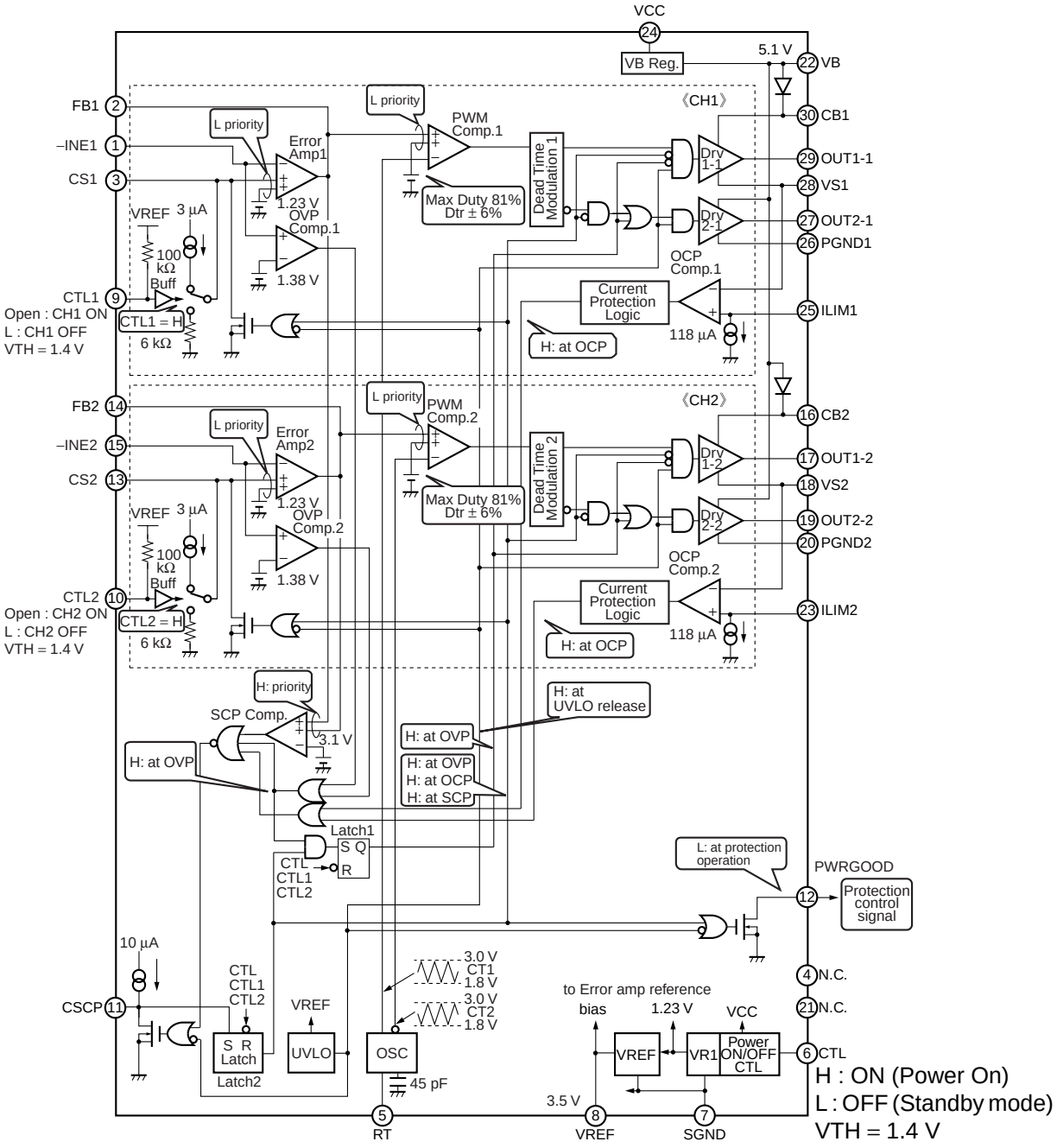


(FPT-30P-M04)

■ PIN DESCRIPTION

Pin No.	Symbol	I/O	Descriptions
1	–INE1	I	CH1 error amp inverted input terminal
2	FB1	O	CH1 error amp output terminal
3	CS1	—	CH1 soft-start capacitor connection terminal
4	N.C.	—	No connection
5	RT	—	Triangular waveform oscillation frequency setting resistor connection terminal
6	CTL	I	Power supply control terminal. “H” level : IC operating mode “L” level : IC Standby mode
7	SGND	—	Ground terminal
8	VREF	O	Reference voltage output terminal
9	CTL1	I	CH1 control terminal “H” level : CH1 ON state “L” level : CH1 OFF state and protection status reset
10	CTL2	I	CH2 control terminal “H” level : CH2 ON state “L” level : CH2 OFF state and protection status reset
11	CSCP	—	Timer-latch short-circuit protection capacitor connection terminal
12	PWRGOOD	O	CH1, CH2 protection status output terminal
13	CS2	—	CH2 soft-start capacitor connection terminal
14	FB2	O	CH2 error amp output terminal
15	–INE2	I	CH2 error amp inverted input terminal
16	CB2	—	CH2 boot capacitor connection terminal Connect a capacitor between the CB2 and VS2 terminals.
17	OUT1-2	O	CH2 totem-pole output terminal (External main-side FET gate drive)
18	VS2	—	CH2 external main-side FET source connection terminal
19	OUT2-2	O	CH2 totem-pole output terminal (External synchronous-rectification-side FET gate drive)
20	PGND2	—	Ground terminal
21	N.C.	—	No connection
22	VB	O	Output circuit bias output terminal
23	ILIM2	I	CH2 overcurrent detection resistor connection terminal
24	VCC	—	Reference voltage, control circuit power supply terminal
25	ILIM1	I	CH1 overcurrent detection resistor connection terminal
26	PGND1	—	Ground terminal
27	OUT2-1	O	CH1 totem-pole output terminal (External synchronous-rectification-side FET gate drive)
28	VS1	—	CH1 external main-side FET source connection terminal
29	OUT1-1	O	CH1 totem-pole output terminal (External main-side FET gate drive)
30	CB1	—	CH1 boot capacitor connection terminal Connect a capacitor between the CB1 and VS1 terminals.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power-supply voltage	V_{CC}	—	—	20	V
Boot voltage	V_{CB}	CB terminal	—	25	V
Output current	I_O	—	—	120	mA
Peak output current	I_{OP}	Duty ≤ 5% ($t = 1 / f_{OSC} \times$ Duty)	—	800	mA
Power dissipation	P_D	Ta ≤ +25 °C	—	1390*	mW
Storage temperature	T_{STG}	—	−55	+125	°C

* : The packages are mounted on the dual-sided epoxy board (10 cm × 10 cm) .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power-supply voltage	V_{CC}	—	5.5	12	18	V
Boot voltage	V_{CB}	CB terminal	—	—	23	V
Reference voltage output current	I_{OR}	VREF terminal	− 1	—	0	mA
Bias output current	I_{OB}	VB terminal	− 1	—	0	mA
Input voltage	V_{IN}	–INE terminal	0	—	V_{CC} − 1.8	V
	V_{CTL}	CTL1, CTL2 terminal	0	—	V_{REF}	V
		CTL terminal	0	—	V_{CC}	V
Output voltage	V_{PG}	PWRGOOD terminal	0	—	15	V
Output current	I_O	—	− 100	—	100	mA
Peak output current	I_{OP}	Duty ≤ 5% ($t = 1 / f_{OSC} \times$ Duty)	− 700	—	700	mA
Oscillation frequency	f_{OSC}	—	100	300	500	kHz
Timing resistor	R_T	—	30	47	130	kΩ
Boot capacitor	C_B	—	—	0.1	1.0	µF
Reference voltage output capacitor	C_{REF}	VREF terminal	—	0.1	1.0	µF
Bias output capacitor	C_{VB}	VB terminal	1.0	4.7	10	µF
Soft-start capacitor	C_S	—	—	0.1	1	µF
Short-circuit detection capacitor	C_{SCP}	—	—	0.01	1	µF
Overcurrent detection setting resistor	R_{LIM}	—	0.1	1	10	kΩ
Operating ambient temperature	Ta	—	− 30	+ 25	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = 12 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
1. Reference Voltage Block [REF]	Output voltage	V_{REF}	8	Ta = + 25 °C	3.465	3.500	3.535	V
		$\Delta V_{REF}/V_{REF}$	8	Ta = 0 °C to + 85 °C	—	0.5*	—	%
	Input stability	Line	8	VCC = 5.5 V to 18 V	—	1	10	mV
	Load stability	Load	8	VREF = 0 mA to – 1 mA	—	3	10	mV
	Short-circuit output current	I_{OS}	8	VREF = 0 V	– 40	– 20	– 10	mA
2. Bias Voltage Block [VB]	Output voltage	V_B	22	—	5.0	5.1	5.2	V
3. Triangular Waveform Oscillator Block [OSC]	Oscillation frequency	f_{OSC}	17, 29	RT = 47 kΩ	270	300	330	kHz
	Frequency/ temperature variation	$\Delta f_{OSC}/f_{OSC}$	17, 29	Ta = 0 °C to + 85 °C	—	1*	—	%
4. Undervolt-age (VCC) Lockout Circuit Block [UVLO]	Threshold voltage	V_{TH}	8	VREF = ↗	2.6	2.8	3.0	V
	Hysteresis width	V_H	8	—	—	0.2*	—	V
5. Short-circuit Protection Circuit Block [SCP]	Threshold voltage	V_{TH}	11	—	0.65	0.70	0.75	V
	Input source current	I_{CSCP}	11	—	– 14	– 10	– 6	µA
	Reset voltage	V_{RST}	8	VREF = ↘	1.7	2.1	2.5	V
6. Overcurrent Protection Circuit Block [OCP]	ILIM terminal input current	I_{LIM}	23, 25	RT = 47 kΩ	106	118	130	µA
	Offset voltage	V_{IO}	23, 25	—	—	1*	—	mV
7. Overvoltage Protection Circuit Block [OVP]	Threshold voltage	V_{TH}	1, 15	–INE = ↗	1.35	1.38	1.41	V
	Input bias current	I_B	1, 15	–INE = 0 V	–730	–110	—	nA
8.Protection Status Output Cirsuit Block [PWRGOOD]	Output leakage current	I_{LEAK}	12	PWRGOOD = 5 V	—	—	40	µA
	Output "L" level voltage	V_{OL}	12	PWRGOOD = 1 mA	—	0.1	0.4	V
9. Soft-start Circuit Block [CS]	Charge current	I_{CS}	3, 13	—	– 4.2	– 3.0	– 1.8	µA

*: Standard design value

(Continued)

(VCC = 12 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
10. Error Amp Block [Error Amp]	Threshold voltage	V_{TH1}	1, 15	FB = 2.4 V, Ta = + 25 °C	1.221	1.230	1.239	V
		V_{TH2}	1, 15	FB = 2.4 V, Ta = 0 °C to + 85 °C	1.218	1.230	1.242	V
	Input bias current	I_B	1, 15	–INE = 0 V	– 730	– 110	—	nA
	Voltage gain	A_V	2, 14	DC	60	100	—	dB
	Frequency bandwidth	BW	2, 14	A_V = 0 dB	—	1.5*	—	MHz
	Output voltage	V_{FBH}	2, 14	—	3.2	3.4	—	V
		V_{FBL}	2, 14	—	—	40	200	mV
	Output source current	I_{SOURCE}	2, 14	FB = 2.4 V	—	– 2	– 1	mA
	Output sink current	I_{SINK}	2, 14	FB = 2.4 V	150	250	—	µA
11. PWM Comparator Block [PWM Comp.]	Threshold voltage	V_{TL}	2, 14	Duty cycle = 0 %	1.7	1.8	—	V
		V_{TH}	2, 14	Duty cycle = Dtr	—	2.86	3.00	V
12. Dead Time Control Block [DTC]	Maximum duty cycle	Dtr	17, 29	RT = 47 kΩ	75	81	87	%
13. Output Block [Drive]	Output current (main side)	$I_{SOURCE1}$	17, 29	OUT1 = 12 V, CB = 17 V, VS = 12 V, Duty ≤ 5 % (t = 1/ f_{OSC} × Duty)	—	– 700*	—	mA
		I_{SINK1}	17, 29	OUT1 = 17 V, CB = 17 V, VS = 12 V, Duty ≤ 5 % (t = 1/ f_{OSC} × Duty)	—	900*	—	mA
	Output voltage (main side)	V_{OH1}	17, 29	OUT1 = – 100 mA, CB = 17 V, VS = 12 V	V_{CB} – 2.5	V_{CB} – 0.9	—	V
		V_{OL1}	17, 29	OUT1 = 100 mA, CB = 17 V, VS = 12 V	—	V_S + 0.9	V_S + 1.4	V
	Output current (synchronous rectification side)	$I_{SOURCE2}$	19, 27	OUT2 = 0 V, Duty ≤ 5 % (t = 1/ f_{OSC} × Duty)	—	– 750*	—	mA
		I_{SINK2}	19, 27	OUT2 = 5.1 V, Duty ≤ 5 % (t = 1/ f_{OSC} × Duty)	—	900	—	mA

*: Standard design value

(Continued)

(Continued)

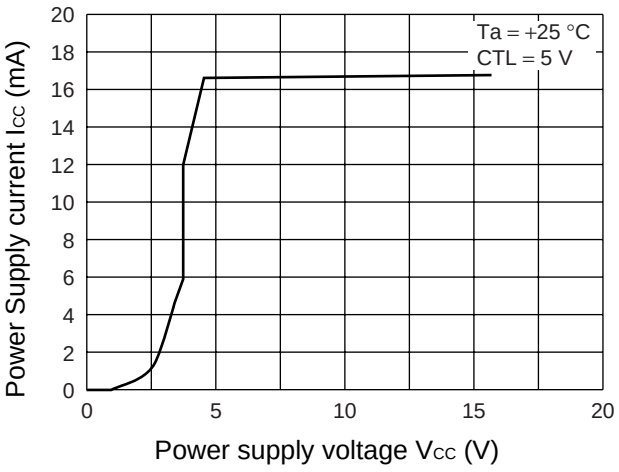
(VCC = 12 V, VB = 0 mA, VREF = 0 mA, Ta = + 25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
13. Output Block [Drive]	Output voltage (synchronous rectification side)	V_{OH2}	19, 27	OUT2 = – 100 mA	2.5	4.1	—	V
		V_{OL2}	19, 27	OUT2 = 100 mA	—	1.0	1.4	V
	Diode voltage	V_D	16, 30	VB = 10 mA	—	0.9	1.1	V
	Dead time	t_{D1}	29, 27, 17, 19	OUT1 = OUT2 = OPEN, VS = 0 V OUT2 : ↓ – OUT1 : ↑	40	80	120	ns
		t_{D2}	29, 27, 17, 19	OUT1 = OUT2 = OPEN, VS = 0 V OUT1 : ↓ – OUT2 : ↑	60	120	180	ns
14. Control Block (CTL, CTL1, CTL2) [CTL]	Output ON condition	V_{ON}	9, 10	—	2	—	V_{REF}	V
	Output OFF condition	V_{OFF}	9, 10	—	0	—	0.8	V
	Output ON condition	V_{ON}	6	—	2	—	V_{CC}	V
	Output OFF condition	V_{OFF}	6	—	0	—	0.8	V
	Input current	I_{CTL}	9, 10	CTL1 = CTL2 = 0 V	– 44	– 35	– 29	µA
			6	CTL = 5 V	—	50	75	µA
15. General	Standby current	I_{CCS}	24	CTL = 0 V	—	0	10	µA
	Power-supply current	I_{CC}	24	CTL = 5 V	—	15	23	mA

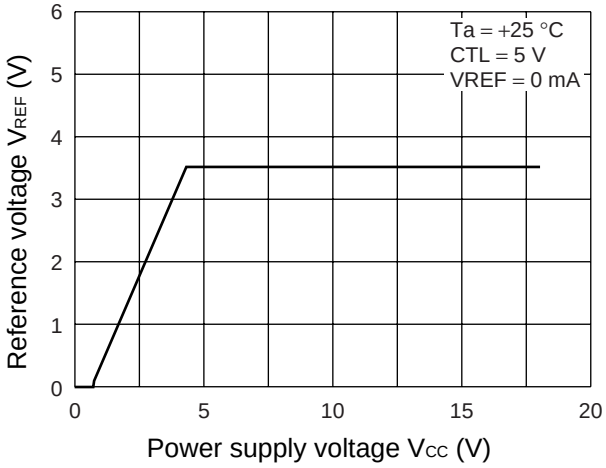
*: Standard design value

■ TYPICAL CHARACTERISTICS

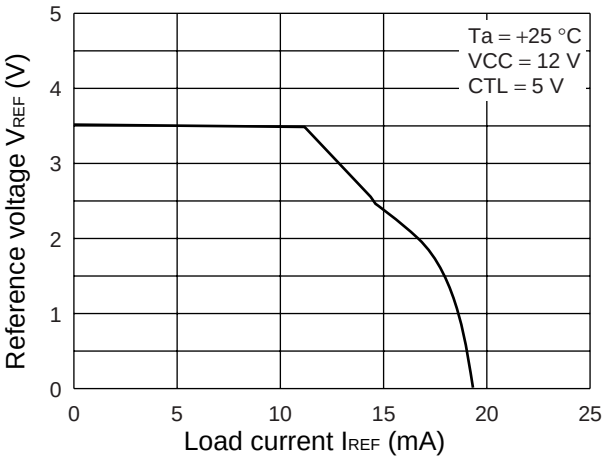
Power Supply Current vs. Power Supply Voltage



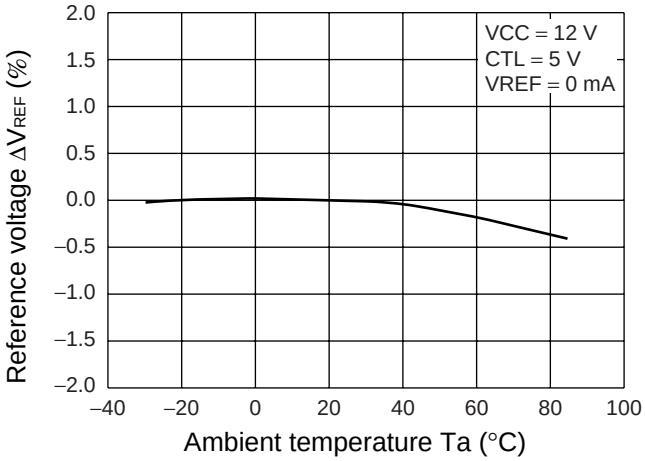
Reference Voltage vs. Power Supply Voltage



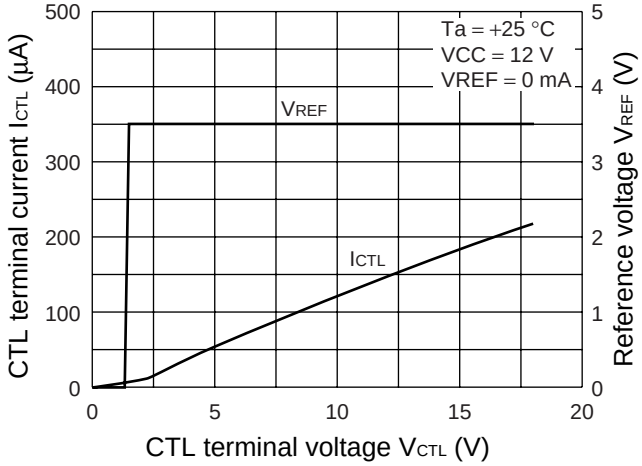
Reference Voltage vs. Load Current



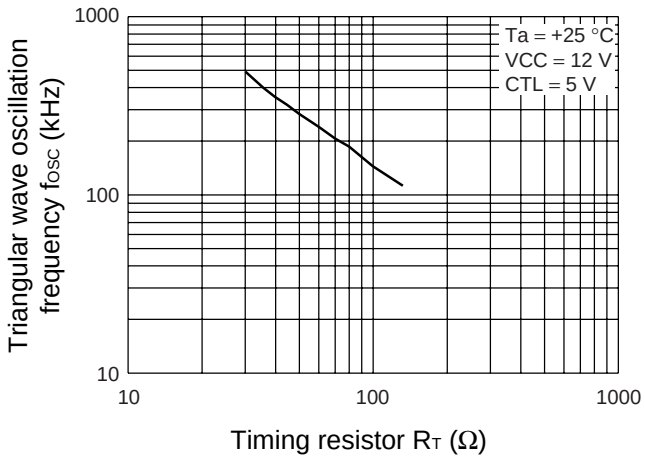
Reference Voltage vs. Ambient Temperature



CTL Terminal Current, Reference Voltage vs. CTL Terminal Voltage

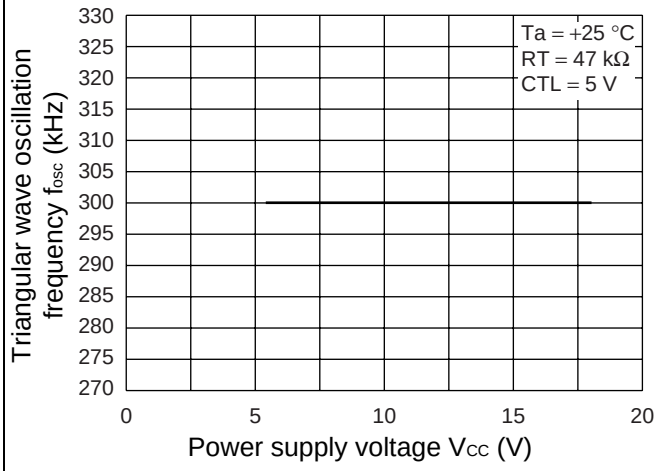


Triangular Wave Oscillation Frequency vs. Timing Resistor

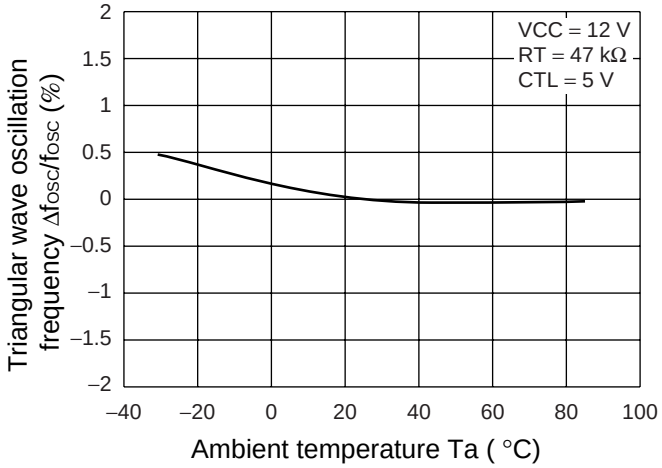


(Continued)

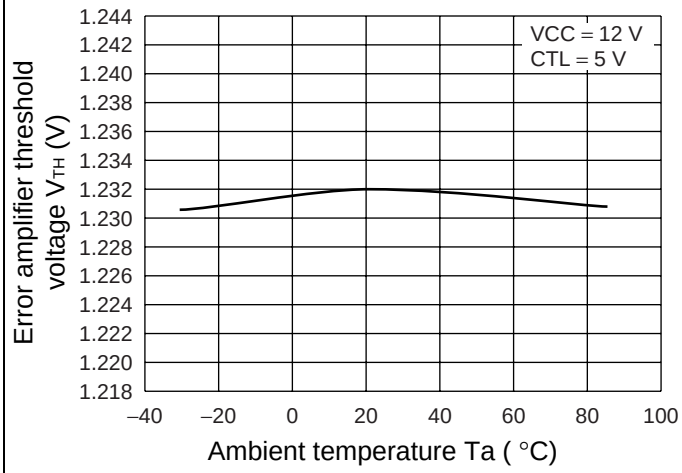
Triangular Wave Oscillation Frequency vs. Power Supply Voltage



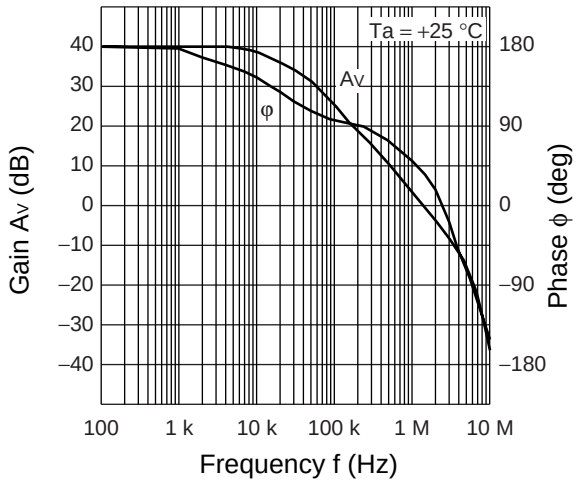
Triangular Wave Oscillation Frequency vs. Ambient Temperature

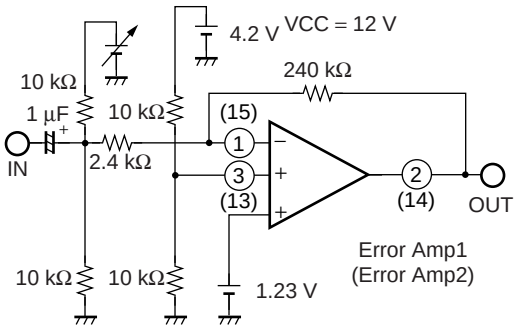


Error Amplifier Threshold Voltage vs. Ambient Temperature



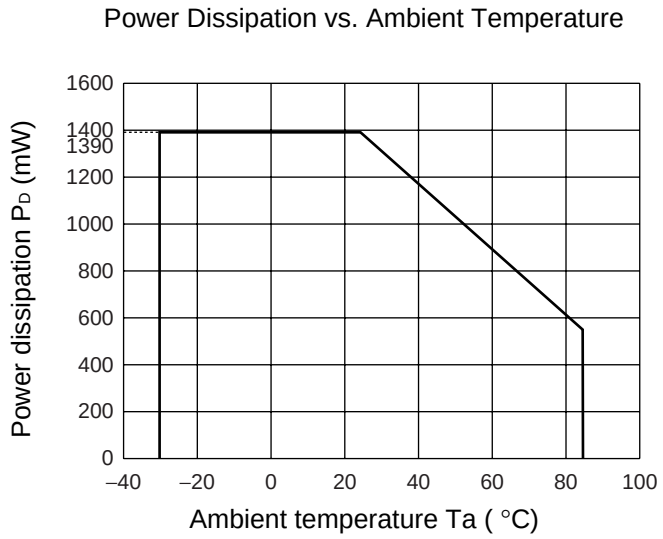
Error Amplifier, Gain, Phase vs. Frequency





(Continued)

(Continued)



■ FUNCTIONS

1. DC/DC Converter Functions

(1) Reference voltage block (Ref)

The reference voltage circuit generates a temperature-compensated reference voltage (typically 3.5 V) using the voltage supplied from the power supply terminal (pin 24) . The voltage is used as the reference voltage for the IC's internal circuitry.

The reference voltage can be used to supply a load current of up to 1 mA to an external device through the VREF terminal (pin 8) .

(2) Triangular-wave oscillator block (OSC)

The triangular waveform oscillator incorporates a timing capacitor connected respectively to the RT terminal (pin 5) to generate triangular oscillation waveforms CT1 (amplitude of 1.8 V to 3.0 V) and CT2 (amplitude of 1.8 V to 3.0 V in antiphase with CT1). The symmetrical-phase system using the two opposite-phase triangular waves reduces the input ripple current, resulting in a smaller input capacitor.

The triangular oscillation waveforms are input to the IC's internal PWM comparator.

(3) Error amplifier block (Error Amp1, Error Amp2)

The error amplifier detects the DC/DC converter output voltage and outputs PWM control signals. By connecting a feedback resistor and capacitor between the output terminal and inverted input terminal, it is possible to create any desired level of loop gain, thereby providing stable phase compensation to the system.

Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor to the CS1 terminal (pin 3) or CS2 terminal (pin 13), the non-inverted input terminal for Error Amp. The use of Error Amp for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load on the DC/ DC converter.

(4) PWM comparator (PWM Comp.) block

The PWM comparator is a voltage-pulse width modulator that controls the output duty depending on the input/output voltage.

Main side : Turns the output transistor on in the intervals in which the error amplifier output voltage is higher than the triangular wave voltage.

Synchronous rectification side : Turns the output transistor on in the intervals in which the error amplifier output voltage is lower than the triangular wave valtage.

(5) Output block

The output circuits on the main side and on the synchronous rectification side are both in the totem pole configuration, capable of driving an external N-ch MOS FET.

In addition, because the output drive ability (700 mA Max : Duty ≤ 5%) is high, the gate – source capacity is large and the FET of low ON resistor can be used.

2. Channel Control Function

Channels, main, VB and PWRGOOD are turned on and off depending on the voltage levels at the CTL terminal (pin 6), CTL1 terminal (pin 9) and CTL2 terminal (pin 10).

Channel On/Off Setting Conditions

CTL	CTL1	CTL2	Power	CH1	CH2	VB	PWRGOOD
L	—*	—*	OFF	OFF	OFF	OFF	OFF
H	L	L	ON	OFF	OFF	ON	ON
H	H	L	ON	ON	OFF	ON	ON
H	L	H	ON	OFF	ON	ON	ON
H	H	H	ON	ON	ON	ON	ON

*: Undefined

3. Protective Functions

(1) Undervoltage lockout protection circuit (UVLO)

The transient state or a momentary drops in supply voltage, which occurs when the power supply is turned on, may cause the control IC to malfunction, resulting in breakdown or degradation of the system. To prevent such malfunctions, the undervoltage lockout protection circuit detects the internal reference voltage level with respect to the power supply voltage, turns off the output transistor, and sets the dead time to 100% while holding the CSCP terminal (pin 11) at the “L” level and setting the PWRGOOD terminal (pin 12) to the “L” level.

The system is restored when the supply voltage reaches the threshold voltage of the undervoltage lockout protection circuit.

(2) Timer-latch overcurrent protection circuit block (OCP)

The timer-latch overcurrent protection circuit is actuated upon completion of the soft-start period. When an overcurrent flows, the circuit detects the increase in the voltage between the main-side FET’s drain and source using the main-side FET ON resistor, actuates the timer circuit, and starts charging the capacitor CSCP connected to the CSCP terminal (pin 11). If the overcurrent remains flowing beyond the predetermined period of time, the circuit sets the latch to turn off the FETs on the main side and synchronous rectification side of each channel while setting the PWRGOOD terminal (pin 12) to the “L” level. The detection current value can be set by resistor RLIM1 connected between the main-side FET’s drain and the ILIM1 terminal (pin 25) and resistor RLIM2 connected between the drain and the ILIM2 terminal (pin 23).

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the “L” level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the “L” level. (See “1. Setting Timer-Latch Overcurrent Protection Detection Current” in ■ ABOUT TIMER-LATCH PROTECTION CIRCUIT.)

(3) Timer-latch short-circuit protection circuit (SCP)

The short-circuit detection comparator (SCP Comp.) provided for the two channels detects the output voltage level and, if the error amplifier output voltage of either channel reaches the short-circuit detection voltage (typically 3.1 V), the timer circuit is actuated to start charging the external capacitor Cscp connected to the CSCP terminal (pin 11).

When the capacitor voltage reaches about 0.7 V, the circuit turns off the output transistor and sets the dead time to 100%.

The PWRGOOD terminal (pin 12) is fixed at the “L” level.

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the “L” level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the “L” level. (See “2. Setting Time Constant for Timer-Latch Short-Circuit Protection Circuit” in ■ ABOUT TIMER-LATCH PROTECTION CIRCUIT.)

(4) Timer-latch overvoltage protection circuit block (OVP)

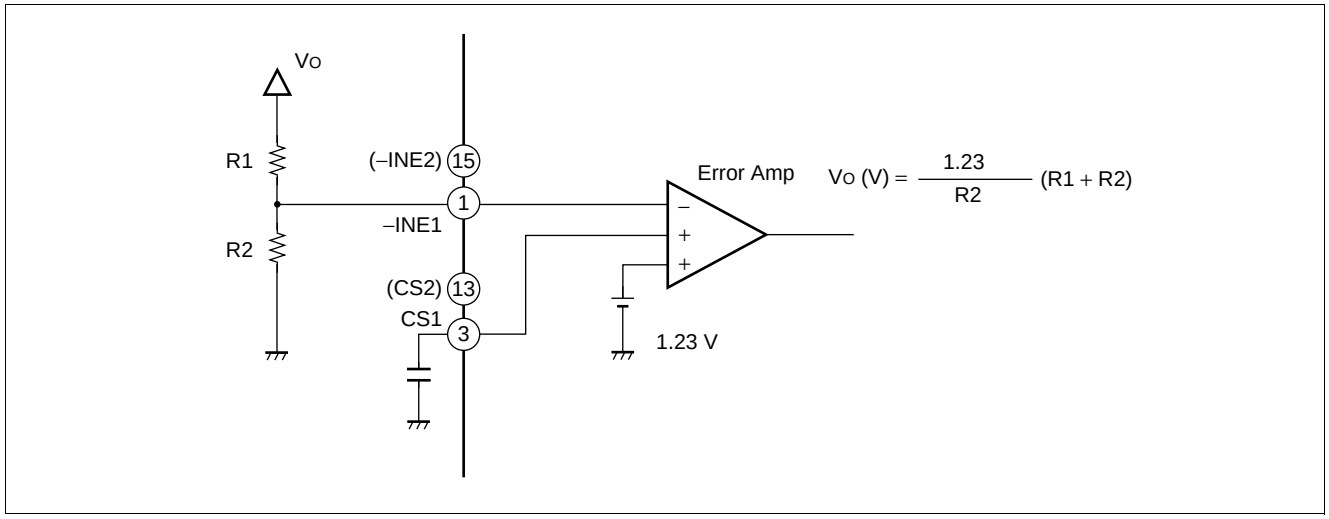
When the overvoltage detection comparator (OVP Comp.) provided for each channel detects the DC-DC converter's output voltage level exceeding its threshold voltage, the timer-latch overvoltage protection circuit actuates the timer circuit and starts charging the capacitor CSCP connected to the CSCP terminal (pin 11). If the overvoltage remains applied beyond the predetermined period of time, the circuit sets the latch to turn off the FET on the main side of each channel while setting the PWRGOOD terminal (pin 12) to the "L" level.

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the "L" level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the "L" level. (See "3. Setting Detection of Timer-Latch Overvoltage Protection Circuit" in ■ ABOUT TIMER-LATCH PROTECTION CIRCUIT.)

(5) Protection status output circuit block (PWRGOOD)

The protection status output circuit outputs the "L" level signal to the PWRGOOD terminal (pin 12) when each protection circuit is actuated.

■ SETTING THE OUTPUT VOLTAGE



< CH1, CH2 >

■ SETTING THE TRIANGULAR OSCILLATION FREQUENCY

The triangular oscillation frequency is determined by the timing capacitor connected to the timing resistor (R_T) connected to the RT terminal (pin 5).

Triangular oscillation frequency: f_{OSC}

$$f_{OSC}\ (kHz) \fallingdotseq \frac{14100}{R_T\ (k\Omega)}$$

■ SETTING THE SOFT-START AND DISCHARGE TIMES

To prevent rush currents when the IC is turned on, you can set a soft-start by connecting soft-start capacitors (C_{S1} and C_{S2}) to the CS1 terminal (pin 3) for channel 1 and the CS2 terminal (pin 13) for channel 2, respectively.

Setting the each control terminals (CTL1 and CTL2) from “L” to “OPEN” switches SW1 and SW2 from B to A to charge the external soft-start capacitors (C_{S1} and C_{S2}) connected to the CS1 and CS2 terminals at 3 μA.

The error amplifier output (FB1 or FB2) is determined by comparison between the lower one of the potentials at two noninverted input terminals (1.23 V, CS terminal voltages) and the inverted input terminal voltage (-INE).

The FB terminal voltage during the soft-start period is therefore determined by comparison between the -INE terminal and CS terminal voltages. The DC/DC converter output voltage rises in proportion to the CS terminal voltage as the soft-start capacitor connected to the CS terminal is charged.

The soft-start time is obtained from the following equation:

Soft-start time: ts (time to output 100%)

$ts\ (s) \fallingdotseq 0.41 \times C_S\ (\mu F)$

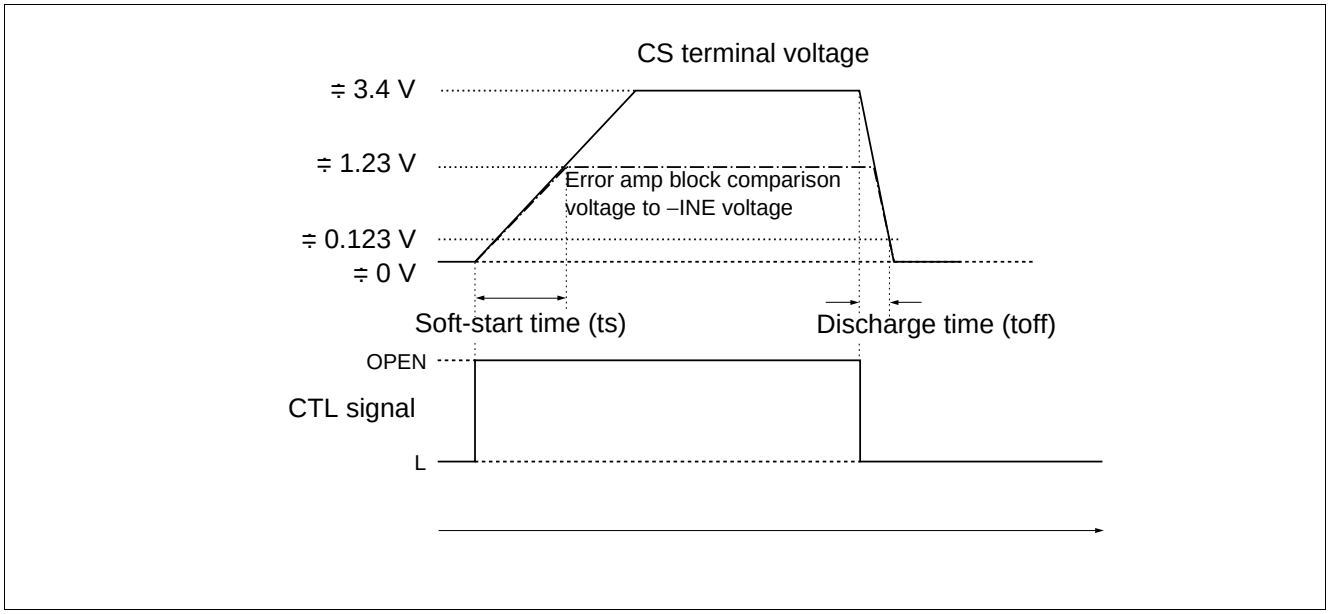
Setting the each control terminals (CTL1 and CTL2) from “OPEN” to “L” switches SW1 and SW2 from A to B.

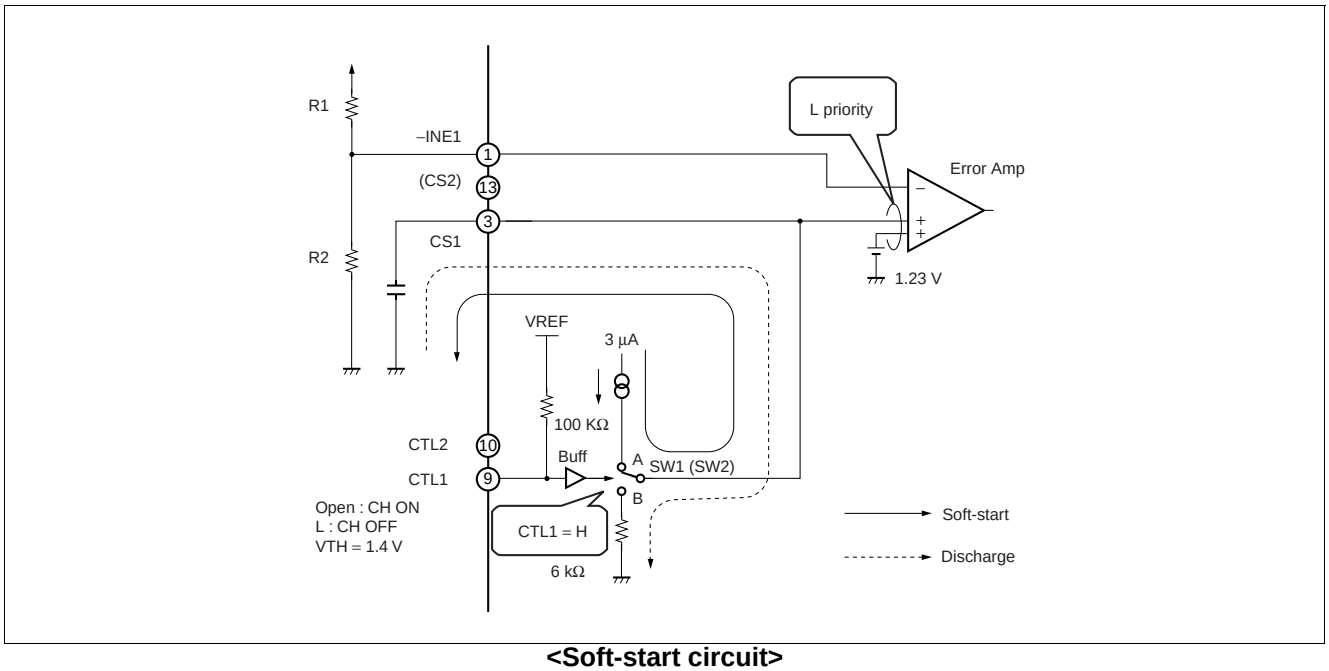
Then the IC discharges the soft-start capacitors (C_{S1} and C_{S2}) charged at about 3.4 V using the internally set discharge resistor (Rs: = 6 kΩ) and lowers the output voltage regardless of the DC/DC converter load current.

The discharge time is obtained from the following equation:

Discharge time: toff (time to output 10%)

$toff\ (s) \fallingdotseq 0.020 \times C_S\ (\mu F)$

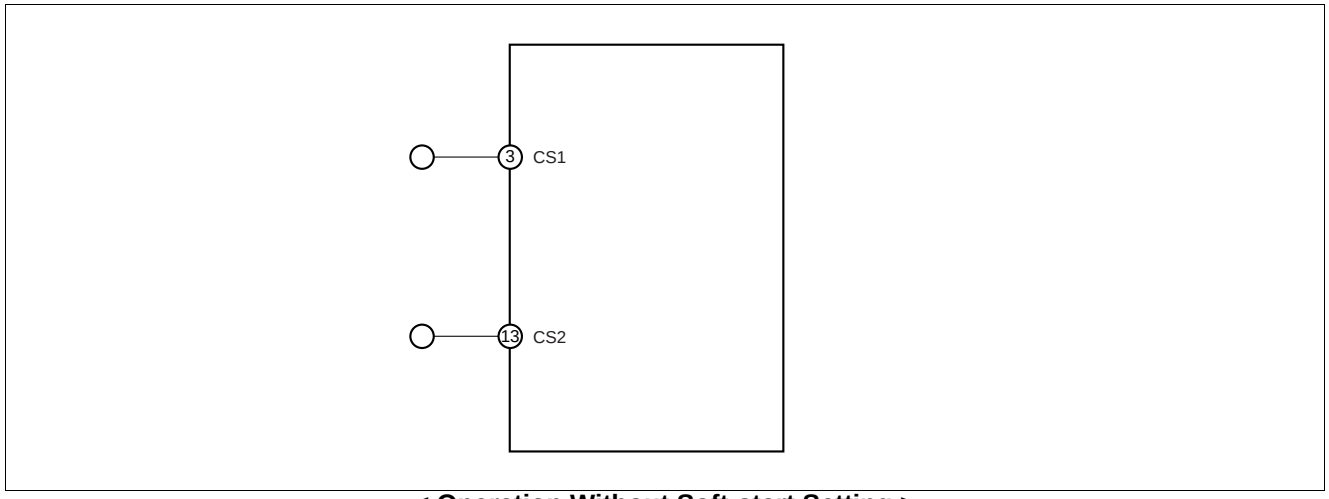




<Soft-start circuit>

■ TREATMENT OF UNUSED CS TERMINALS

When the soft-start function is not used, the CS1 terminal (pin 3) and CS2 terminal (pin 13) should be left open.



< Operation Without Soft-start Setting >

■ ABOUT TIMER-LATCH PROTECTION CIRCUIT

1. Setting Timer-Latch Overcurrent Protection Detection Current

The overcurrent protection circuit is actuated upon completion of the soft-start period. When an overcurrent flows, the circuit detects the increase in the voltage between the main-side FET's drain and source using the main-side FET ON resistor (RON), actuates the timer circuit, and starts charging the capacitor CSCP connected to the CSCP terminal (pin 11). If the overcurrent remains flowing beyond the predetermined period of time, the circuit sets the latch to turn off the FETs on the main side and synchronous rectification side of each channel while setting the PWRGOOD terminal (pin 12) to the "L" level. The detection current value can be set by the resistors (R_{LIM1} and R_{LIM2}) connected between the main-side FET's drain and the ILIM1 terminal (pin 25) and between the drain and the ILIM2 terminal (pin 23), respectively.

The internal current (I_{LIM}) can be set by the timing resistor (R_T) connected to the RT terminal (pin 5).
Time until activating timer circuit and setting latch is equal to short-circuit detection time in "2. Setting Time Constant for Timer-Latch Short-Circuit Protection Circuit".

Internal current value: I_{LIM}

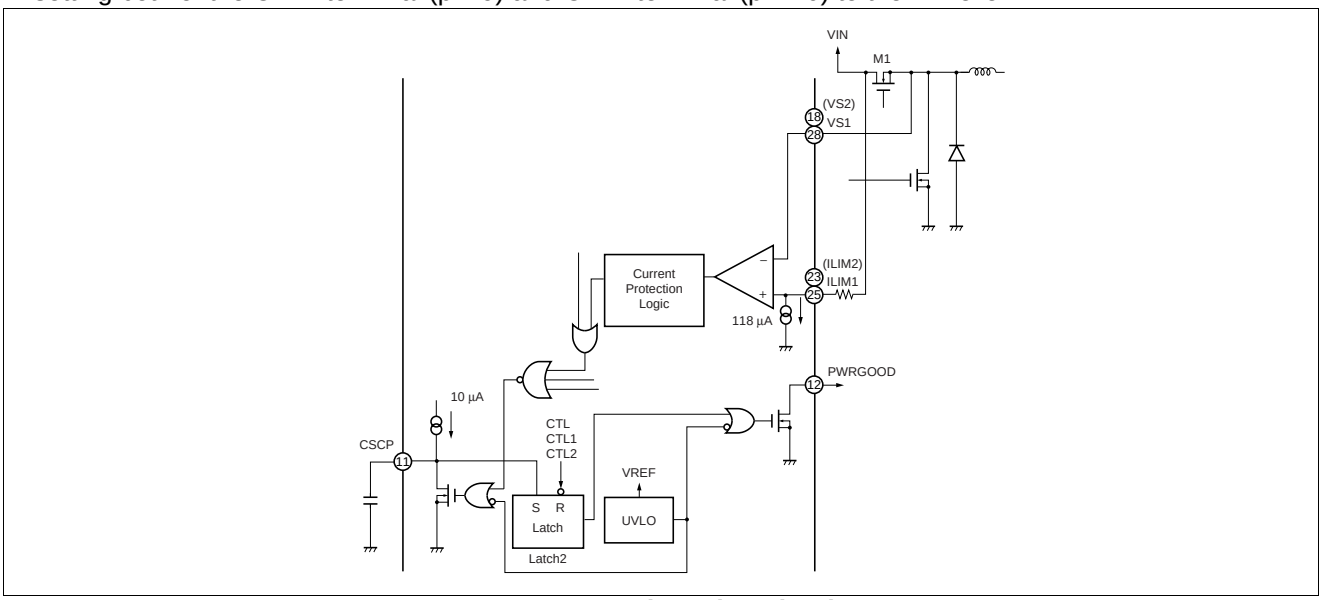
$$I_{LIM}\ (\mu A) \fallingdotseq \frac{5546}{R_T\ (k\Omega)}$$

Detection current value: I_{OCP}

$$I_{OCP}\ (A) \fallingdotseq \frac{I_{LIM}(A) \times R_{LIM}(\Omega)}{R_{ON}\ (\Omega)} - \frac{(Vin(V) - V_O(V)) \times V_O(V)}{2 \times Vin(V) \times f_{OSC}(Hz) \times L(H)}$$

R_{LIM}: Overcurrent detection resistor
R_{ON}: Main-side FET ON resistor
Vin: Input voltage
V_O: DC-DC converter output voltage
f_{OSC}: Oscillation frequency
L: Coil inductance

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the "L" level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the "L" level.



<Overcurrent detection circuit>

2. Setting Time Constant for Timer-Latch Short-Circuit Protection Circuit

Each channel uses the short-circuit detection comparator (SCP Comp.) to always compare the error amplifier's output level to the reference voltage.

While the DC-DC converter load conditions are stable on both channels, the short-circuit detection comparator keeps its output at the "H" level and the CSCP terminal (pin 11) remains at the "L" level.

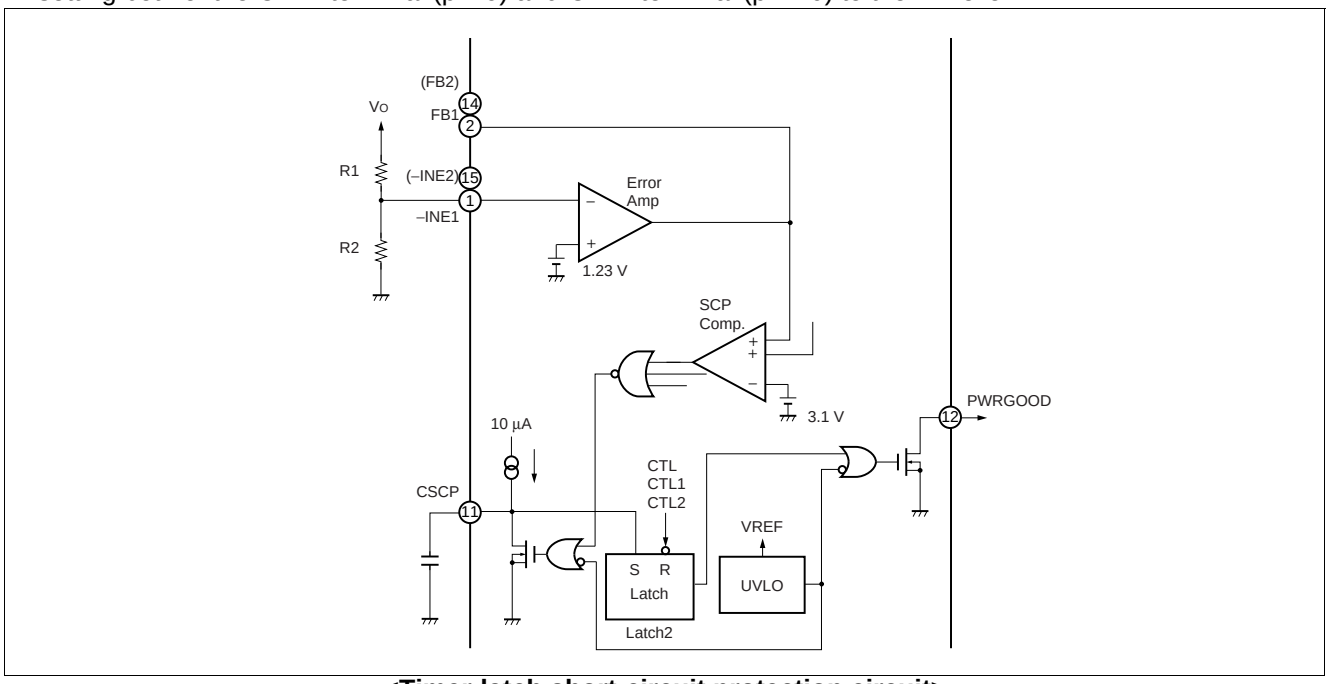
If a load condition changes rapidly due to a short-circuit of the load, causing the output voltage to drop, the short-circuit detection comparator changes its output to the "L" level. This causes the external short-circuit protection capacitor Cscp connected to the CSCP terminal to be charged at 10 µA.

Short-circuit detection time (t_{SCP})

t_{SCP} (s) ≒ 0.070 × C_{SCP} (µF)

When capacitor Cscp is charged to the threshold voltage (VTH ≒ 0.70 V), the protection circuit sets the latch and turns off the external FET (setting the dead time to 100%). At this time, the latch input is closed and the CSCP terminal is held at the "L" level. The protection circuit closes both channels even when a short-circuit is detected on only either.

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the "L" level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the "L" level.



<Timer-latch short-circuit protection circuit>

3. Setting Overvoltage Detection by the Timer-Latch Overvoltage Protection Circuit

An overvoltage output from the DC-DC converter can be detected by connecting external resistors from the DC-DC converter output to the noninverted input terminal (-INE1 terminal (pin 1) and -INE2 terminal (pin 15)) of the overvoltage comparators (OVP Comp. 1 and 2).

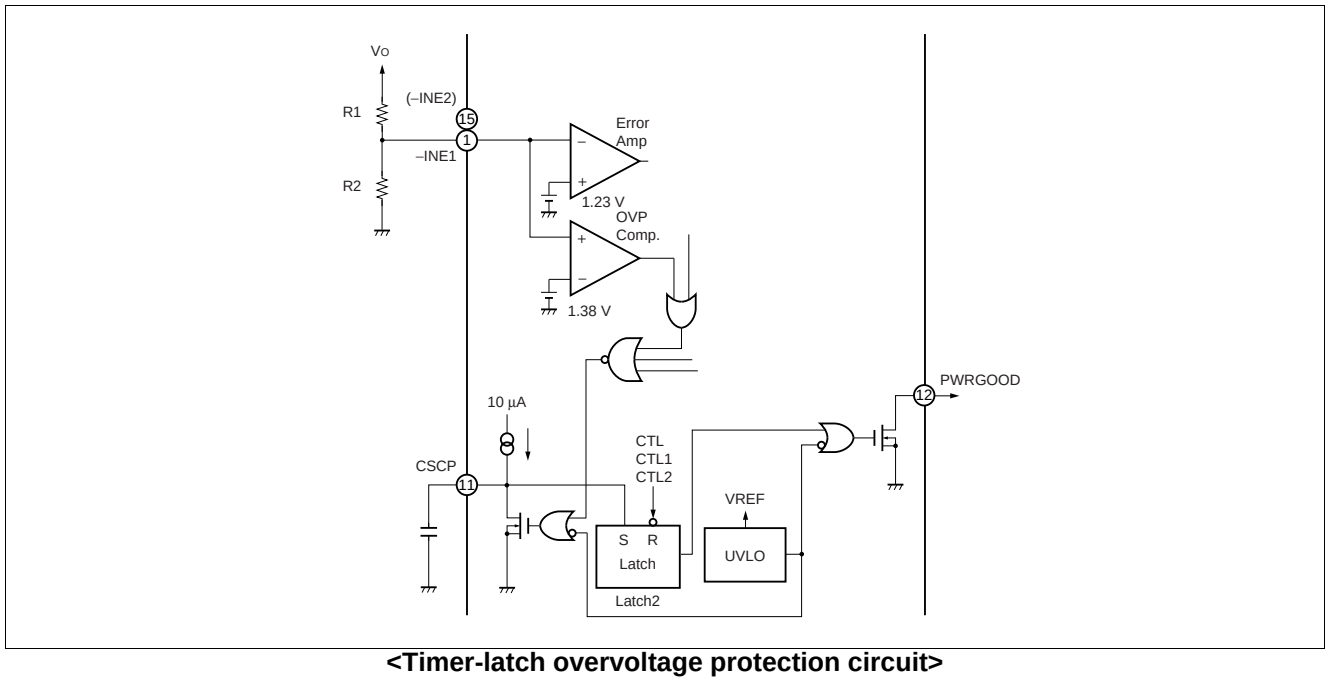
When the DC-DC converter output voltage exceeds the overvoltage detection level, the output of the overvoltage comparator (OVP Comp. 1, 2) becomes the “H” level and the overvoltage protection circuit actuates the timer circuit to start charging the external capacitor Cscp connected to the CSCP terminal (pin 11). If the overvoltage remains applied beyond setting time, the circuit sets the latch to turn off the FET on the main side of each channel while setting the PWRGOOD terminal (pin 12) to the “L” level. The protection circuit closes both channels even when an overvoltage is detected on only either.

Note that the time from the actuation of the timer circuit until the latch is set is equal to the short-circuit detection time defined in “2. Setting Time Constant for Timer-Latch Short-Circuit Protection Circuit”.

Overvoltage detection voltage : V_{OVP}

$$V_{OVP}\ (V) \fallingdotseq 1.38 \times (R1\ (\Omega) + R2\ (\Omega)) / R2\ (\Omega) \fallingdotseq 1.12 \times V_O$$

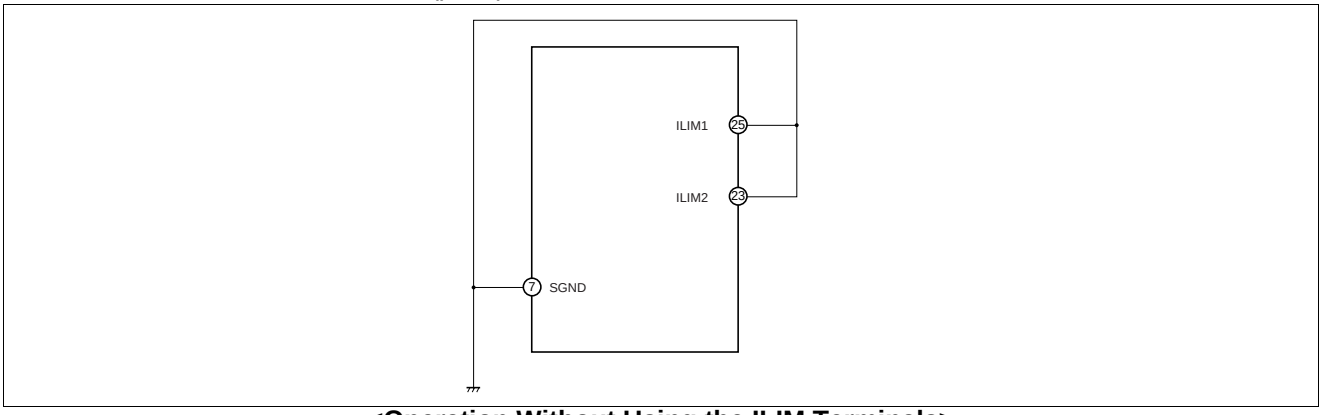
To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the "L" level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the "L" level.



<Timer-latch overvoltage protection circuit>

■ TREATMENT OF UNUSED ILIM TERMINALS

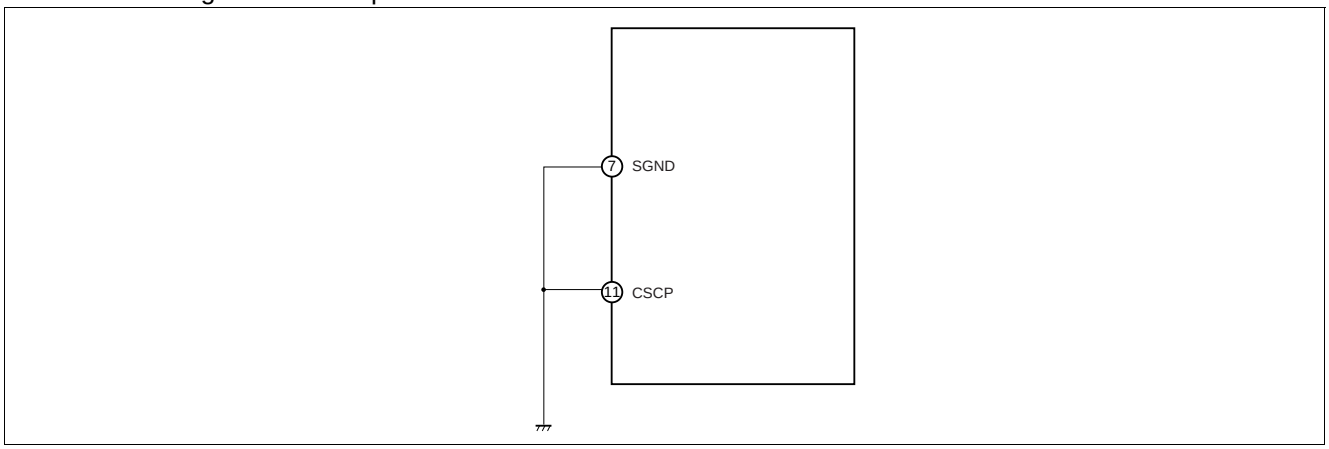
When the overcurrent protection circuit is not used, the ILIM1 terminal (pin 25) and ILIM2 terminal (pin 23) should be shorted to the SGND terminal (pin 6) .



<Operation Without Using the ILIM Terminals>

■ PROCESSING WITHOUT USING THE CSCP TERMINAL

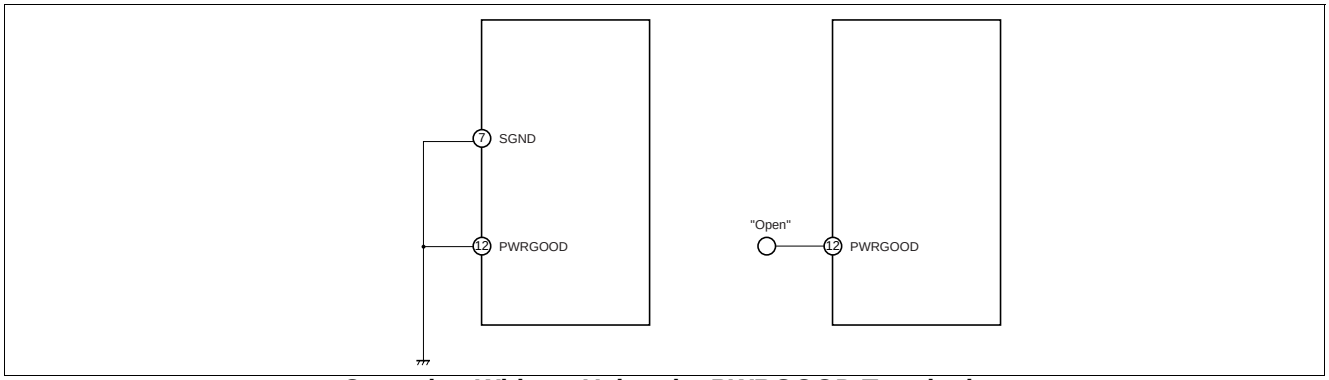
When the timer-latch short-circuit protection circuit is not used, the CSCP terminal (pin 11) should be shorted to SGND using the shortest possible connection.



<Operation Without Using the CSCP Terminals>

■ TREATMENT OF UNUSED PWRGOOD TERMINALS

When the PWRGOOD terminal is not used, the PWRGOOD terminal (pin 12) should be shorted or open to the SGND terminal.



<Operation Without Using the PWRGOOD Terminals>

■ OUTPUT STATES DURING PROTECTION CIRCUIT OPERATION

The table below lists the output states with each protection circuits actuated.

Protection circuit / Output terminal		CH1		CH2		PWRGOOD
		OUT1-1	OUT2-1	OUT1-2	OUT2-2	
Overcurrent protection circuit	CH1	L	L	L	L	L
	CH2	L	L	L	L	L
Short-circuit protection	CH1	L	L	L	L	L
	CH2	L	L	L	L	L
Overvoltage protection circuit	CH1	L	H	L	H	L
	CH2	L	H	L	H	L
Under voltage lockout protection circuit		L	L	L	L	L

■ RESETTING THE LATCH OF EACH PROTECTION CIRCUIT

When the overvoltage, overcurrent, or short-circuit protection circuit detects each abnormality, it sets the latch to fix the output at the "L" level. The PWRGOOD terminal (pin 12) is fixed at the "L" level upon abnormality detection by each protection circuit.

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the "L" level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the "L" level.

■ NOTE ON IC'S INTERNAL POWER CONSUMPTION

The oscillation frequency of an IC and the total gate charge of FETs largely affects the internal dissipation of the IC.

Pay attention to the following point with respect to the internal power consumption of the IC when applications are used.

I_B (mean current) is obtained from the following equation, assuming Qg1 and Qg2 as the total gate charges applied to the gate capacitors ($Ciss_1$, $Ciss_2$, $Crss_1$, $Crss_2$) of external FETs Q1 and Q2.

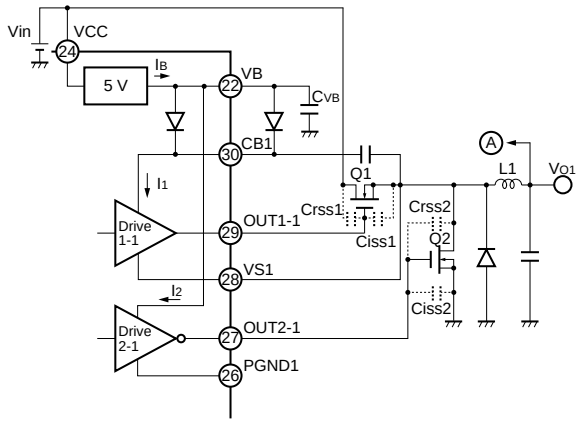
Current per channel

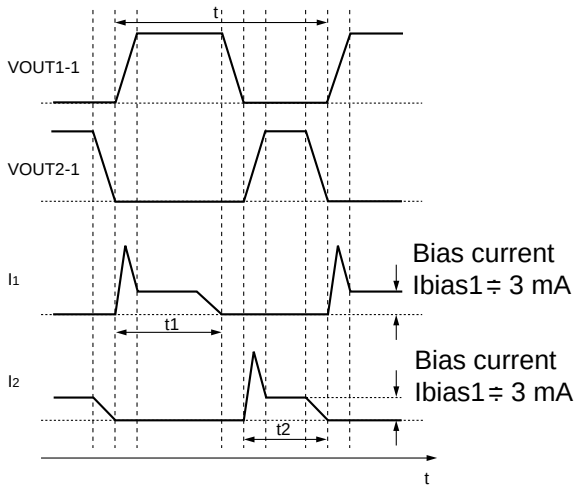
$$I_B\ (A) = I_1 + I_2$$

As the current consumption by the IC, excluding I_B, is about 15 mA, the power consumption is obtained from the following equation :

Power consumption : Pc

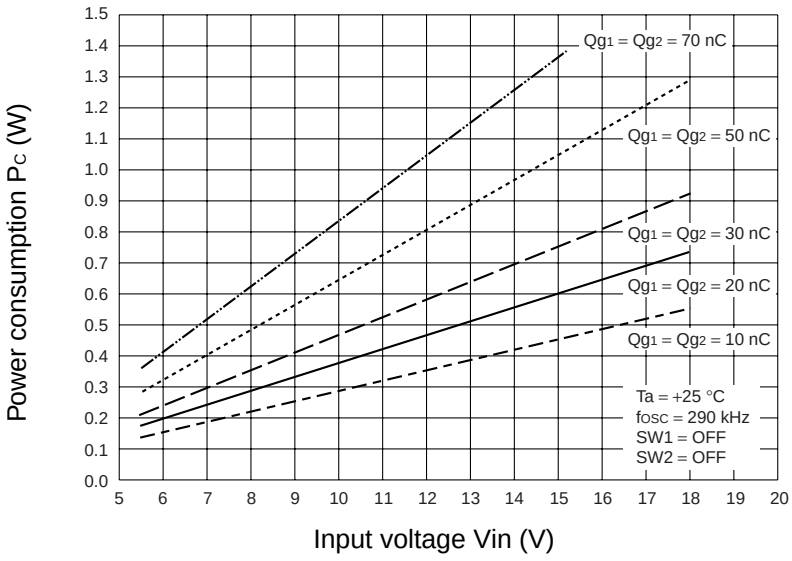
$$Pc\ (W) = 0.015 \times V_{CC}\ (V) + 2 \times V_{CC}\ (V) \bullet I_B\ (A) - V_B\ (V) \bullet I_B\ (A)$$



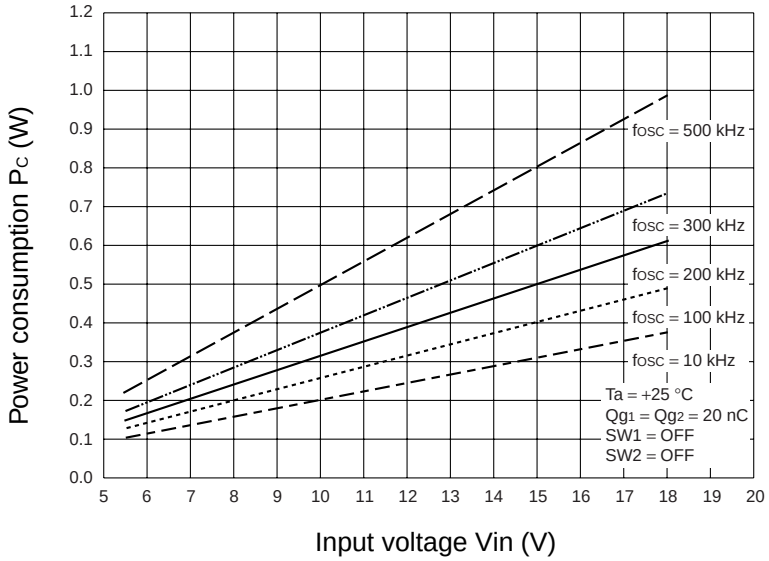


See "Power Consumption vs. Input Voltage" on the next page as a reference and use the above method of obtaining the power consumption to design your application of the IC taking account of the "Power Dissipation vs. Ambient Temperature" characteristic in the "TYPICAL CHARACTERISTICS" section.

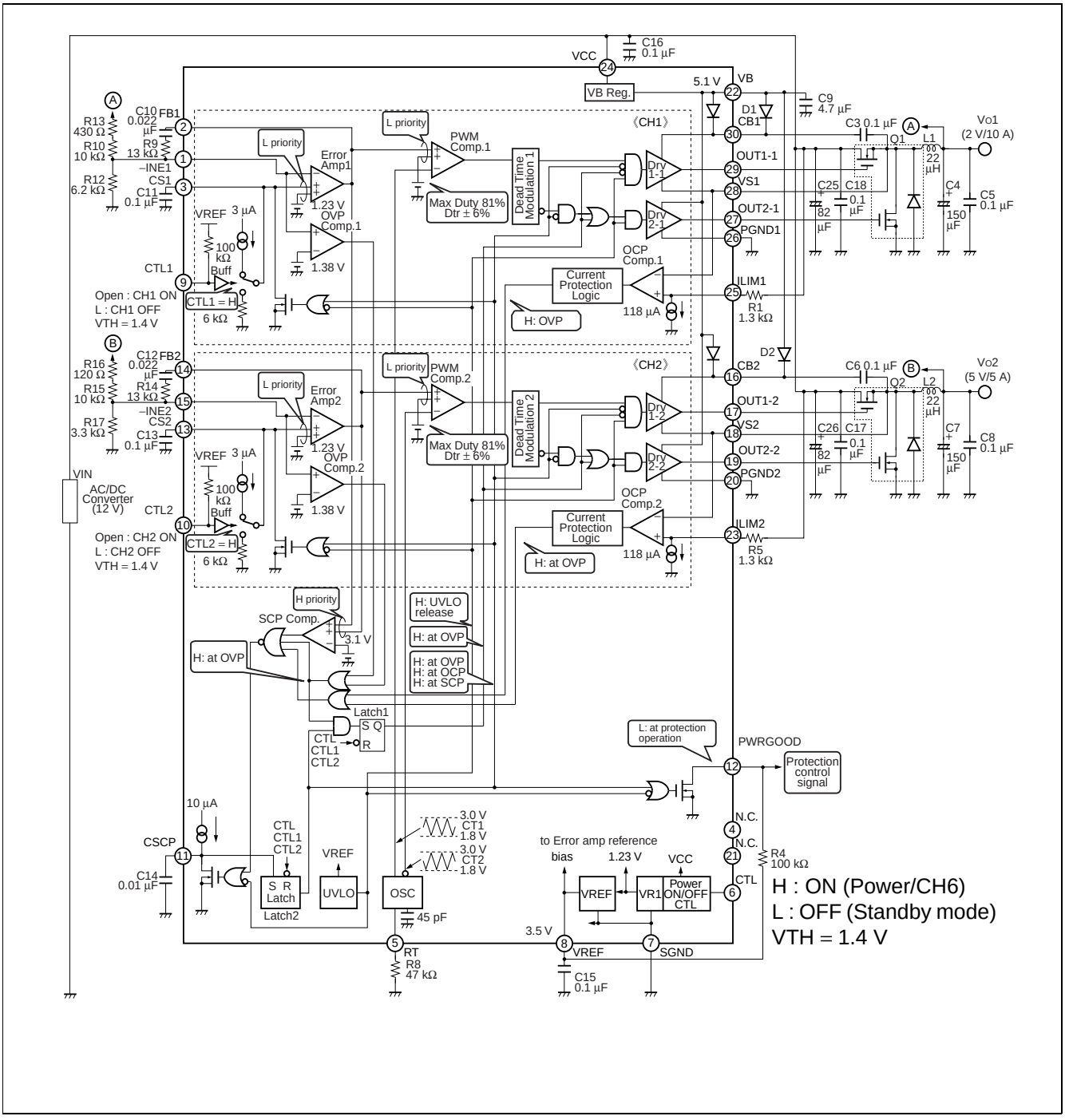
Power Consumption vs. Input Voltage (Qg Parameter)



Power Consumption vs. Input Voltage (f_{OSC} Parameter)



■ SAMPLE CIRCUIT



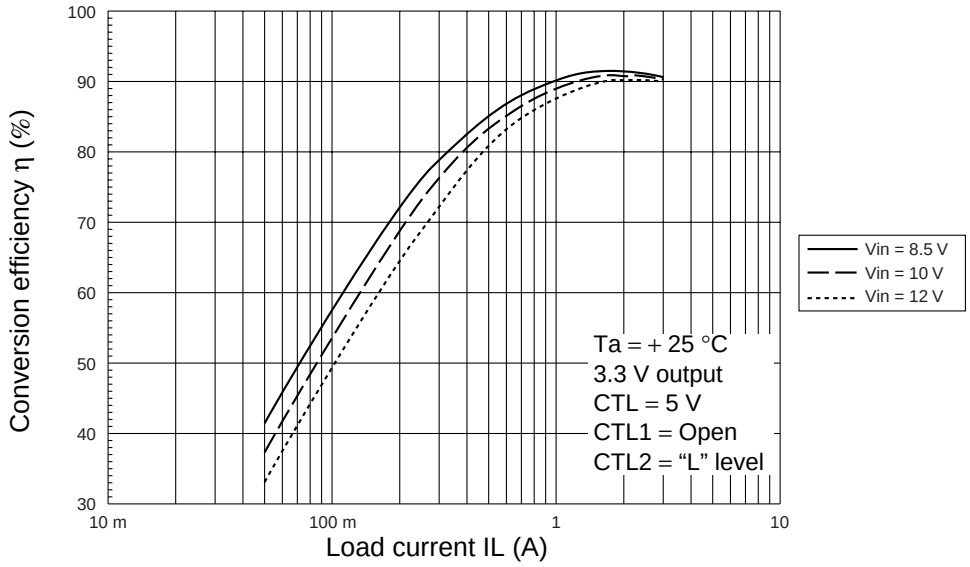
■ PARTS LIST

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS NO.
Q1, Q2	Dual FETKY™	Main sides: VDS = 30 V, Qg = 9.9 nC (Max) Synchronous sides: VDS = 30 V, Qg = 20.7 nC (Max) SBD: VF = 0.52 V (Max) at IF = 1 A		IR	IRF7901D1
D1, D2	Diode	VF = 0.3 V (Max) , at IF = 10 mA		ROHM	RB495D
L1, L2	Coil	22 µH	3.5 A, 31.6 mΩ	TDK	SLF12565T-220M3R5
C3, C6	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C4	OS-CON™	150 µF	6.3 V	SANYO	6SVP150M
C5, C8	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C7	OS-CON™	150 µF	6.3 V	SANYO	6SVP150M
C9	Ceramics Condenser	4.7 µF	10 V	TDK	C3216JB1A475M
C10	Ceramics Condenser	0.022 µF	50 V	TDK	C1608JB1H223K
C11, C13	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C12	Ceramics Condenser	0.022 µF	50 V	TDK	C1608JB1H223K
C14	Ceramics Condenser	0.01 µF	50 V	TDK	C1608JB1H103K
C15, C16	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C17, C18	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C25, C26	OS-CON™	82 µF	16 V	SANYO	16SVP82M
R1, R5	Resistor	1.3 Ω	0.5 %	SUSUMU	RR0816P132D
R4	Resistor	100 Ω	0.5 %	SUSUMU	RR0816P104D
R8	Resistor	47 kΩ	0.5 %	SUSUMU	RR0816P473D
R9	Resistor	13 kΩ	0.5 %	SUSUMU	RR0816P133D
R10	Resistor	10 kΩ	0.5 %	SUSUMU	RR0816P103D
R12	Resistor	6.2 kΩ	0.5 %	SUSUMU	RR0816P622D
R13	Resistor	430 Ω	0.5 %	SUSUMU	RR0816P431D
R14	Resistor	13 kΩ	0.5 %	SUSUMU	RR0816P133D
R15	Resistor	10 kΩ	0.5 %	SUSUMU	RR0816P103D
R16	Resistor	120 Ω	0.5 %	SUSUMU	RR0816P121D
R17	Resistor	3.3 kΩ	0.5 %	SUSUMU	RR0816P332D

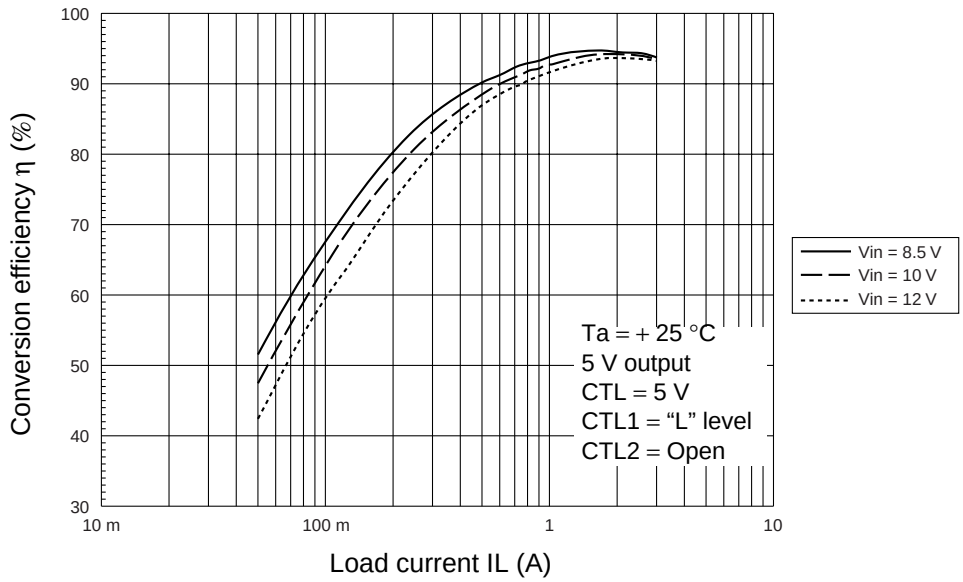
Note : IR : International Rectifier Corp.
ROHM : ROHM Co., Ltd.
TDK : TDK Corporation
SANYO : SANYO Electric Co., Ltd.
SUSUMU : SUSUMU Electronics Corp.
Dual FETKY is a trademark of International Rectifier Corp.
OS-CON is a trademark of SANYO Electric Co., Ltd.

■ REFERENCE DATA

Conversion Efficiency vs. Load Current (CH1)

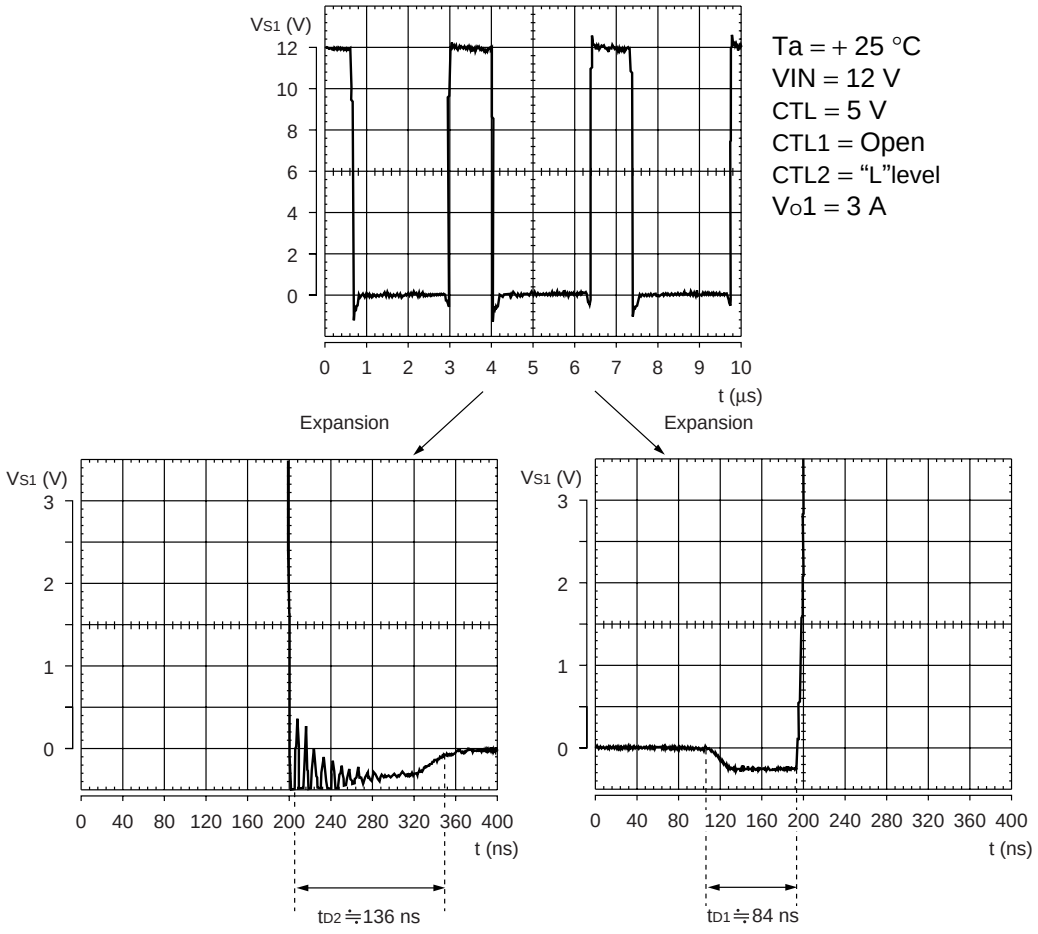


Conversion Efficiency vs. Load Current (CH2)



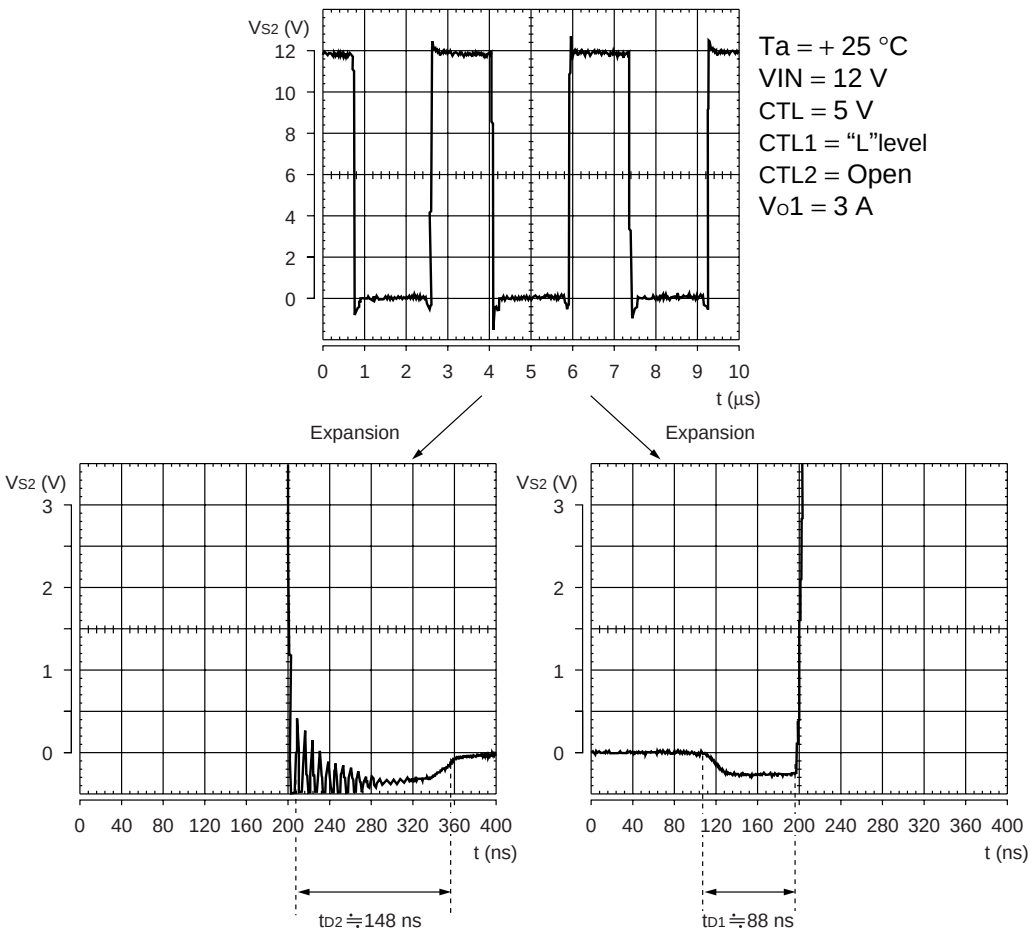
(Continued)

Switching Waveform (CH1)



(Continued)

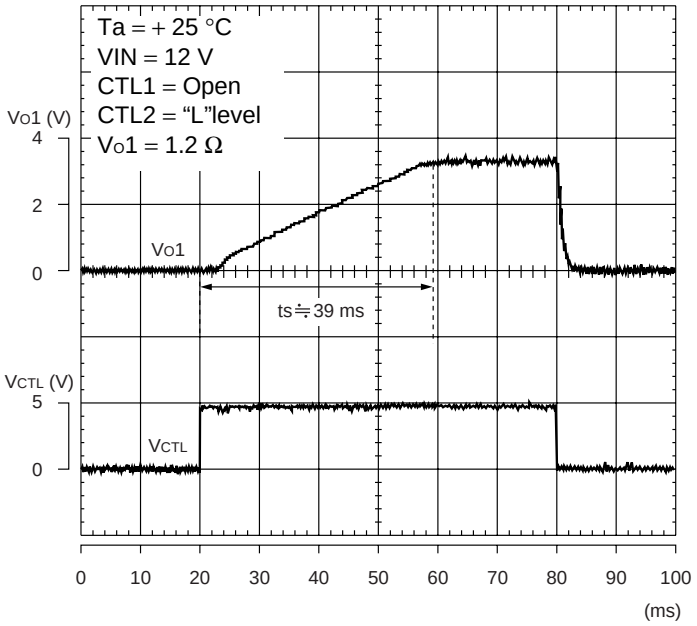
Switching Waveform (CH2)



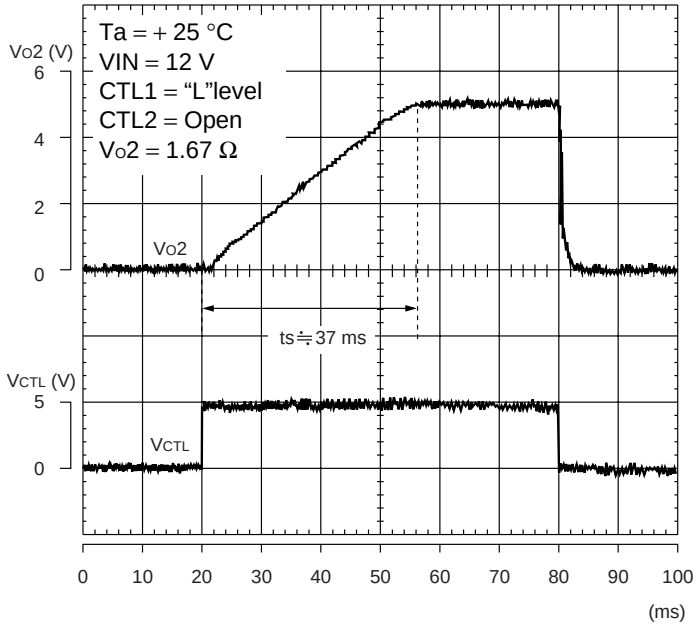
(Continued)

(Continued)

Soft-start Operating Waveform (CH1)



Soft-start Operating Waveform (CH2)



■ NOTES ON USE

- Take account of common impedance when designing the earth line on a printed wiring board.

- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools, and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.

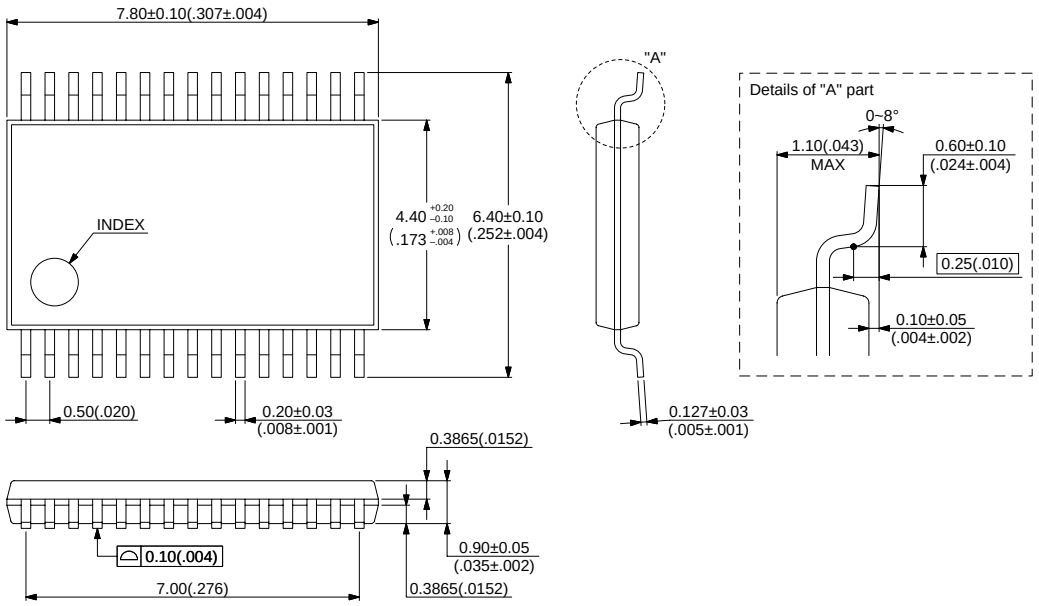
- Do not apply a negative voltage.
  - Applying a negative voltage of −0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB3889PFT	30-pin plastic TSSOP (FPT-30P-M04)	

■ PACKAGE DIMENSION

30-pin plastic TSSOP
(FPT-30P-M04)



Dimensions in mm (inches)

FUJITSU LIMITED

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0209