Dual-Channel, 10-/12-/14-Bit, 500 MSPS Digital-to-Analog Converters (DACs)

Check for Samples: DAC3152, DAC3162, DAC3172

FEATURES

- Low Power: 300 mW at 500 MSPS
- LVDS Input Data Bus
  - Interleaved DDR Data Load
- High DC Accuracy: ±1 LSB DNL, ±2 LSB INL
- Low Latency: 1.5 Clock Cycles
- Simple Control: No Software Required
- Differential Scalable Output: 2 mA to 20 mA
- On-Chip 1.2-V Reference
- 1.8-V and 3.3-V DC Supplies
- Space Saving Package: 48-pin 7-mm × 7-mm QFN

APPLICATIONS

- Cellular Base Stations
- Wideband Communications
- Medical Instrumentation
- Test and Measurement

DESCRIPTION

The DAC3152/DAC3162/DAC3172 is a low-power, low-latency, high-dynamic-range, dual-channel, 10-/12-/14-bit, pin-compatible family of digital-to-analog converters (DACs) with a sample rate as high as 500 MSPS.

The device simplicity (no software required), low latency, and low power simplify the design of complex systems. The DACs interface seamlessly with the high-performance TRF3703-33 analog quadrature modulator for direct upconversion architectures.

Digital data for both DAC channels is interleaved through a single LVDS data bus with on-chip termination. The high input rate of the devices allows the processing of wide-bandwidth signals.

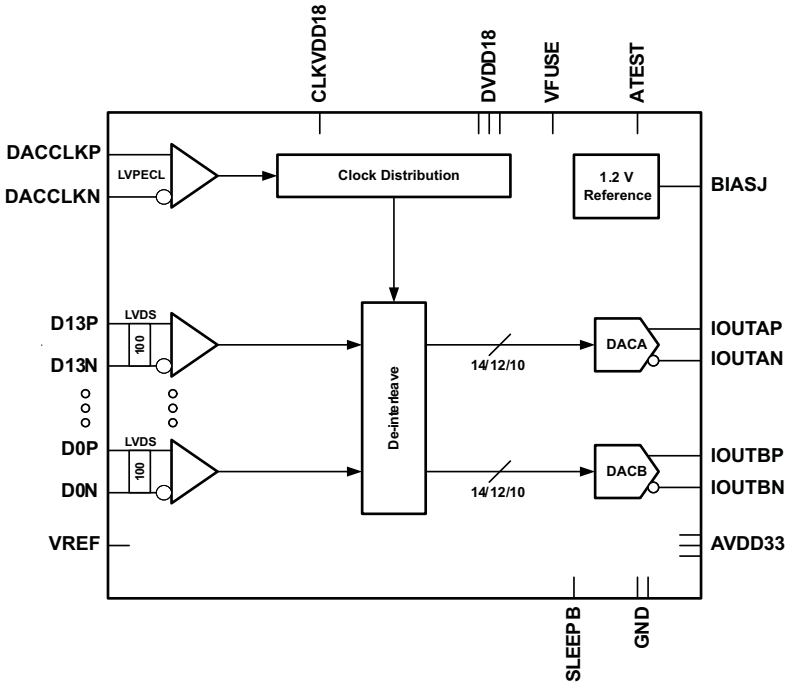
The devices are characterized for operation over the entire industrial temperature range of –40°C to 85°C and are available in a pin-compatible, small 48-pin 7-mm ×7-mm QFN package.

The low power, small size, speed, superior crosstalk, simplicity, and low latency of the DAC3152/DAC3162/DAC3172 make them an attractive fit for a variety of applications.

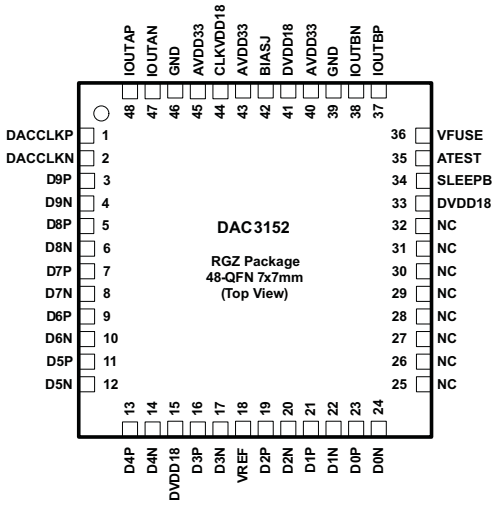
PRODUCT PREVIEW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



DAC3152 PINOUT AND PIN FUNCTIONS

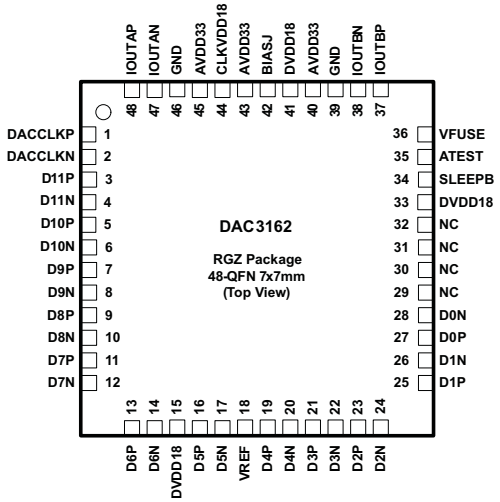


PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD33	40, 43, 45	I	Analog supply voltage (3.3 V)
ATEST	35	O	Factory use only. **Leave unconnected for normal operation.**
BIASJ	42	O	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.
CLKVDD18	44	I	Internal clock buffer supply voltage (1.8 V) This supply can be shared with DIGVDD18.
D[9..0]P	3, 5, 7, 9, 11, 13, 16, 19, 21, 23	I	LVDS positive input data bits 0 through 9. Each positive/negative LVDS pair has an internal 100-Ω termination resistor. Data format relative to DACCLKP/N clock is double data rate (DDR) with two data transfers per DACCLKP/N clock cycle. Dual-channel data is interleaved on this bus. D9P is most-significant data bit (MSB) – pin 3 D0P is least-significant data bit (LSB) – pin 23
D[9..0]N	4, 6, 8, 10, 12, 14, 17, 20, 22, 24	I	LVDS negative input data bits 0 through 9. (See D[9:0]P description above) D9N is most-significant data bit (MSB) – pin 4 D0N is least-significant data bit (LSB) – pin 24
DACCLKP	1	I	Positive external LVPECL clock input with a self-bias of approximately CLKVDD18/2. Input data is latched on both edges of DACCLKP/N (double data rate).
DACCLKN	2	I	Complementary external LVPECL clock input (see the DACCLKP description)
DVDD18	15, 33, 41	I	Digital supply voltage (1.8 V). This supply can be shared with CLKVDD18.
GND	39, 46, Thermal pad	I	Pins 39 and 46 and the thermal pad located on the bottom of the QFN package are ground for all supplies.
IOUTAP	48	O	A-channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full-scale current sink and the least-positive voltage on the IOUTAP pin. Similarly, a 0xFFFF data input results in a 0-mA current sink and the most-positive voltage on the IOUTAP pin.
IOUTAN	47	O	A-channel DAC complementary current output. IOUTAN has the opposite behavior of the IOUTAP described above. An input data value of 0x0000 results in a 0-mA sink and the most-positive voltage on the IOUTAN pin.
IOUTBP	37	O	B-channel DAC current output. See the IOUTAP description above.
IOUTBN	38	O	B-channel DAC complementary current output. See the IOUTAN description above.
NC	25–32	–	No connect. Leave unconnected for normal operation.
SLEEPB	34	I	Connect to GND to put the device in sleep mode or to AVDD for active mode. Internal pullup
VFUSE	36	I	Digital supply voltage (1.8 V). This supply pin is also used for factory fuse programming. **Connect to DVDD18 pins for normal operation.**
VREF	18	I/O	Factory use only. **For normal operation, connect to a 0.1-μF decoupling capacitor to GND.**

PRODUCT PREVIEW

DAC3162 PINOUT AND PIN FUNCTIONS

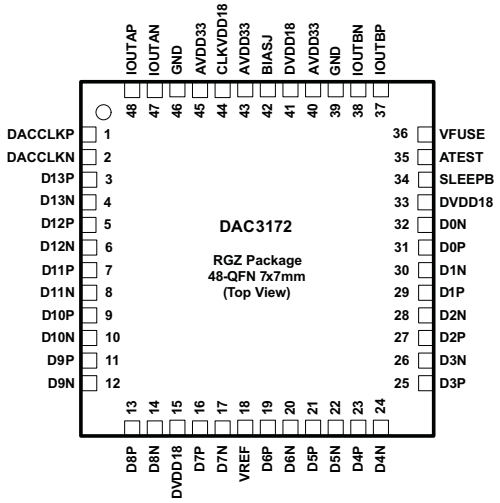


PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD33	40, 43, 45	I	Analog supply voltage (3.3 V)
ATEST	35	O	Factory use only. **Leave unconnected for normal operation.**
BIASJ	42	O	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.
CLKVDD18	44	I	Internal clock buffer supply voltage (1.8 V) This supply can be shared with DIGVDD18.
D[11..0]P	3, 5, 7, 9, 11, 13, 16, 19, 21, 23, 25, 27	I	LVDS positive input data bits 0 through 11. Each positive/negative LVDS pair has an internal 100 Ω termination resistor. Data format relative to DACCLKP/N clock is double data rate (DDR) with two data transfers per DACCLKP/N clock cycle. Dual channel data is interleaved on this bus. D11P is most-significant data bit (MSB) – pin 3 D0P is least-significant data bit (LSB) – pin 23
D[11..0]N	4, 6, 8, 10, 12, 14, 17, 20, 22, 24, 26, 28	I	LVDS negative input data bits 0 through 11. (See D[11:0]P description above) D11N is most-significant data bit (MSB) – pin 4 D0N is least-significant data bit (LSB) – pin 24
DACCLKP	1	I	Positive external LVPECL clock input with a self-bias of approximately CLKVDD18/2. Input data is latched on both edges of DACCLKP/N (double data rate).
DACCLKN	2	I	Complementary external LVPECL clock input (see the DACCLKP description)
DVDD18	15, 33, 41	I	Digital supply voltage (1.8 V) This supply can be shared with CLKVDD18.
GND	39, 46, Thermal pad	I	Pins 39, 46 and the thermal pad located on the bottom of the QFN package are ground for all supplies.
IOUTAP	48	O	A-channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full-scale current sink and the least-positive voltage on the IOUTAP pin. Similarly, a 0xFFFF data input results in a 0-mA current sink and the most-positive voltage on the IOUTAP pin.
IOUTAN	47	O	A-channel DAC complementary current output. IOUTAN has the opposite behavior of the IOUTAP described above. An input data value of 0x0000 results in a 0 mA sink and the most positive voltage on the IOUTAN pin.
IOUTBP	37	O	B-channel DAC current output. See the IOUTAP description above.
IOUTBN	38	O	B-channel DAC complementary current output. See the IOUTAN description above.
NC	25-32	-	No connect. Leave unconnected for normal operation.
SLEEPB	34	I	Connect to GND to put the device in sleep mode or to AVDD for active mode. Internal pullup.
VFUSE	36	I	Digital supply voltage (1.8V). This supply pin is also used for factory fuse programming. **Connect to DVDD18 pins for normal operation.**
VREF	18	I/O	Factory use only. **For normal operation, connect to a 0.1-μF decoupling capacitor to GND.**

PRODUCT PREVIEW

DAC3172 PINOUT AND PIN FUNCTIONS



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD33	40, 43, 45	I	Analog supply voltage (3.3 V)
ATEST	35	O	Factory use only. **Leave unconnected for normal operation.**
BIASJ	42	O	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.
CLKVDD18	44	I	Internal clock buffer supply voltage (1.8 V) This supply can be shared with DIGVDD18.
D[13..0]P	3, 5, 7, 9, 11, 13, 16, 19, 21, 23, 25, 27, 29, 31	I	LVDS positive input data bits 0 through 13. Each positive/negative LVDS pair has an internal 100 Ω termination resistor. Data format relative to DACCLKP/N clock is double data rate (DDR) with two data transfers per DACCLKP/N clock cycle. Dual channel data is interleaved on this bus. D13P is most-significant data bit (MSB) – pin 3 D0P is least-significant data bit (LSB) – pin 23
D[13..0]N	4, 6, 8, 10, 12, 14, 17, 20, 22, 24, 26, 28, 30, 32	I	LVDS negative input data bits 0 through 13. (See D[13:0]P description above) D13N is most-significant data bit (MSB) – pin 4 D0N is least-significant data bit (LSB) – pin 24
DACCLKP	1	I	Positive external LVPECL clock input with a self-bias of approximately CLKVDD18/2. Input data is latched on both edges of DACCLKP/N (Double Data Rate).
DACCLKN	2	I	Complementary external LVPECL clock input (see the DACCLKP description)
DVDD18	15, 33, 41	I	Digital supply voltage (1.8 V) This supply can be shared with CLKVDD18.
GND	39, 46, Thermal pad	I	Pins 39 and 46 and the thermal pad located on the bottom of the QFN package are ground for all supplies.
IOUTAP	48	O	A-channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full-scale current sink and the least-positive voltage on the IOUTAP pin. Similarly, a 0xFFFF data input results in a 0-mA current sink and the most-positive voltage on the IOUTAP pin.
IOUTAN	47	O	A-channel DAC complementary current output. IOUTAN has the opposite behavior of the IOUTAP described above. An input data value of 0x0000 results in a 0-mA sink and the most-positive voltage on the IOUTAN pin.
IOUTBP	37	O	B-channel DAC current output. See the IOUTAP description above.
IOUTBN	38	O	B-channel DAC complementary current output. See the IOUTAN description above.
NC	25-32	-	No connect. Leave unconnected for normal operation.
SLEEPB	34	I	Connect to GND to put the device in sleep mode or to AVDD for active mode. Internal pullup.
VFUSE	36	I	Digital supply voltage (1.8V). This supply pin is also used for factory fuse programming. **Connect to DVDD18 pins for normal operation.**
VREF	18	I/O	Factory use only. **For normal operation, connect to a 0.1-μF decoupling capacitor to GND.**

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE		UNIT
		MIN	MAX	
Supply-voltage range(2)	DVDD18, CLKVDD18	–0.5	1.5	V
	VFUSE	–0.5	1.5	V
	AVDD33	–0.5	4	V
Pin-voltage range(2)	D[13..0]P/N	–0.5	DVDD18 + 0.5	V
	DACCLKP/N	–0.5	CLKVDD18 + 0.5 V	V
	BIASJ, SLEEPB	–0.5	AVDD33 + 0.7 V	V
	IOUTAP/N, IOUTBP/N	–1	AVDD33 + 0.7 V	V
Peak input current (any input)			20	mA
Peak total input current (all inputs)			–30	mA
Operating free-air temperature range, T_A		–40	85	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to GND

THERMAL INFORMATION

THERMAL METRIC(1)		DAC3152	DAC3162	DAC3172	UNITS
		RGZ (48 PINS)	RGZ (48 PINS)	RGZ (48 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	TBD	TBD	TBD	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance				
θ_{JB}	Junction-to-board thermal resistance				
ψ_{JT}	Junction-to-top characterization parameter				
ψ_{JB}	Junction-to-board characterization parameter				
θ_{JCbot}	Junction-to-case (bottom) thermal resistance				

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS – DC SPECIFICTIONS

over recommended operating free-air temperature range, nominal supplies, $IOUT_{FS}$ = 20 mA (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	DAC3152			DAC3162			DAC3172			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			10			12			14			Bits
DC ACCURACY												
DNL	Differential nonlinearity			±0.1			±0.25			±0.5		LSB
INL	Integral nonlinearity			±0.25			±0.5			±1		LSB
ANALOG OUTPUT												
	Coarse-gain linearity			±0.04			±0.04			±0.04		LSB
	Offset error	Mid code offset		±0.001			±0.001			±0.001		%FSR
	Gain error			±2			±2			±2		%FSR
	Gain mismatch			±2			±2			±2		%FSR
	Full-scale output current		2		20	2		20	2		20	mA
	Output compliance range		AVDD – 0.5		AVDD + 0.5	AVDD – 0.5		AVDD + 0.5	AVDD – 0.5		AVDD + 0.5	V
	Output resistance			300			300			300		kΩ
	Output capacitance			5			5			5		pF
REFERENCE												
V_{REF}	Internal reference voltage			1.2			1.2			1.2		V
TEMPERATURE COEFFICIENTS												
	Offset drift			±0.04			±0.04			±0.04		ppm/°C
	Gain drift			±30			±30			±30		ppm/°C
	Reference-voltage drift			±8			±8			±8		ppm/°C
POWER SUPPLY												
	AVDD33		3	3.3	3.6	3	3.3	3.6	3	3.3	3.6	V
	CLKVDD18, DVDD18		1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
PSRR	Power-supply rejection ratio	DC tested		±0.2			±0.2			±0.2		%FSR/V
POWER CONSUMPTION												
		f_{DAC} = 500 MSPS, f_{OUT} = 10 MHz	300	320		300	320		300	320		mW
		f_{DAC} = 320 MSPS, f_{OUT} = 10 MHz	280			280			280			mW
	Power-down mode: no clock, DAC on sleep mode, static data pattern		3	5		3	5		3	5		mW
$I_{(AVDD33)}$	Analog supply current			50	55		50	55		50	55	mA
$I_{(DVDD18)}$	Digital supply current			60	66		60	66		60	66	mA
$I_{(CLKVDD)}$	Clock supply current			10	11		10	11		10	11	mA
	Operating range		–40	25	85	–40	25	85	–40	25	85	°C

(1) Measured differentially across IOUTAP/N or IOUTBP/N with 25 Ω each to AVDD.

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ELECTRICAL CHARACTERISTICS – DIGITAL SPECIFICATIONS

over recommended operating free-air temperature range, nominal supplies, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DAC3152			DAC3162			DAC3172			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
LVDS INPUTS: DIGITAL INPUT DATA (1)												
$V_{A,B+}$	Logic-high differential input voltage threshold		150	400		150	400		150	400		mV
VA,B–	Logic-low differential input voltage threshold		–150	–400		–150	–400		–150	–400		mV
V_{COM}	Input common mode			1.2			1.2			1.2		V
Z_T	Internal termination			110			110			110		Ω
C_L	LVDS input capacitance			2			2			2		pF
f_{INTERL}	Interleaved LVDS data rate				1000			1000			1000	MSPS
f_{DATA}	Input data rate (per DAC)				500			500			500	MSPS
CLOCK INPUT: DACCLKP/N												
	Duty cycle		40		60	40		60	40%		60%	
	Differential voltage (2)		0.4	1.0		0.4	1.0		0.4	1.0		V
	Clock Frequency				500			500			500	MHz
CMOS INTERFACE: SLEEPB												
V_{IH}	High-level input voltage		2			2			2			V
V_{IL}	Low-level input voltage				0.8			0.8			0.8	V
I_{IH}	High-level input current		-40		40	-40		40	-40		40	µA
I_{IL}	Low-level input current		-40		40	-40		40	-40		40	µA
C_I	CMOS Input capacitance			2			2			2		pF
DIGITAL INPUT DATA TIMING SPECIFICATIONS: *DOUBLE EDGE* LATCHING												
$t_{s(DATA)}$	Setup time, valid to either edge of DACCLKP/N		200			200			200			ps
$t_{h(DATA)}$	Hold time, valid after either edge of DACCLKP/N		200			200			200			ps

(1) See LVDS INPUTS section for terminology.
(2) Driving the clock input with a differential voltage lower than 1 V will result in degraded performance

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS – AC SPECIFICATIONS

over recommended operating free-air temperature range, nominal supplies, $IOUT_{FS}$ = 20mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DAC3152			DAC3162			DAC3172			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG OUTPUT (1)												
f_{DAC}	Maximum DAC rate		500			500			500			MSPS
$t_{s(DAC)}$	Output settling time to 0.1%	Transition: Code 0x0000 to 0xFFFF		10			10			10		ns
$t_{r(IOUT)}$	Output rise time 10% to 90%			220			220			220		ps
$t_{f(IOUT)}$	Output fall time 90% to 10%			220			220			220		ps
	Latency			1.5			1.5			1.5		DAC clock cycles
Power-up Time	DAC wake-up time	IOUT current settling to 1% of $IOUT_{FS}$.		2			2			2		µs
	DAC sleep time	IOUT current settling to less than 1% of $IOUT_{FS}$.		2			2			2		µs
AC PERFORMANCE (2)												
SFDR	Spurious-free dynamic range, single tone at 0 dBFS	f_{DAC} = 500 MSPS, f_{OUT} = 10 MHz		76			78			80		dBc
		f_{DAC} = 500 MSPS, f_{OUT} = 20 MHz		71			73			75		
		f_{DAC} = 500 MSPS, f_{OUT} = 70 MHz		67			68			70		
IMD3	Third-order two-tone intermodulation distortion, each tone at –12 dBFS	f_{DAC} = 500 MSPS, f_{OUT} = 10 ± 0.5 MHz		86			88			90		dBc
		f_{DAC} = 500 MSPS, f_{OUT} = 20 ± 0.5 MHz		81			83			85		
		f_{DAC} = 500 MSPS, f_{OUT} = 70 ± 0.5 MHz		72			73			75		
NSD	Noise spectral density, single tone at 0 dBFS	f_{DAC} = 500 MSPS, f_{OUT} = 10 MHz		–154			–157			–160		dBm/Hz
		f_{DAC} = 500 MSPS, f_{OUT} = 70 MHz		–153			–154			–155		
ACLR (3)	Adjacent-channel leakage ratio, single carrier	f_{DAC} = 491.52 MSPS, f_{OUT} = 30 MHz		78			79			80		dBc
		f_{DAC} = 491.52 MSPS, f_{OUT} = 70 MHz		75			76			77		
	Channel isolation	f_{DAC} = 500 MSPS, f_{OUT} = 10 MHz		100			100			100		dBc

(1) Measured single-ended into 50-Ω load.
(2) 4:1 transformer output termination, 50-Ω doubly terminated load.
(3) Single carrier, W-CDMA with 3.84 MHz BW, 5-MHz spacing, centered at IF, PAR = 12 dB. TESTMODEL 1, 10 ms

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DEFINITION OF SPECIFICATIONS

Adjacent-Carrier Leakage Ratio (ACLR): Defined for a 3.84-Mcps 3GPP W-CDMA input signal measured in a 3.84-MHz bandwidth at a 5-MHz offset from the carrier with a 12-dB peak-to-average ratio.

Analog and Digital Power-Supply Rejection Ratio (APSRR, DPSRR): Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

Differential Nonlinearity (DNL): Defined as the variation in analog output associated with an ideal 1-LSB change in the digital input code.

Gain Drift: Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Gain Error: Defined as the percentage error (in FSR%) for the ratio between the measured full-scale output current and the ideal full-scale output current.

Integral Nonlinearity (INL): Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Intermodulation Distortion (IMD3): The two-tone IMD3 is defined as the ratio (in dBc) of the third-order intermodulation distortion product to either fundamental output tone.

Offset Drift: Defined as the maximum change in dc offset, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Offset Error: Defined as the percentage error (in FSR%) for the ratio between the measured mid-scale output current and the ideal mid-scale output current.

Output Compliance Range: Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result in reduced reliability of the device or adversely affecting distortion performance.

Reference Voltage Drift: Defined as the maximum change of the reference voltage in ppm per degree Celsius from value at ambient (25°C) to values over the full operating temperature range.

Spurious-Free Dynamic Range (SFDR): Defined as the difference (in dBc) between the peak amplitude of the output signal and the peak spurious signal.

Signal-to-Noise Ratio (SNR): Defined as the ratio of the RMS value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

DATA INTERFACE

The parallel-port data interface to the device consists of a single LVDS bus that accepts interleaved A and B data with up to 14-bit resolution. Data is sampled by the LVPECL double-data-rate (DDR) clock DACCLK. DACCLK is additionally used for the data conversion process, and hence a low-jitter source is recommended. Setup and hold requirements must be met for proper sampling.

The interleaved data for channels A and B is interleaved in the form A0, B0, A1, B1… into the data bus. Data into the device is formatted according to the diagram shown in Figure 1.

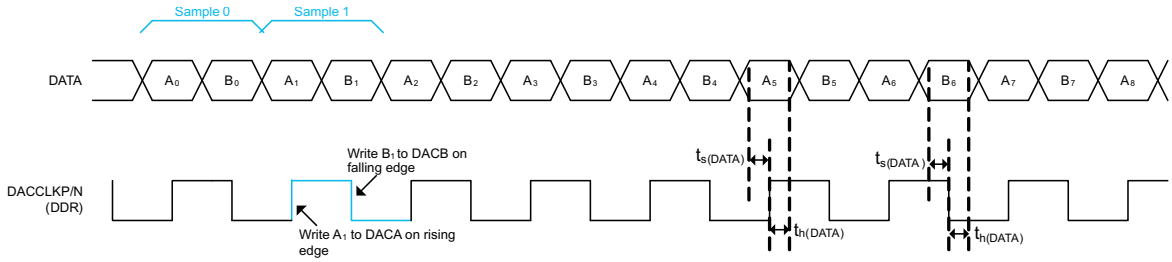

Figure 1. Data Transmission Format

CLOCK INPUT

The DAC clock (DACCLKP/N) is an internally biased differential input that for optimal performance should be driven by a low-jitter clock source. The DACCLK signal is used for both data latching (in DDR format) and as the data conversion clock. Figure 2 shows an equivalent circuit for the DAC input clock.

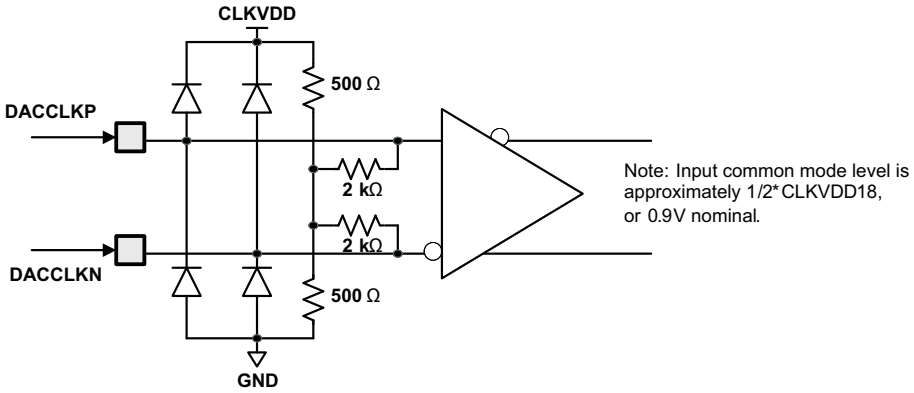

Figure 2. DACCLKP/N Equivalent Input Circuit

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The preferred configuration for driving the DACCLK input consists of a differential ECL/PECL source as shown in Figure 3. Although not optimal due to the limited signal swing, an LVDS source can also be used to drive the clock input.

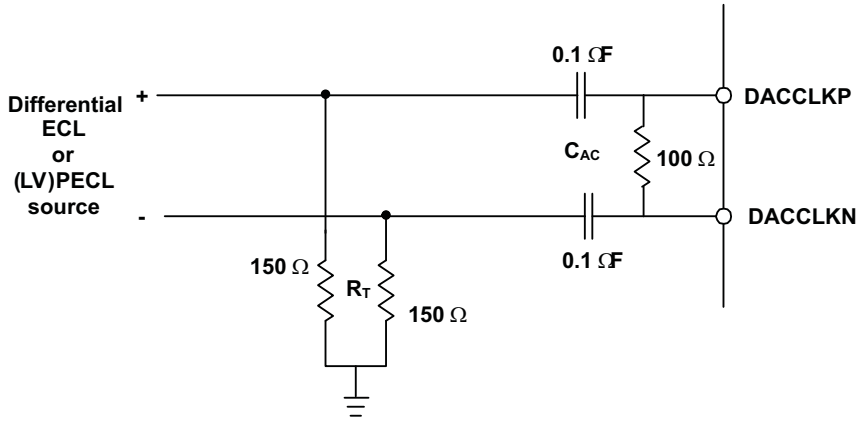

Figure 3. Preferred Clock Input Configuration With a Differential ECL/PECL Clock Source

A single-ended clock, such as a clean sinusoid or a TTL/CMOS signal (for low rate operation), can also be used to drive the clock if configured as in the input circuits of Figure 4 and Figure 5.

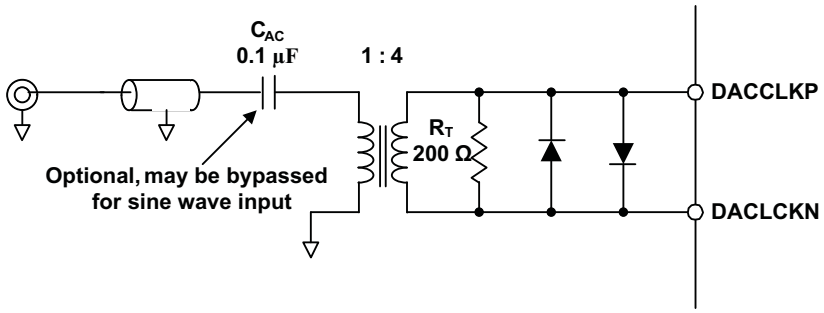

Figure 4. Clock Input Configuration Using 50-Ω Cable Input

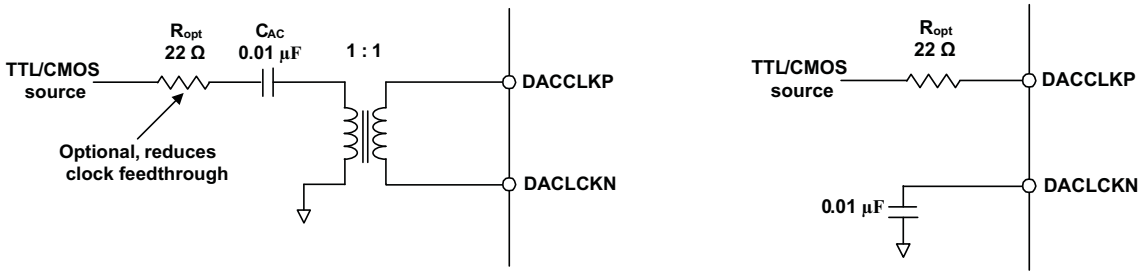

Figure 5. Clock Input Configuration With a Single-Ended TTL/CMOS Clock

PRODUCT PREVIEW

DATA INPUTS

The input data LVDS pairs (D[13:0]P/N) have the input configuration shown in Figure 6. Figure 7 shows the typical input levels and common-mode voltage used to drive these inputs.

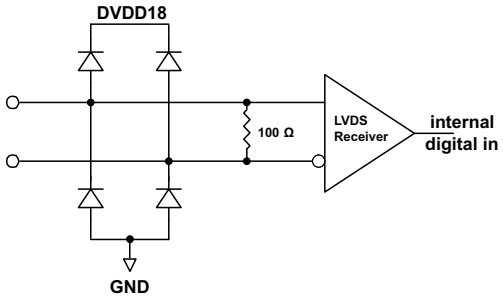

Figure 6. D[13:0]P/N LVDS Input Configuration

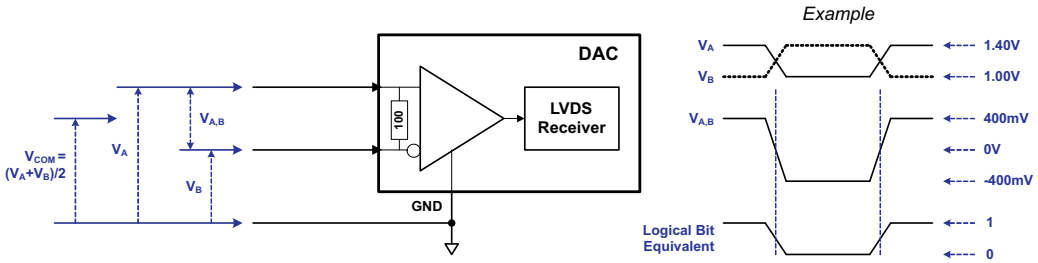

Figure 7. LVDS Data Input Levels

Table 1.

Applied Voltages		Resulting Differential Voltage	Resulting Common-Mode Voltage	Logical Bit Binary Equivalent
V_A	V_B	$V_{A,B}$	V_{COM}	
1.4 V	1 V	400 mV	1.2 V	1
1 V	1.4 V	–400 mV		0
1.2 V	0.8 V	400 mV	1 V	1
0.8 V	1.2 V	–400 mV		0

CMOS INPUT

Figure 8 shows a schematic of the SLEEPB equivalent CMOS digital inputs. See the specification table for logic thresholds. The pullup circuitry is approximately equivalent to 100 kΩ.

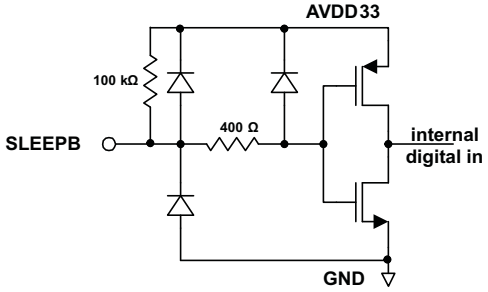

Figure 8. SLEEPB Digital Equivalent Input

PRODUCT PREVIEW

REFERENCE OPERATION

The DAC3152/DAC3162/DAC3172 uses a band-gap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS} to pin BIASJ. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip band-gap reference voltage and control amplifier. The default full-scale output current equals 16 times this bias current and can thus be expressed as:

$$IOUT_{FS} = 16 \times I_{BIAS} = 16 \times V_{BG} / R_{BIAS}$$

The band-gap reference voltage delivers an accurate voltage of 1.2 V. The full-scale output current can be adjusted from 20 mA down to 2 mA by varying resistor RBIAS or changing the externally applied reference voltage. The internal control amplifier has a wide input range, supporting the full-scale output current range of 20 dB. The recommended value for R_{BIAS} is 960 Ω, which results in a full-scale output current of 20 mA.

DAC TRANSFER FUNCTION

The DAC outputs of the DAC3152/DAC3162/DAC3172 consist of a segmented array of NMOS current sinks, capable of sinking a full-scale output current up to 20 mA. Differential current switches direct the current to either one of the complementary output nodes IOUTP or IOUTN. Complementary output currents enable differential operation, thus canceling out common-mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, and even-order distortion components, and increasing signal output power by a factor of two.

The full-scale output current is set using external resistor R_{BIAS} in combination with an on-chip band-gap voltage reference source (1.2 V) and control amplifier. Current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a maximum full-scale output current equal to 16 times I_{BIAS}.

The relation between IOUTP and IOUTN can be expressed as:

$$IOUT_{FS} = IOUTP + IOUTN$$

Current flowing into a node is denoted as – current, and current flowing out of a node as + current. Because the output stage is a current sink, the current flows from AVDD33 into the IOUTP and IOUTN pins. The output current flow in each pin driving a resistive load can be expressed as:

$$IOUTP = IOUT_{FS} \times ((2^N – 1) – CODE) / 2^N$$

$$IOUTN = IOUT_{FS} \times CODE / 2^N$$

where CODE is the decimal representation of the DAC data input word and N is the DAC bit resolution.

For the case where IOUTP and IOUTN drive resistor loads R_L directly, this translates into single-ended voltages at IOUTP and IOUTN:

$$VOUTP = AVDD – | IOUTP | \times R_L$$

$$VOUTN = AVDD – | IOUTN | \times R_L$$

Assuming that the data is full scale ($2^N – 1$ in offset binary notation) and the R_L is 25 Ω, the differential voltage between pins IOUTP and IOUTN can be expressed as:

$$VOUTP = AVDD – | – 0 \text{ mA} | \times 25 \Omega = 3.3 \text{ V}$$

$$VOUTN = AVDD – | –20 \text{ mA} | \times 25 \Omega = 2.8 \text{ V}$$

$$VDIFF = VOUTP – VOUTN = 0.5 \text{ V}$$

Note that care should be taken not to exceed the compliance voltages at nodes IOUTP and IOUTN, which would lead to increased signal distortion.

ANALOG CURRENT OUTPUTS

The DAC outputs can be easily configured to drive a doubly terminated 50-Ω cable using a properly selected RF transformer. Figure 9 and Figure 10 show the 50-Ω doubly terminated transformer configuration with 1:1 and 4:1 impedance ratios, respectively. Note that the center tap of the primary input of the transformer must be connected to AVDD to enable a dc current flow. Applying a 20-mA full-scale output current would lead to a 0.5 Vpp output for a 1:1 transformer and a 1-Vpp output for a 4:1 transformer. The low dc impedance between IOUTP or IOUTN and the transformer center tap sets the center of the ac signal to AVDD, so the 1-Vpp output for the 4:1 transformer results in an output between AVDD – 0.5 V and AVDD + 0.5 V.

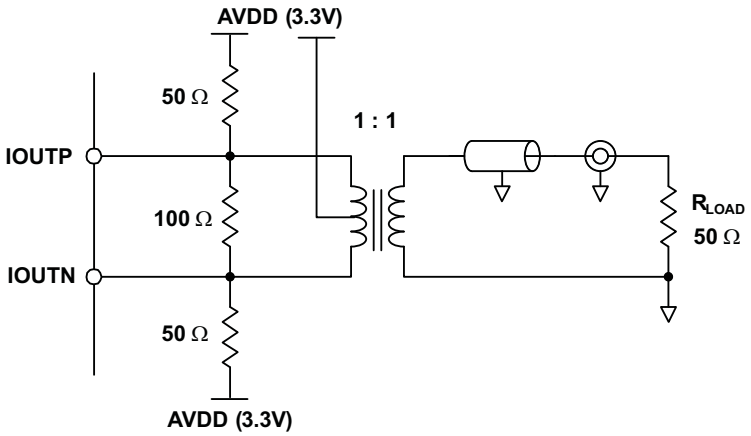

Figure 9. Driving a Doubly Terminated 50 Ω Cable Using a 1:1 Impedance Ratio Transformer

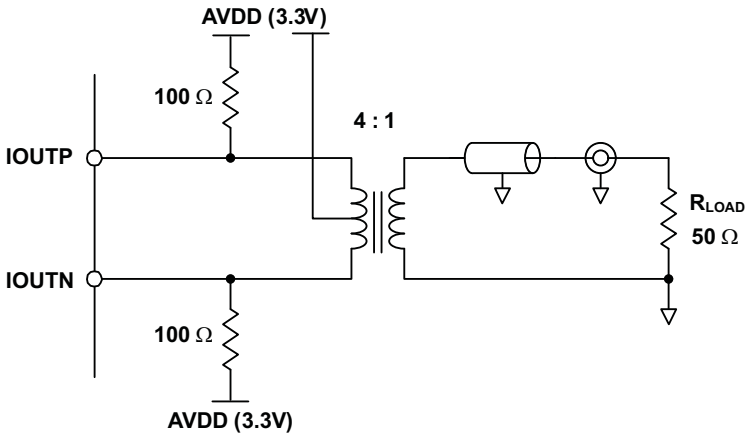

Figure 10. Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

PRODUCT PREVIEW

PASSIVE INTERFACE TO ANALOG QUADRATURE MODULATORS

A common application in communication systems is to interface the DAC to an IQ modulator like the TRF3703 family of modulators from Texas Instruments. The input of the modulator is generally of high impedance and requires a specific common-mode voltage. A simple resistive network can be used to maintain 50-Ω load impedance for the DAC3152/DAC3162/DAC3172 and also provide the necessary common-mode voltages for both the DAC and the modulator.

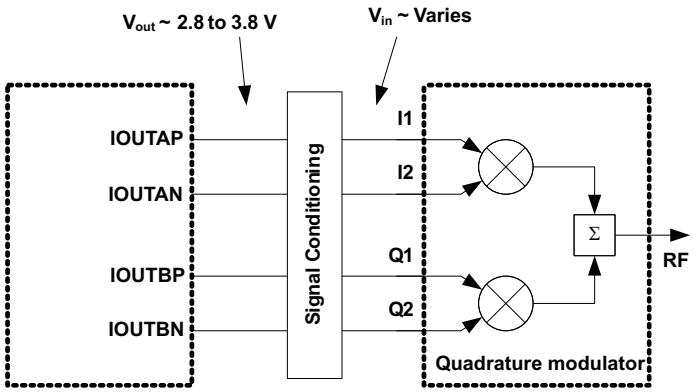

Figure 11. DAC to Analog Quadrature Modulator Interface

The DAC3152/DAC3162/DAC3172 has a maximum 20-mA full-scale output and a voltage compliance range of AVDD ± 0.5 V. The TRF3703 IQ modulator family can be operated at three common-mode voltages: 1.5 V, 1.7 V, and 3.3 V.

Figure 12 shows the recommended passive network to interface the DAC to the TRF3703-17, which has a common-mode voltage of 1.7 V. The network generates the 3.3-V common mode required by the DAC output and 1.7 V at the modulator input, while still maintaining a 50-Ω load for the DAC.

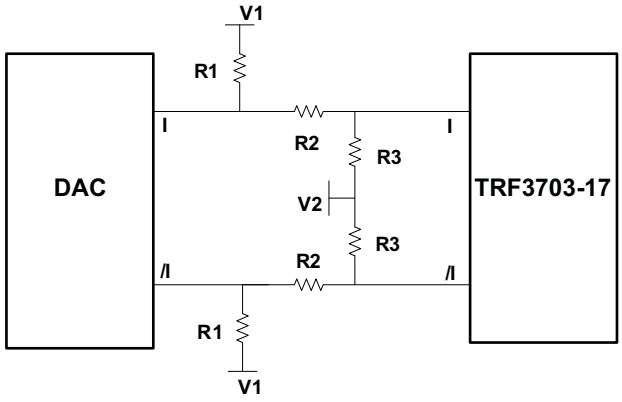

Figure 12. DAC to TRF3703-17 Interface

If V1 is set to 5 V and V2 is set to –5 V, the corresponding resistor values are R1 = 57 Ω, R2 = 80 Ω, and R3 = 336 Ω. The loss developed through R2 is about –1.86 dB. When there is no –5-V supply available and V2 is set to 0 V, the resistor values are R1 = 66 Ω, R2 = 101 Ω, and R3 = 107 Ω. The loss with these values is –5.76 dB.

Figure 13 shows the recommended network for interfacing with the TRF3703-33, which requires a common mode of 3.3 V. This is the simplest interface, as there is no voltage shift. With V1 = 5 V and V2 = 0 V, the resistor values are R1 = 66 Ω and R3 = 208 Ω.

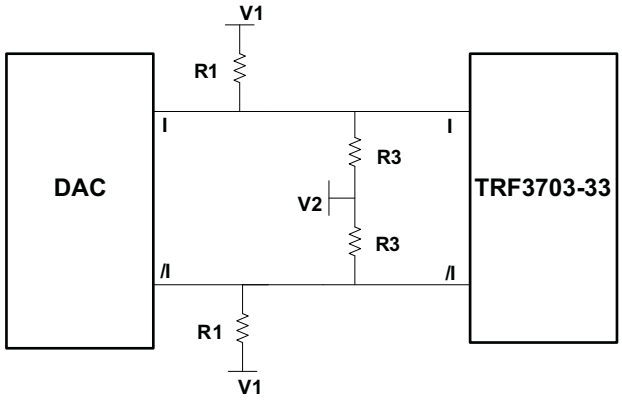

Figure 13. DAC to TRF3703-33 Interface

In most applications, a baseband filter is required between the DAC and the modulator to eliminate the DAC images. This filter can be placed after the common-mode biasing network. For the DAC to modulator network shown in Figure 14, R2 and the filter load R4 must be considered into the DAC impedance. The filter must be designed for the source impedance created by the resistor combination of R3 // (R2 + R1). The effective impedance seen by the DAC is affected by the filter termination resistor, resulting in R1 // (R2 + R3 // (R4/2)).

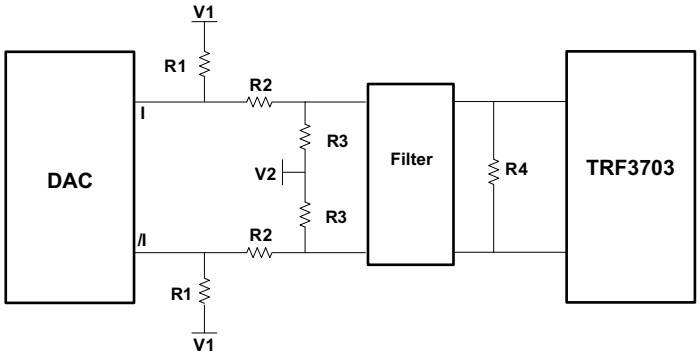

Figure 14. DAC to Modulator Interface With Filter

Factoring in R4 into the DAC load, a typical interface to the TRF3703-17 with V1 = 5 V and V2 = 0 V results in the following values: R1 = 72 Ω, R2 = 116 Ω, R3 = 124 Ω and R4 = 150 Ω. This implies that the filter must be designed for 75-Ω input and output impedance (single-ended impedance). The common-mode levels for the DAC and modulator are maintained at 3.3 V and 1.7 V, and the DAC load is 50 Ω. The added load of the filter termination causes the signal to be attenuated by –10.8 dB.

A filter can be implemented in a similar manner to interface with the TRF3703-33. In this case, it is much simpler to balance the loads and common mode voltages, due to the absence of R2. An added benefit is that there is no loss in this network. With V1 = 5 V and V2 = 0 V, the network can be designed such that R1 = 115 Ω, R3 = 681 Ω, and R4 = 200 Ω. This results in a filter impedance of R1 // R2 = 100 Ω, and a DAC load of R1 // R3 // (R4/2), which is equal to 50 Ω. R4 is a differential resistor and does not affect the common-mode level created by R1 and R3. The common-mode voltage is set at 3.3 V for a full-scale current of 20 mA.

For more information on how to interface the DAC3152/DAC3162/DAC3172 to an analog quadrature modulator, see the application reports *Passive Terminations for Current Output DACs* (SLAA399) and *Design of Differential Filters for High-Speed Signal Chains* (SLWA053)

PRODUCT PREVIEW

POWER-UP SEQUENCE

The following start-up sequence is recommended to power up the DAC3152/DAC3162/DAC3172:

- Supply 1.8 V to DVDD18 and CLKVDD18 simultaneously, and 3.3 V to AVDD33. Within AVDD33, the multiple AVDD33 pins should be powered up simultaneously. The 1.8-V and 3.3-V supplies can be powered up simultaneously or in any order.

  There are no specific requirements on the ramp rate for the supplies.
- Provide the DAC clock to the DACCLKP/N inputs.
- Toggle the SLEEPB pin for a minimum 25-ns active-low pulse duration.
- Provide the LVDS data inputs.

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
DAC3152IRGZR	PREVIEW	VQFN	RGZ	48	2500	TBD	Call TI	Call TI
DAC3152IRGZT	PREVIEW	VQFN	RGZ	48	250	TBD	Call TI	Call TI
DAC3162IRGZR	PREVIEW	VQFN	RGZ	48	2500	TBD	Call TI	Call TI
DAC3162IRGZT	PREVIEW	VQFN	RGZ	48	250	TBD	Call TI	Call TI
DAC3172IRGZR	PREVIEW	VQFN	RGZ	48	2500	TBD	Call TI	Call TI
DAC3172IRGZT	PREVIEW	VQFN	RGZ	48	250	TBD	Call TI	Call TI

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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
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TBD: The Pb-Free/Green conversion plan has not been defined.
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the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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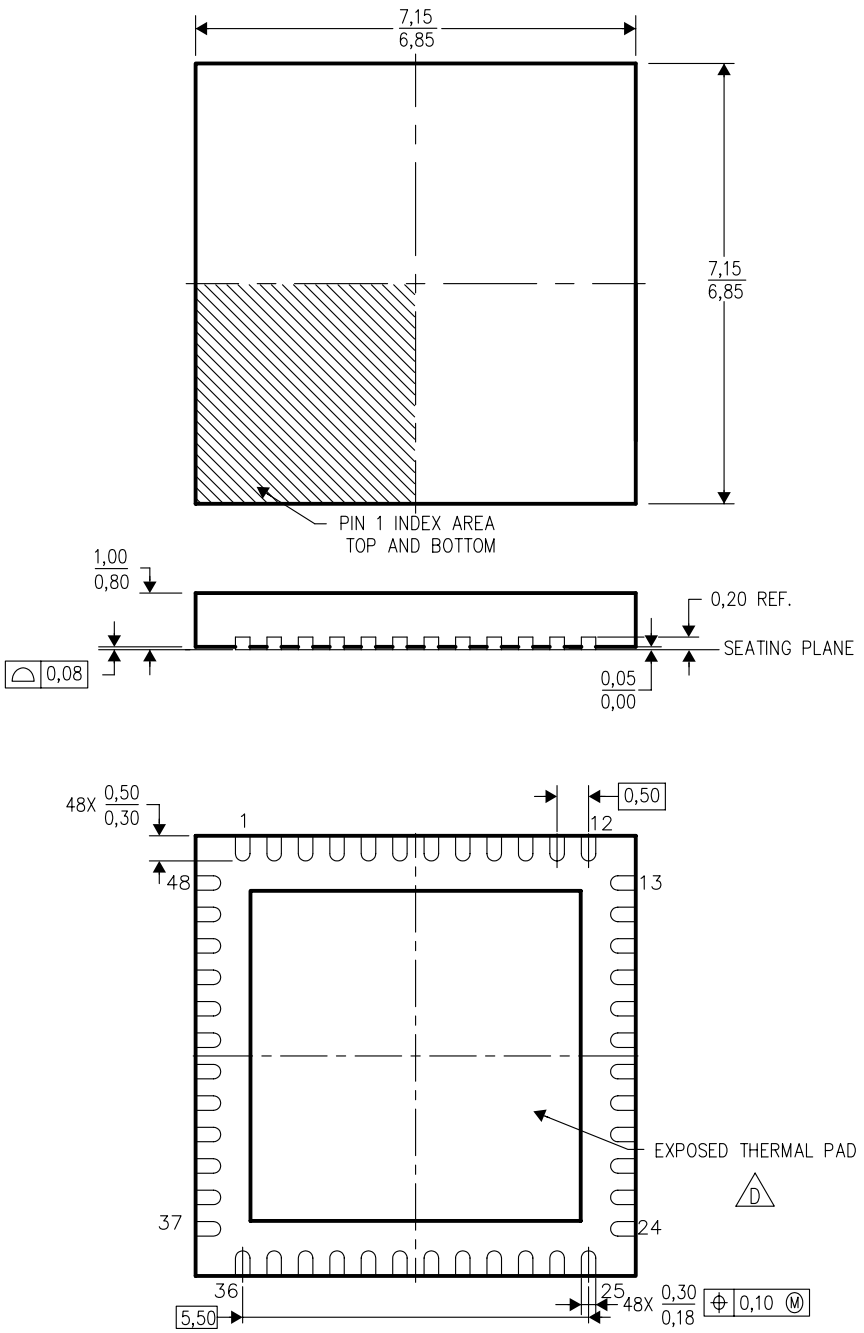

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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