2.7 V to 5.5 V, Serial-Input, Voltage-Output, Unbuffered 16-Bit DAC

AD5541A

FEATURES

Full 16-bit performance
2.7 V to 5.5 V single-supply operation
Low 0.375 mW power dissipation at 3 V
1 µs settling time
−40°C to +125°C temperature range
Low glitch: 1.1 nV-sec
50 MHz SPI-/QSPI-/MICROWIRE-/DSP-compatible interface standards
Power-on reset clears DAC output to zero scale
Available in 10-lead MSOP
Hardware LDAC function
5 kV HBM ESD classification

APPLICATIONS

Automatic test equipment
Precision source-measure instruments
Data acquisition systems
Medical instrumentation
Aerospace instrumentation
Communications infrastructure equipment
Industrial control

FUNCTIONAL BLOCK DIAGRAMS

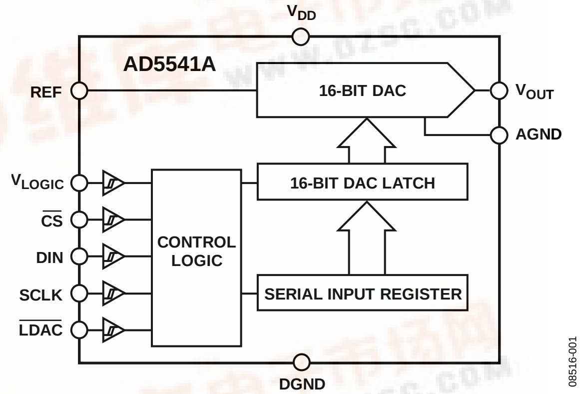

Figure 1.

GENERAL DESCRIPTION

The AD5541A is a single, 16-bit, serial input, unbuffered voltage output digital-to-analog converter (DAC) that operates from a single 2.7 V to 5.5 V supply.

The DAC output range extends from 0 V to VREF and is guaranteed monotonic, providing 1 LSB INL accuracy at 16 bits without adjustment over the full specified temperature range of −40°C to +125°C.

Offering unbuffered outputs, the AD5541A achieves a 1 µs settling time with low power consumption and low offset errors. Providing low noise performance of 11.8 nV/√Hz and low glitch, the AD5541A is suitable for deployment across multiple end systems.

The AD5541A uses a versatile 3-wire interface that is compatible with a 50 MHz SPI, QSPI™, MICROWIRE™, and DSP interface standards.

PRODUCT HIGHLIGHTS

1. Single-Supply Operation. The AD5541A is fully specified and guaranteed for a single 2.7 V to 5.5 V supply.
2. Low Power Consumption. This part consumes, typically, 0.625 mW with a 5 V supply and 0.375 mW at 3 V.
3. 3-Wire Serial Interface.
4. Unbuffered Output Capable of Driving 60 kΩ Loads. This reduces power consumption because there is no internal buffer to drive.
5. Power-On Reset Circuitry.

Table 1. Related Devices

Part No.	Description
AD5541	Single,16-bit unbuffered *nano*DAC, ±1 LSB INL, SOIC
AD5024/ AD5044/ AD5064	Quad 12-/14-/16-bit *nano*DAC, ±1 LSB INL, TSSOP
AD5062	Single, 16-bit *nano*DAC, ±1 LSB INL, SOT-23
AD5063	Single, 16-bit *nano*DAC, ±1 LSB INL, MSOP
AD5061	Single, 16-bit *nano*DAC, ±4 LSB INL, SOT-23
AD5040/AD5060	14-/16-bit *nano*DAC, ±1 LSB INL, SOT-23

Rev. 0

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REVISION HISTORY

7/10—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, 2.5 V ≤ V_{REF} ≤ V_{DD}, AGND = DGND = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Condition
STATIC PERFORMANCE					
Resolution	16			Bits	
Relative Accuracy (INL)		±0.5	±1.0	LSB	B grades
		±0.5	±2.0	LSB	A grade
Differential Nonlinearity (DNL)		±0.5	±1.0	LSB	Guaranteed monotonic
Gain Error		0.5	±2	LSB	T_A = 25°C
			±3	LSB	−40°C < T_A < +85°C
			±4	LSB	−40°C < T_A < +125°C
Gain Error Temperature Coefficient		±0.1		ppm/°C	
Zero-Code Error		0.3	±0.7	LSB	T_A = 25°C
			±1.5	LSB	−40°C < T_A < +85°C
			±3	LSB	−40°C < T_A < +125°C
Zero-Code Temperature Coefficient		±0.05		ppm/°C	
DC Power Supply Rejection Ratio			±1	LSB	ΔV_{DD} ± 10%
OUTPUT CHARACTERISTICS[1]					
Output Voltage Range	0		V_{REF} − 1 LSB	V	Unipolar operation
DAC Output Impedance		6.25		kΩ	Tolerance typically 20%
DAC REFERENCE INPUT[2]					
Reference Input Range	2.0		V_{DD}	V	
Reference Input Resistance	9			kΩ	Unipolar operation
Reference Input Capacitance		26		pF	Code 0x0000
		26		pF	Code 0xFFFF
LOGIC INPUTS					
Input Current			±1	μA	
Input Low Voltage, V_{INL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
Input High Voltage, V_{INH}	2.4			V	V_{DD} = 2.7 V to 5.5 V
Input Capacitance[1]			10	pF	
Hysteresis Voltage[1]		0.15		V	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	All digital inputs at 0, V_{LOGIC}, or V_{DD}
I_{DD}		125	150	μA	V_{IH} = V_{LOGIC} or V_{DD} and V_{IL} = GND
V_{LOGIC}	1.8		5.5	V	
I_{LOGIC}		15	24	μA	All digital inputs at 0, V_{LOGIC}, or V_{DD}
Power Dissipation		0.625	0.825	mW	

[1] Guaranteed by design, not subject to production test.
[2] Reference input resistance is code-dependent, minimum at 0x8555.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, 2.5 V ≤ V_{REF} ≤ V_{DD}, AGND = DGND = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Condition
Output Voltage Settling Time		1		µs	To 1/2 LSB of FS, C_L = 10 pF
Slew Rate		17		V/µs	C_L = 10 pF, measured from 0% to 63%
Digital-to-Analog Glitch Impulse		1.1		nV-sec	1 LSB change around major carry
Reference −3 dB Bandwidth		2.2		MHz	All 1s loaded
Reference Feedthrough		1		mV p-p	All 0s loaded, V_{REF} = 1 V p-p at 100 kHz
Digital Feedthrough		0.2		nV-sec	
Signal-to-Noise Ratio		92		dB	
Spurious Free Dynamic Range		80		dB	Digitally generated sine wave at 1 kHz
Total Harmonic Distortion		74		dB	DAC code = 0xFFFF, frequency 10 kHz, V_{REF} = 2.5 V ± 1 V p-p
Output Noise Spectral Density		11.8		nV/√Hz	DAC code = 0x8400, frequency = 1 kHz
Output Noise		0.134		µV p-p	0.1 Hz to 10 Hz

TIMING CHARACTERISTICS

V_{LOGIC} = 2.7 V to 5.5 V, V_{DD} = 5 V, 2.5 V ≤ V_{REF} ≤ V_{DD}, V_{INH} = 90% of V_{LOGIC}, V_{INL} = 10% of V_{LOGIC}, AGND = DGND = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 4.

Parameter[1, 2]	Limit	Unit	Description
f_{SCLK}	50	MHz max	SCLK cycle frequency
t_1	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	5	ns min	$\overline{\text{CS}}$ low to SCLK high setup
t_5	5	ns min	$\overline{\text{CS}}$ high to SCLK high setup
t_6	5	ns min	SCLK high to $\overline{\text{CS}}$ low hold time
t_7	5	ns min	SCLK high to $\overline{\text{CS}}$ high hold time
t_8	10	ns min	Data setup time
t_9	4	ns min	Data hold time (V_{INH} = 90% of V_{DD}, V_{INL} = 10% of V_{DD})
t_9	5	ns min	Data hold time (V_{INH} = 3 V, V_{INL} = 0 V)
t_{10}	20	ns min	$\overline{\text{LDAC}}$ pulsewidth
t_{11}	10	ns min	$\overline{\text{CS}}$ high to $\overline{\text{LDAC}}$ low setup
t_{12}	15	ns min	$\overline{\text{CS}}$ high time between active periods

[1] Guaranteed by design and characterization. Not production tested
[2] All input signals are specified with $t_R = t_F$ = 1 ns/V and timed from a voltage level of $(V_{INL} + V_{INH})/2$.

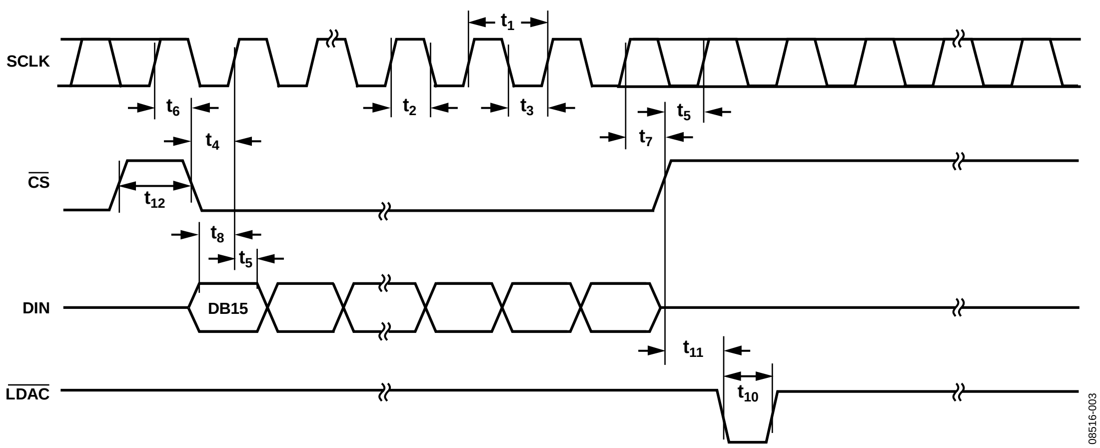


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

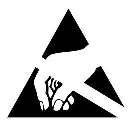
Table 5.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +6 V
V_{LOGIC} to DGND	−0.3 V to +6 V
Digital Input Voltage to DGND	−0.3 V to V_{DD}/V_{LOGIC} + 0.3 V
V_{OUT} to AGND	−0.3 V to V_{DD} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies	±10 mA
Operating Temperature Range	
Industrial (A, B Versions)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature (T_J max)	150°C
Package Power Dissipation	(T_J max − T_A)/θ_{JA}
Thermal Impedance, θ_{JA}	
MSOP (RM-10)	135°C/W
Lead Temperature, Soldering	
Peak Temperature[1]	260°C
ESD[2]	5 kV

[1] As per JEDEC Standard 20.
[2] Human body model (HBM) classification.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

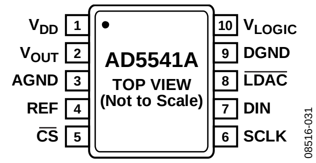


Figure 3. AD5541A 10-Lead MSOP Pin Configuration

Table 6. AD5541A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Analog Supply Voltage, 5 V ± 10%.
2	V_{OUT}	Analog Output Voltage from the DAC.
3	AGND	Ground Reference Point for Analog Circuitry.
4	REF	Voltage Reference Input for the DAC. Connect to an external 2.5 V reference. Reference can range from 2 V to V_{DD}.
5	$\overline{CS}$	Logic Input Signal. The chip select signal is used to frame the serial data input.
6	SCLK	Clock Input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
7	DIN	Serial Data Input. This device accepts 16-bit words. Data is clocked into the input register on the rising edge of SCLK.
8	$\overline{LDAC}$	$\overline{LDAC}$ Input. When this input is taken low, the DAC register is simultaneously updated with the contents of the serial register data.
9	DGND	Digital Ground. Ground reference for digital circuitry.
10	V_{LOGIC}	Logic Power Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

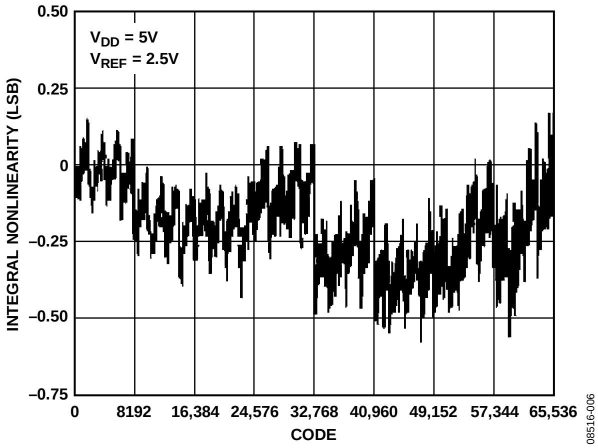


Figure 4. Integral Nonlinearity vs. Code

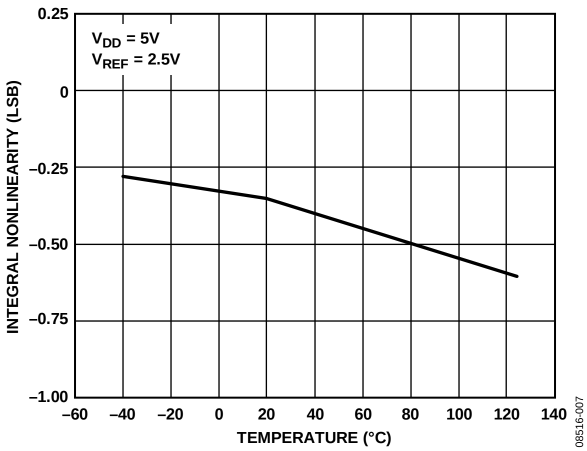


Figure 5. Integral Nonlinearity vs. Temperature

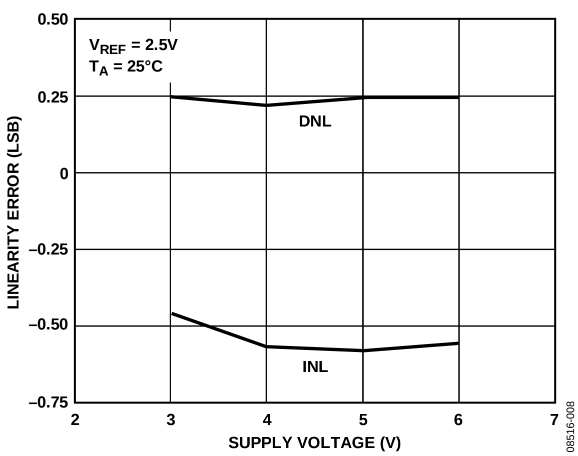


Figure 6. Linearity Error vs. Supply Voltage

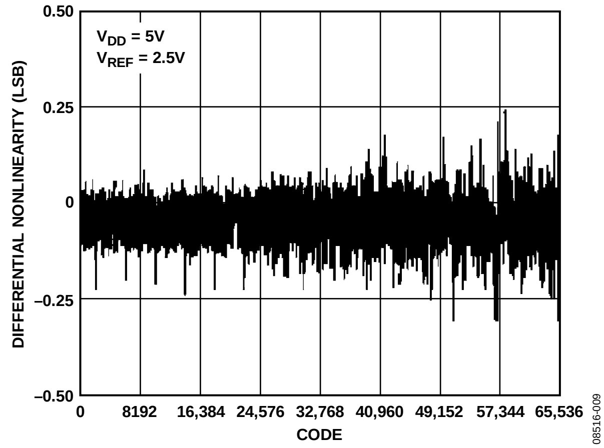


Figure 7. Differential Nonlinearity vs. Code

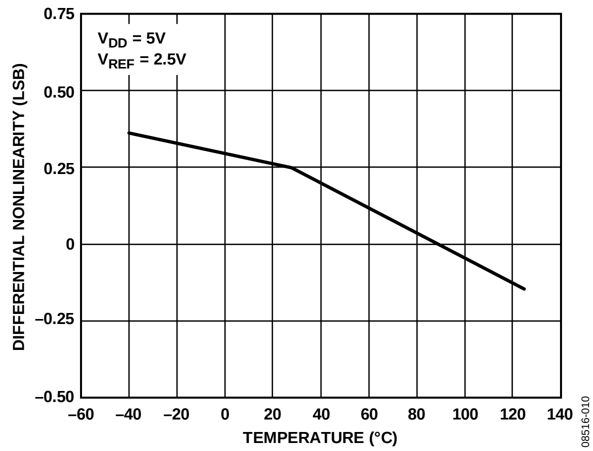


Figure 8. Differential Nonlinearity vs. Temperature

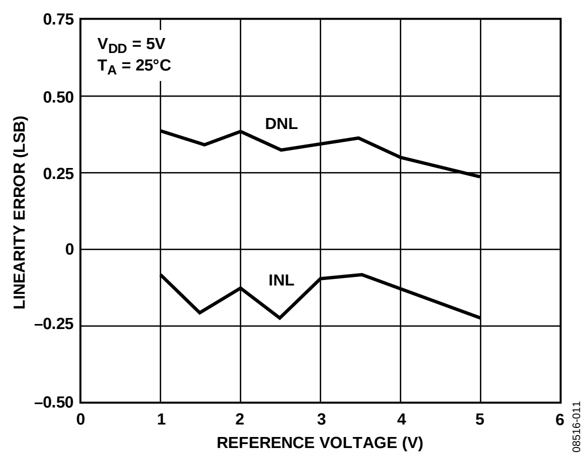


Figure 9. Linearity Error vs. Reference Voltage

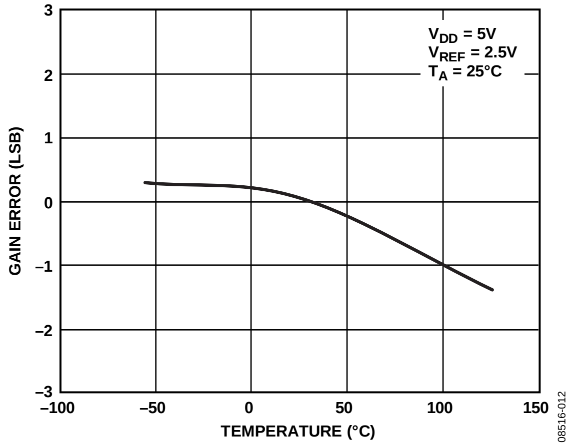


Figure 10. Gain Error vs. Temperature

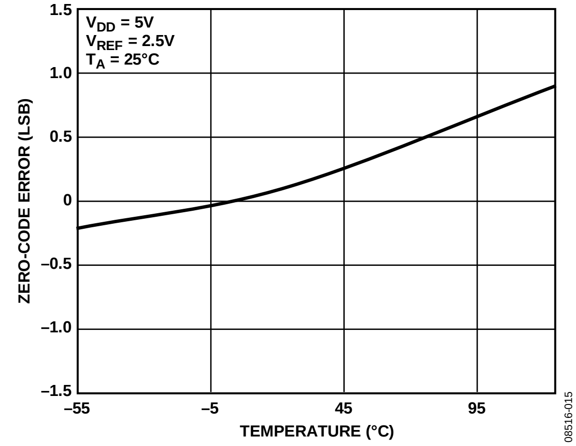


Figure 13. Zero-Code Error vs. Temperature

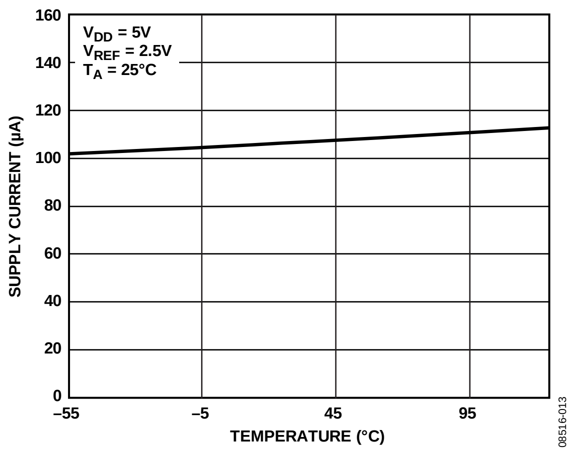


Figure 11. Supply Current vs. Temperature

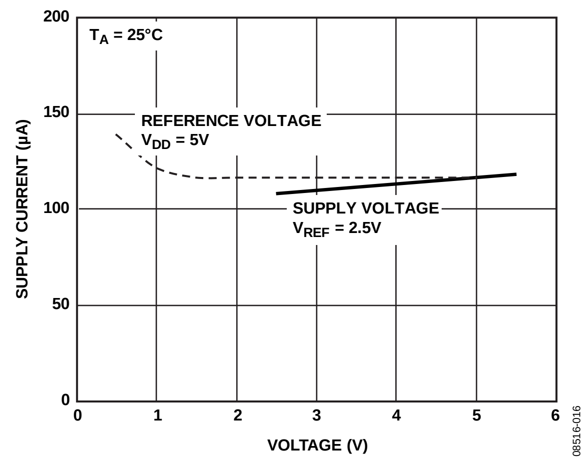


Figure 14. Supply Current vs. Reference Voltage or Supply Voltage

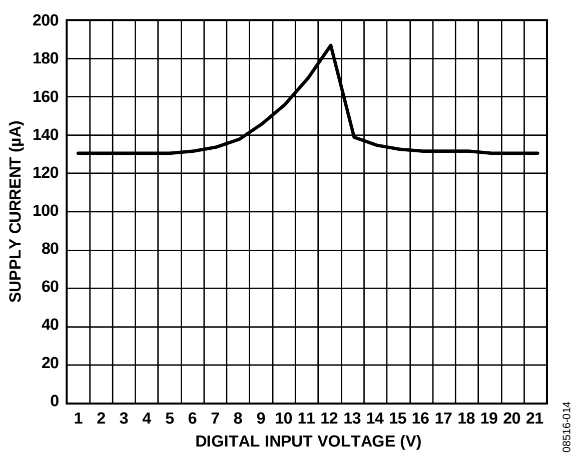


Figure 12. Supply Current vs. Digital Input Voltage

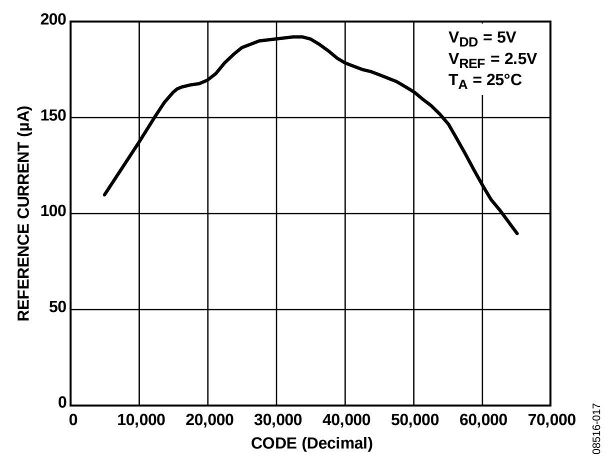


Figure 15. Reference Current vs. Code

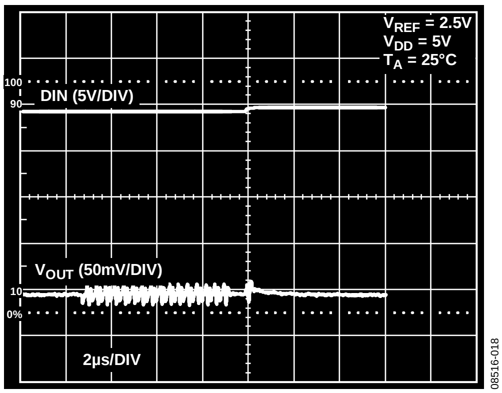


Figure 16. Digital Feedthrough

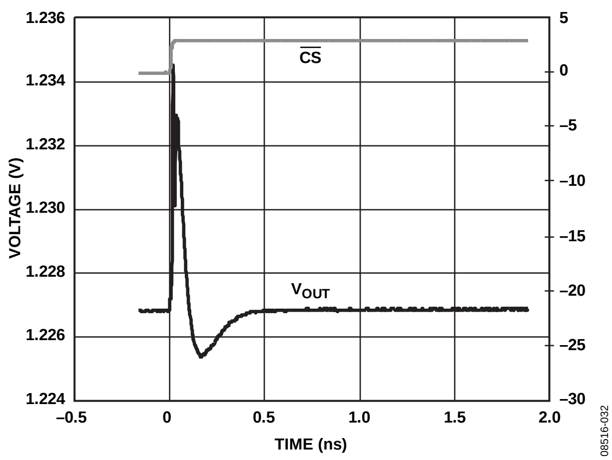


Figure 17. Digital-to-Analog Glitch Impulse

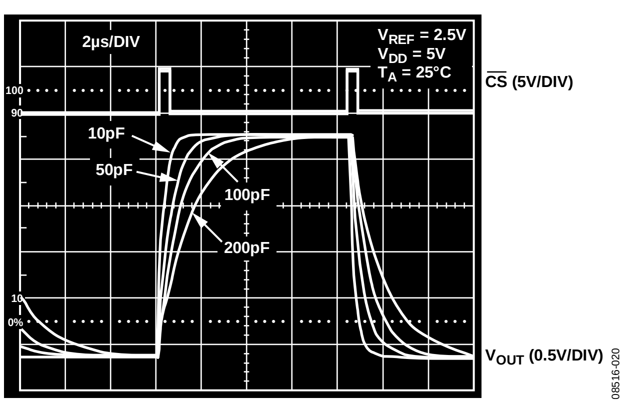


Figure 18. Large Signal Settling Time

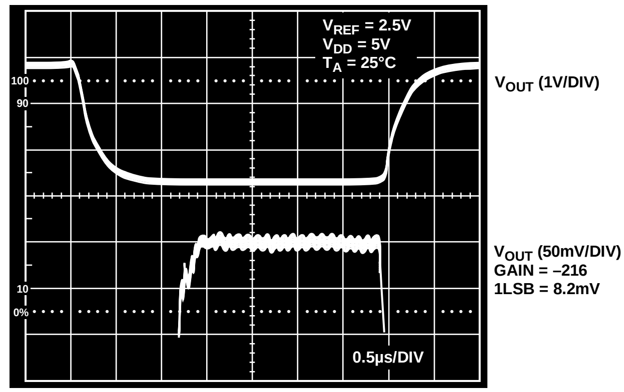


Figure 19. Small Signal Settling Time

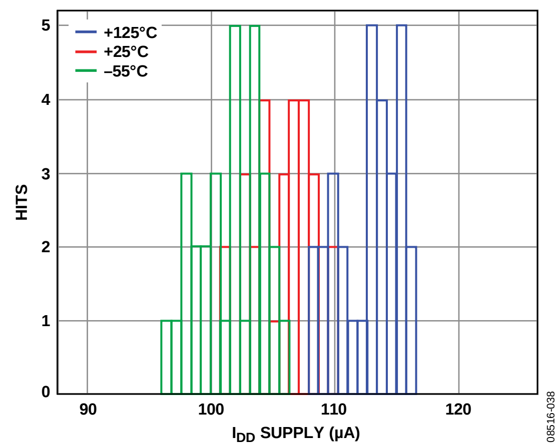


Figure 20. Analog Supply Current Histogram

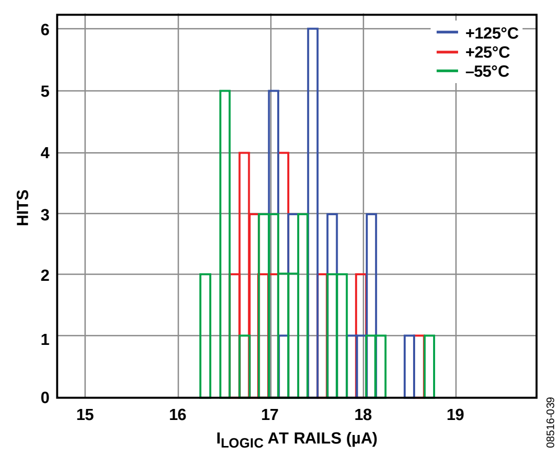


Figure 21. Digital Supply Current Histogram

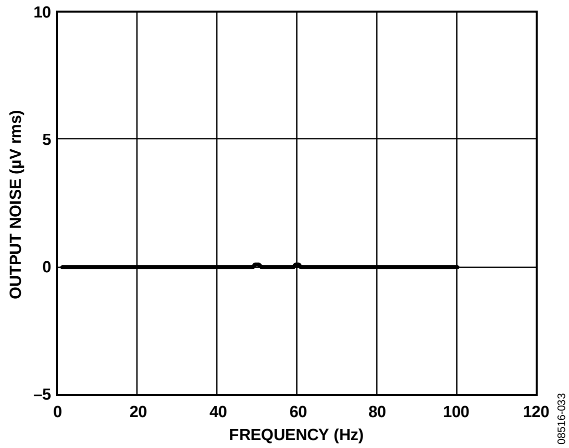


Figure 22. 0.1 Hz to 10 Hz Output Noise

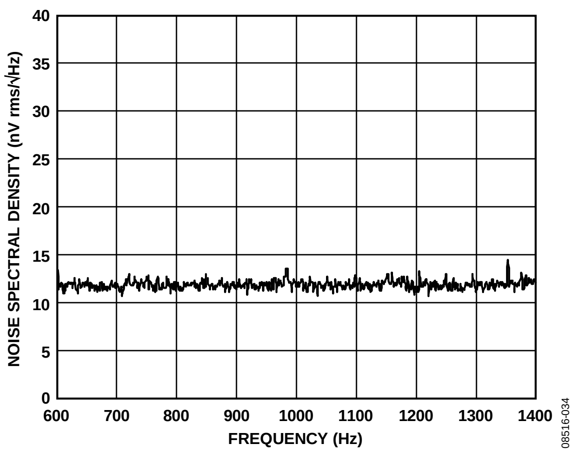


Figure 23. Noise Spectral Density vs. Frequency,1 kHz

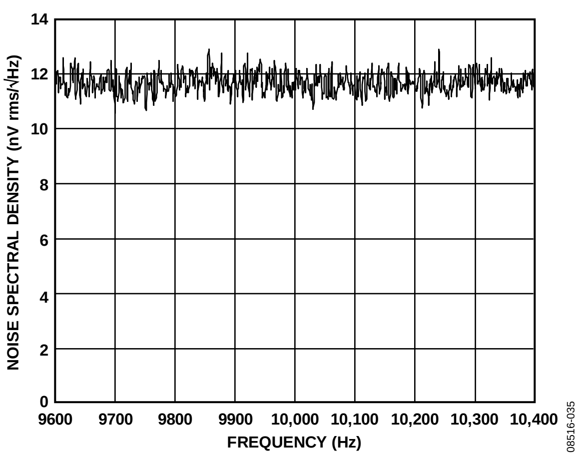


Figure 24. Noise Spectral Density vs. Frequency, 10 kHz

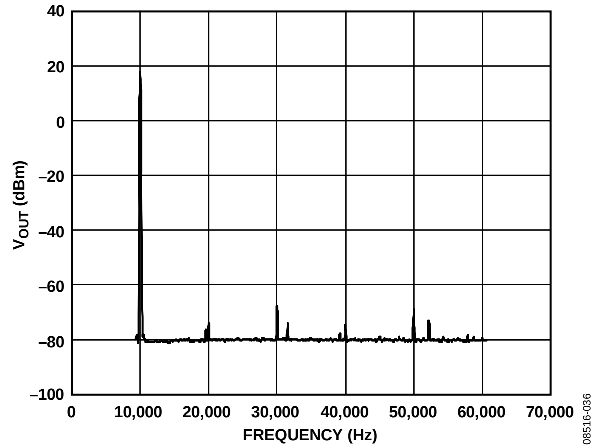


Figure 25. Total Harmonic Distortion

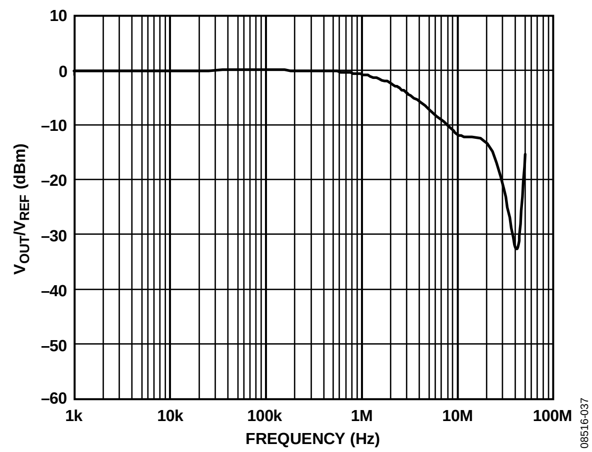


Figure 26. Multiplying Bandwidth

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or INL is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 4.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. A typical DNL vs. code plot is shown in Figure 7.

Gain Error
Gain error is the difference between the actual and ideal analog output range, expressed as a percent of the full-scale range. It is the deviation in slope of the DAC transfer characteristic from ideal.

Gain Error Temperature Coefficient
Gain error temperature coefficient is a measure of the change in gain error with changes in temperature. It is expressed in ppm/°C.

Zero-Code Error
Zero-code error is a measure of the output error when zero-code is loaded to the DAC register.

Zero-Code Temperature Coefficient
This is a measure of the change in zero-code error with a change in temperature. It is expressed in mV/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition. A digital-to-analog glitch impulse plot is shown in Figure 17.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. $\overline{CS}$ is held high while the SCLK and DIN signals are toggled. It is specified in nV-sec and is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa. A typical digital feedthrough plot is shown in Figure 16.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage. The power-supply rejection ratio is quoted in terms of percent change in output per percent change in V_{DD} for full-scale output of the DAC. V_{DD} is varied by ±10%.

Reference Feedthrough
Reference feedthrough is a measure of the feedthrough from the V_{REF} input to the DAC output when the DAC is loaded with all 0s. A 100 kHz, 1 V p-p is applied to V_{REF}. Reference feedthrough is expressed in mV p-p.

THEORY OF OPERATION

The AD5541A is a single, 16-bit, serial input, voltage output DAC. It operates from a single supply ranging from 2.7 V to 5 V and consumes typically 125 μA with a supply of 5 V. Data is written to these devices in a 16-bit word format, via a 3- or 4-wire serial interface. To ensure a known power-up state, this part is designed with a power-on reset function. The output is reset to 0 V.

DIGITAL-TO-ANALOG SECTION

The DAC architecture consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 27. The DAC architecture of the AD5541A is segmented. The four MSBs of the 16-bit data-word are decoded to drive 15 switches, E1 to E15. Each switch connects one of 15 matched resistors to either AGND or V_{REF}. The remaining 12 bits of the data-word drive the S0 to S11 switches of a 12-bit voltage mode R-2R ladder network.

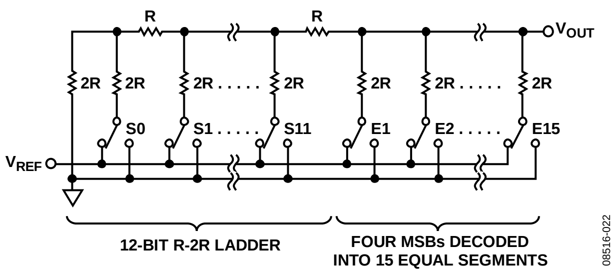


Figure 27. DAC Architecture

With this type of DAC configuration, the output impedance is independent of code, while the input impedance seen by the reference is heavily code dependent. The output voltage is dependent on the reference voltage, as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:
D is the decimal data-word loaded to the DAC register.
N is the resolution of the DAC.

For a reference of 2.5 V, the equation simplifies to the following:

$$V_{OUT} = \frac{2.5 \times D}{65{,}536}$$

This gives a V_{OUT} of 1.25 V with midscale loaded and 2.5 V with full-scale loaded to the DAC.

The LSB size is V_{REF}/65,536.

SERIAL INTERFACE

The AD5541A is controlled by a versatile 3- or 4-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards. The timing diagram is shown in Figure 2. The AD5541A has a separate serial input register from the 16-bit DAC register that allows preloading of a new data value into the serial input register without disturbing the present DAC output voltage.

Input data is framed by the chip select input, $\overline{CS}$. After a high-to-low transition on $\overline{CS}$, data is shifted synchronously and latched into the serial input register on the rising edge of the serial clock, SCLK. After 16 data bits have been loaded into the serial input register, a low-to-high transition on $\overline{CS}$ transfers the contents of the shift register to the DAC register if $\overline{LDAC}$ is held low. If $\overline{LDAC}$ is high at this point, a low-to-high transition on $\overline{CS}$ transfers the contents into the serial input register only. After a new value is fully loaded in the serial input register, it can be asynchronously transferred to the DAC register by strobing the $\overline{LDAC}$ pin. Data is loaded MSB first in 16-bit words. Data can be loaded to the part only while $\overline{CS}$ is low.

UNIPOLAR OUTPUT OPERATION

This DAC is capable of driving unbuffered loads of 60 kΩ. Unbuffered operation results in low supply current, typically 300 µA, and a low offset error. The AD5541A provides a unipolar output swing ranging from 0 V to V_{REF}. Figure 28 shows a typical unipolar output voltage circuit. The code table for this mode of operation is shown in Table 7. The example includes the ADR421 2.5 V reference and the AD8628 low offset and zero-drift reference buffer.

Table 7. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output
1111 1111 1111 1111	$V_{REF} \times (65{,}535/65{,}536)$
1000 0000 0000 0000	$V_{REF} \times (32{,}768/65{,}536) = ½\ V_{REF}$
0000 0000 0000 0001	$V_{REF} \times (1/65{,}536)$
0000 0000 0000 0000	0 V

Assuming a perfect reference, the unipolar worst-case output voltage can be calculated from the following equation:

$$V_{OUT-UNI} = \frac{D}{2^{16}} \times (V_{REF} + V_{GE}) + V_{ZSE} + INL$$

where:
$V_{OUT-UNI}$ is the unipolar mode worst-case output.
D is the code loaded to DAC.
V_{REF} is the reference voltage applied to the part.
V_{GE} is the gain error in volts.
V_{ZSE} is the zero-scale error in volts.
INL is the integral nonlinearity in volts.

OUTPUT AMPLIFIER SELECTION

For bipolar mode, a precision amplifier should be used and supplied from a dual power supply. This provides the $\pm V_{REF}$ output. In a single-supply application, selection of a suitable op amp may be more difficult as the output swing of the amplifier does not usually include the negative rail, in this case, AGND. This can result in some degradation of the specified performance unless the application does not use codes near zero.

The selected op amp must have a very low-offset voltage (the DAC LSB is 38 µV with a 2.5 V reference) to eliminate the need for output offset trims. Input bias current should also be very low because the bias current, multiplied by the DAC output impedance (approximately 6 kΩ), adds to the zero-code error. Rail-to-rail input and output performance is required. For fast settling, the slew rate of the op amp should not impede the settling time of the DAC. Output impedance of the DAC is constant and code-independent, but to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3 dB amplifier bandwidth results in a shorter effective settling time of the combined DAC and amplifier.

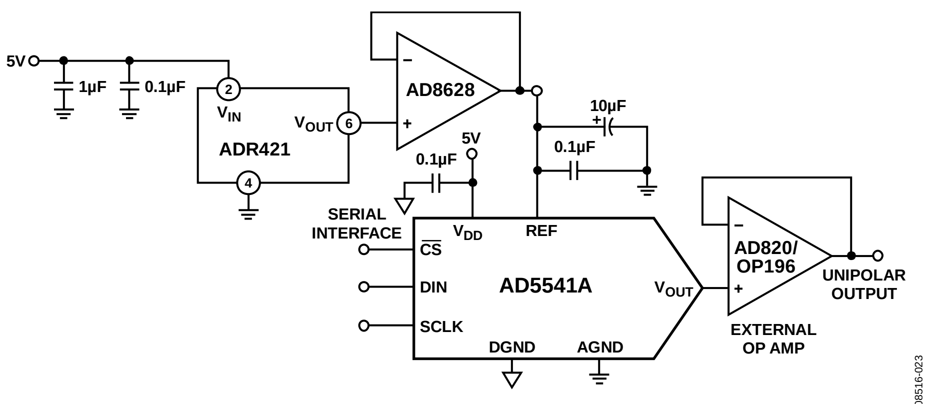


Figure 28. Unipolar Output

FORCE SENSE AMPLIFIER SELECTION

Use single-supply, low-noise amplifiers. A low-output impedance at high frequencies is preferred because the amplifiers must be able to handle dynamic currents of up to ±20 mA.

REFERENCE AND GROUND

Because the input impedance is code-dependent, drive the reference pin from a low impedance source. The AD5541A operates with a voltage reference ranging from 2 V to V_{DD}. References below 2 V result in reduced accuracy. The full-scale output voltage of the DAC is determined by the reference. Table 7 outlines the analog output voltage or particular digital codes.

If the application doesn't require separate force and sense lines, tie the lines close to the package to minimize voltage drops between the package leads and the internal die.

POWER-ON RESET

The AD5541A has a power-on reset function to ensure that the output is at a known state on power-up. On power-up, the DAC register contains all 0s until the data is loaded from the serial register. However, the serial register is not cleared on power-up; therefore, its contents are undefined. When loading data initially to the DAC, 16 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 16 bits are loaded, the last 16 are kept, and if less than 16 bits are loaded, bits remain from the previous word. If the AD5541A must be interfaced with data shorter than 16 bits, pad the data with 0s at the LSBs.

POWER SUPPLY AND REFERENCE BYPASSING

For accurate high-resolution performance, it is recommended that the reference and supply pins be bypassed with a 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor.

APPLICATIONS INFORMATION

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5541A is via a serial bus that uses standard protocol that is compatible with DSP processors and microcontrollers. The communications channel requires a 3- or 4-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5541A requires a 16-bit data-word with data valid on the rising edge of SCLK.

AD5541A TO ADSP-BF531 INTERFACE

The SPI interface of the AD5541A is designed to be easily connected to industry-standard DSPs and microcontrollers. Figure 29 shows how the AD5541A can be connected to the Analog Devices, Inc., Blackfin® DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5541A.

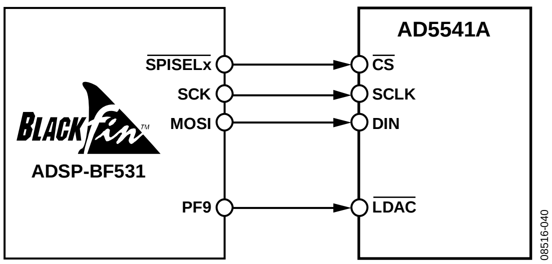


Figure 29. AD5541A to ADSP-2101 Interface

AD5541A TO SPORT INTERFACE

The Analog Devices ADSP-BF527 has one SPORT serial port. Figure 30 shows how one SPORT interface can be used to control the AD5541A.

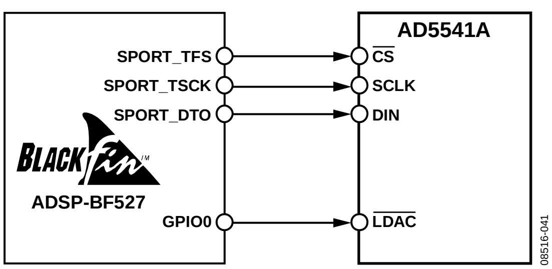


Figure 30. AD5541A to 68HC11/68L11 Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the printed circuit board (PCB) on which the AD5541A is mounted so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5541A is in a system where multiple devices require an analog ground-to-digital ground connection, make the connection at one point only. Establish the star ground point as close as possible to the device.

The AD5541A should have ample supply bypassing of 10 μF in parallel with 0.1 μF on each supply located as close to the package as possible, ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. *i*Coupler® products from Analog Devices provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5541A makes the part ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 31 shows a 4-channel isolated interface to the AD5541A using an ADuM1400. For further information, visit http://www.analog.com/icouplers.

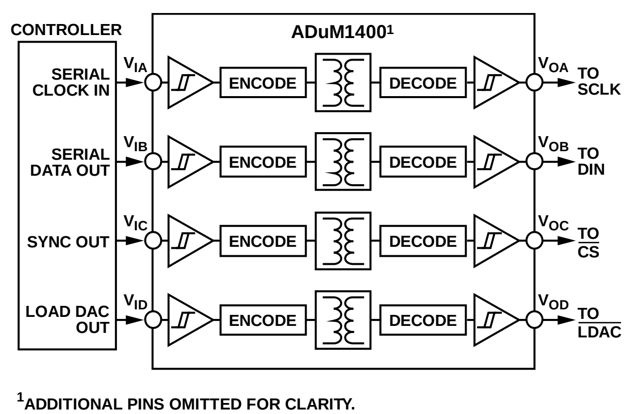


Figure 31. Isolated Interface

DECODING MULTIPLE DACS

The $\overline{CS}$ pin of the AD5541A can be used to select one of a number of DACs. All devices receive the same serial clock and serial data, but only one device receives the $\overline{CS}$ signal at any one time. The DAC addressed is determined by the decoder. There is some digital feedthrough from the digital input lines. Using a burst clock minimizes the effects of digital feedthrough on the analog signal channels. Figure 32 shows a typical circuit.

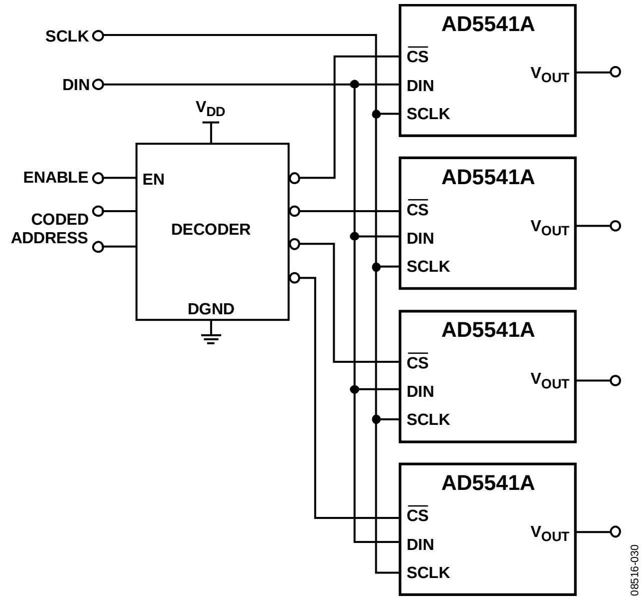


Figure 32. Addressing Multiple DACs

OUTLINE DIMENSIONS

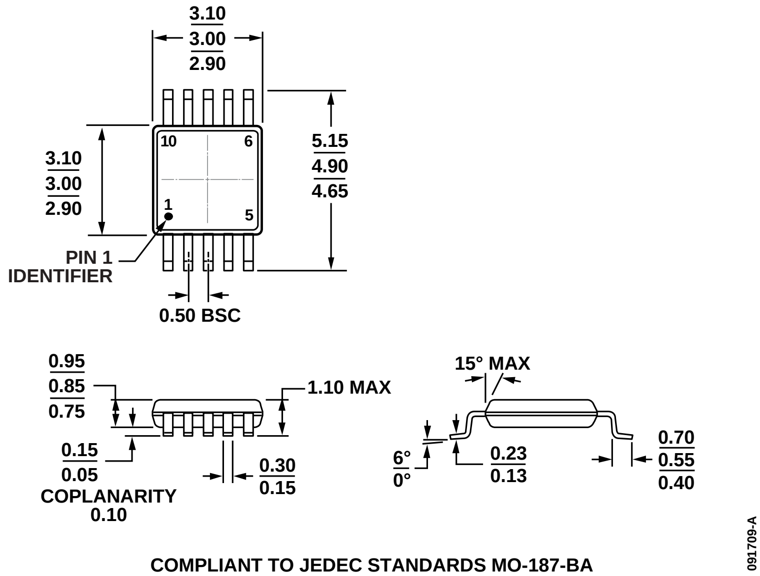


Figure 33. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	INL	DNL	Power-On Reset to Code	Temperature Range	Package Description	Package Option	Branding Code
AD5541ABRMZ	±1 LSB	±1 LSB	Zero Scale	−40°C to +125°C	10-Lead MSOP	RM-10	DEQ
AD5541ABRMZ-REEL7	±1 LSB	±1 LSB	Zero Scale	−40°C to +125°C	10-Lead MSOP	RM-10	DEQ
AD5541AARMZ	±2 LSB	±1 LSB	Zero Scale	−40°C to +125°C	10-Lead MSOP	RM-10	DER
AD5541AARMZ-REEL7	±2 LSB	±1 LSB	Zero Scale	−40°C to +125°C	10-Lead MSOP	RM-10	DER

[1] Z = RoHS Compliant Part.

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