查询"Si5980DU"供应商

Dual N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
100	0.567 at V_{GS} = 10 V	2.5	2.2 nC

FEATURES

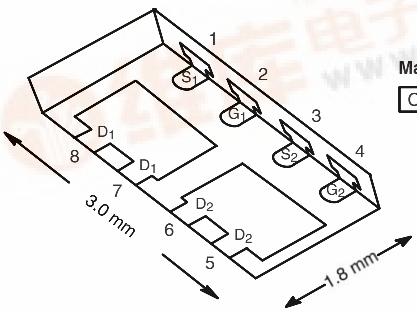
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® ChipFET® Package
  - Small Footprint Area
  - Low On-Resistance
  - Thin 0.8 mm Profile
- Compliant to RoHS Directive 2002/95/EC

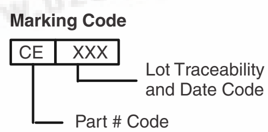
Pb-free
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

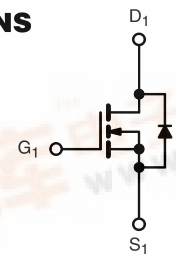
- Load Supply
- Power Supply

PowerPAK® ChipFET Dual

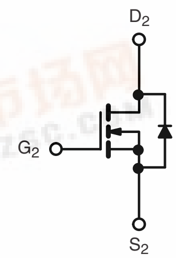




Bottom View



N-Channel MOSFET



N-Channel MOSFET

Ordering Information: Si5980DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	2.5	A
	T_C = 70 °C		2.0	
	T_A = 25 °C		1.3[b, c]	
	T_A = 70 °C		1.0[b, c]	
Pulsed Drain Current		I_{DM}	3	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	6[a]	
	T_A = 25 °C		1.7[b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	2	
Avalanche Energy		E_{AS}	0.2	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	7.8	W
	T_C = 70 °C		5.0	
	T_A = 25 °C		2.0[b, c]	
	T_A = 70 °C		1.3[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, f]	t ≤ 5 s	R_{thJA}	49	61	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	13	16	

Notes:
a. Package limited.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under Steady State conditions is 110 °C/W.

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SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		112		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 7.3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	2		4	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	µA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 3 V, V_{GS} = 10 V	3			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 0.4 A		0.472	0.567	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = 20 V, I_D = 1.3 A		2		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		78		pF
Output Capacitance	C_{oss}			11		
Reverse Transfer Capacitance	C_{rss}			4		
Total Gate Charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 1.3 A		2.2	3.3	nC
Gate-Source Charge	Q_{gs}			1.0		
Gate-Drain Charge	Q_{gd}			0.4		
Gate Resistance	R_g	f = 1 MHz	0.5	2.4	4.8	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, R_L = 50 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω		7	14	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			7	14	
Fall Time	t_f			8	16	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, R_L = 50 Ω $I_D \cong$ 1 A, V_{GEN} = 7.5 V, R_g = 1 Ω		8	16	
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			8	16	
Fall Time	t_f			9	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			6	A
Pulse Diode Forward Current	I_{SM}				3	
Body Diode Voltage	V_{SD}	I_S = 1 A, V_{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 1 A, dI/dt = 100 A/µs, T_J = 25 °C		22	33	ns
Body Diode Reverse Recovery Charge	Q_{rr}			20	30	nC
Reverse Recovery Fall Time	t_a			15		ns
Reverse Recovery Rise Time	t_b			7		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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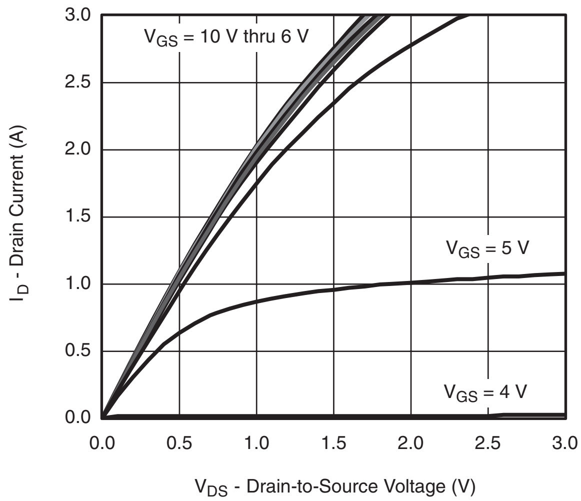
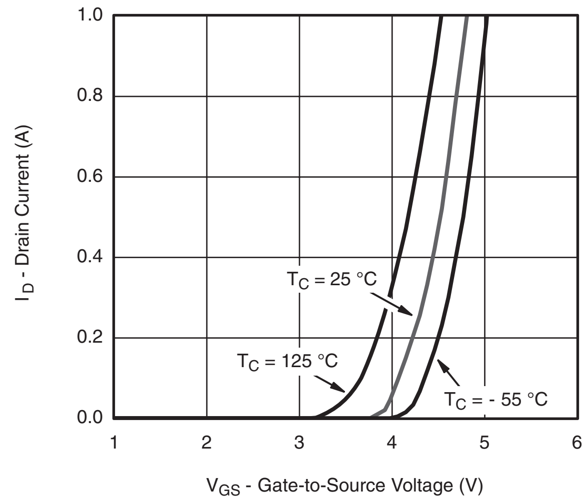
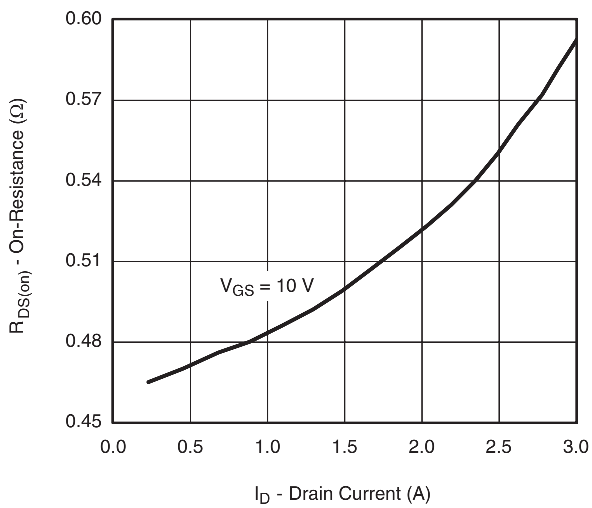
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



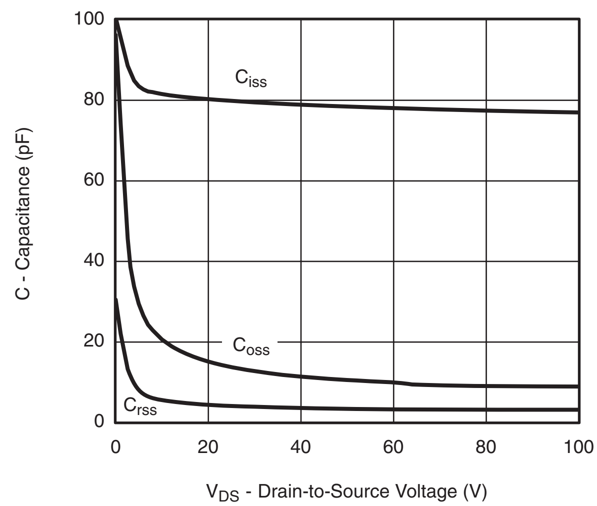
Output Characteristics



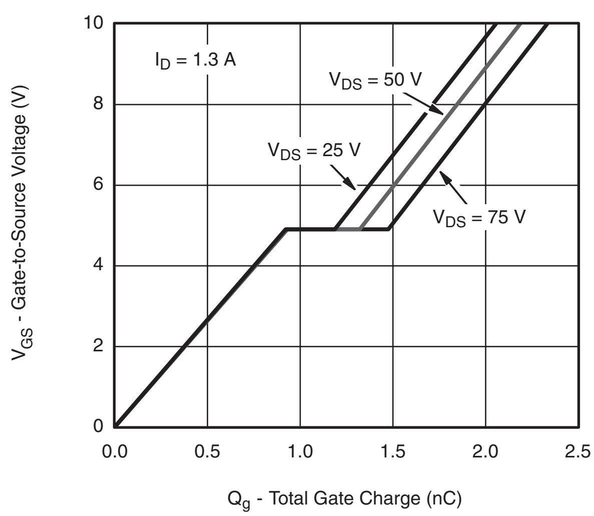
Transfer Characteristics



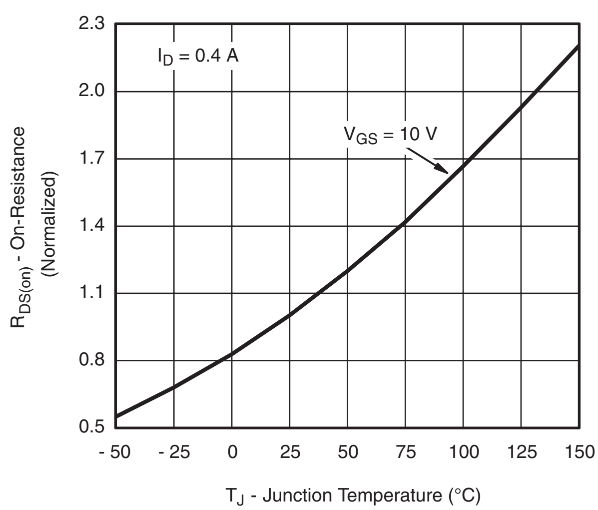
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

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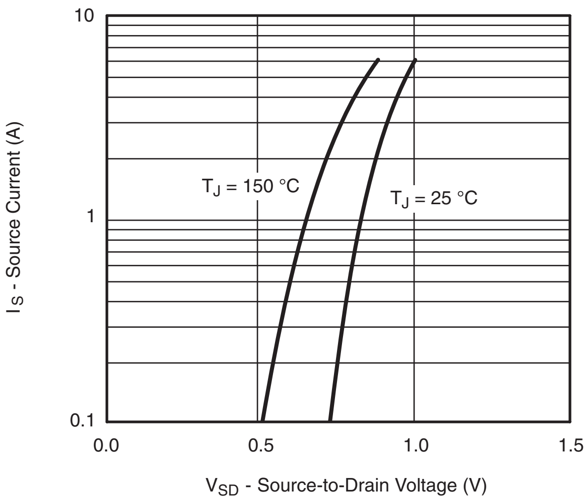
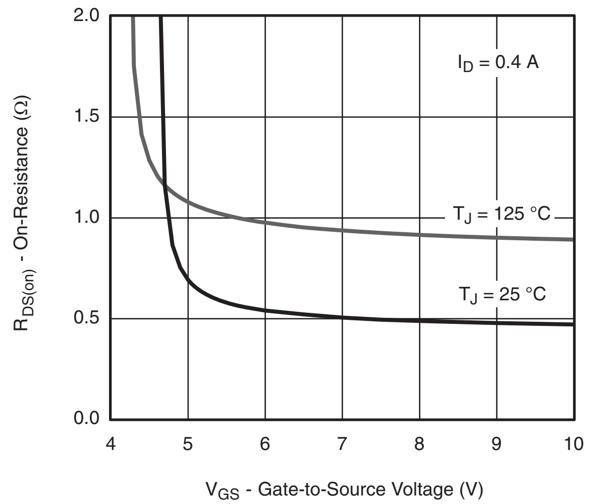
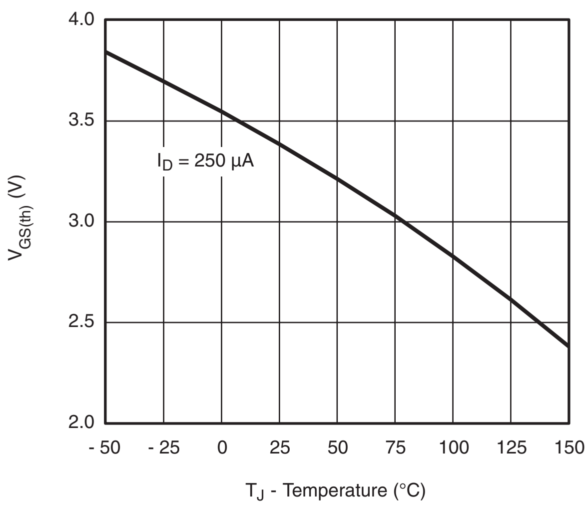
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



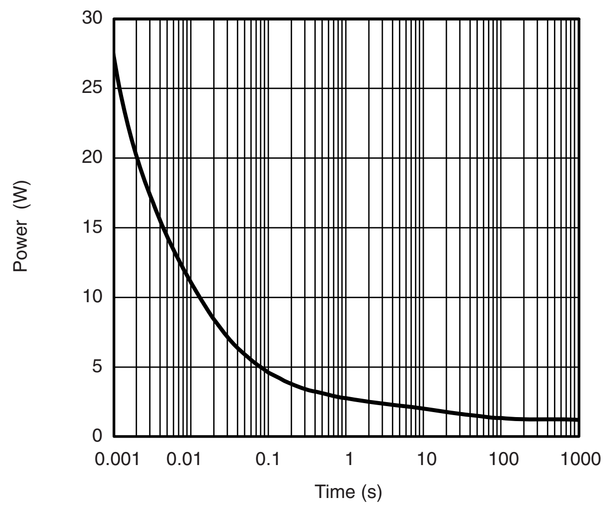
Source-Drain Diode Forward Voltage



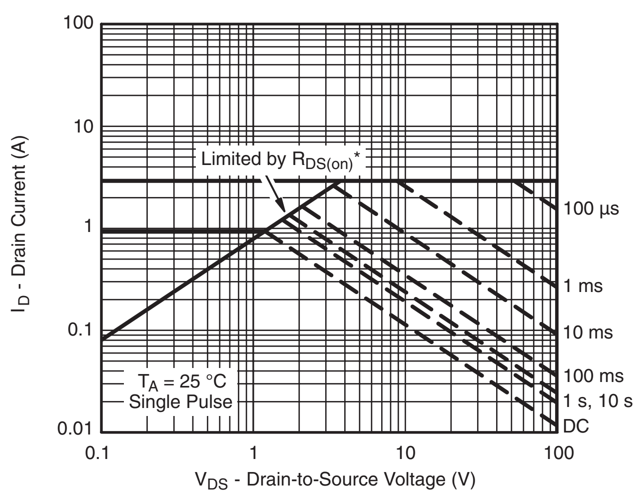
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



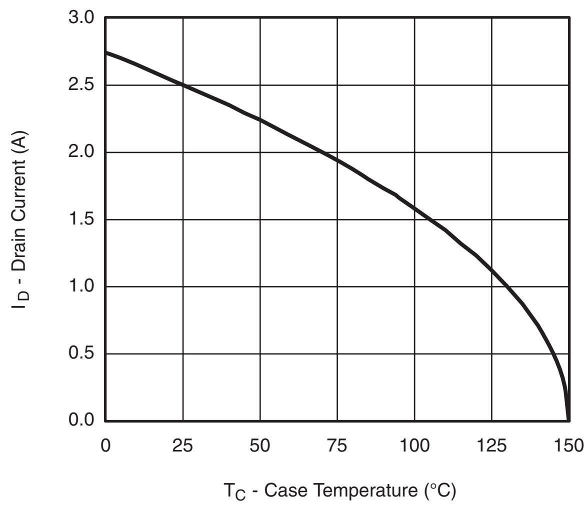
Single Pulse Power, Junction-to-Ambient



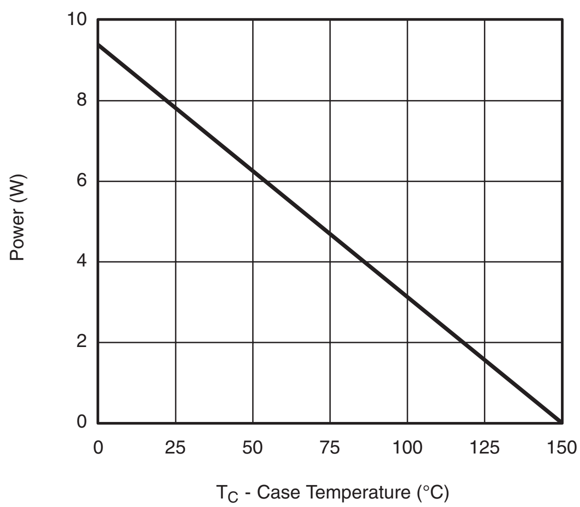
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

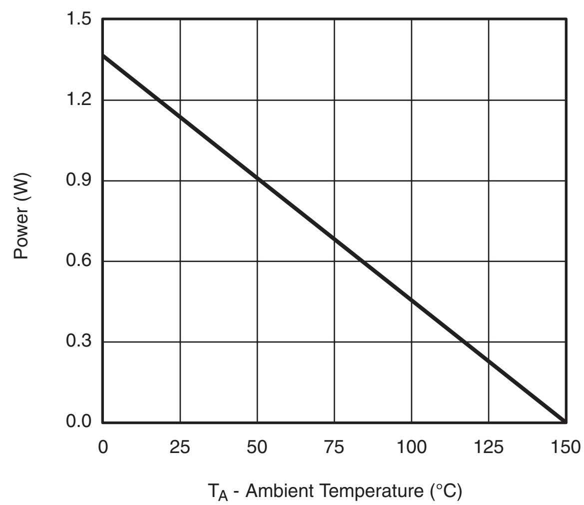
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



Power, Junction-to-Case



Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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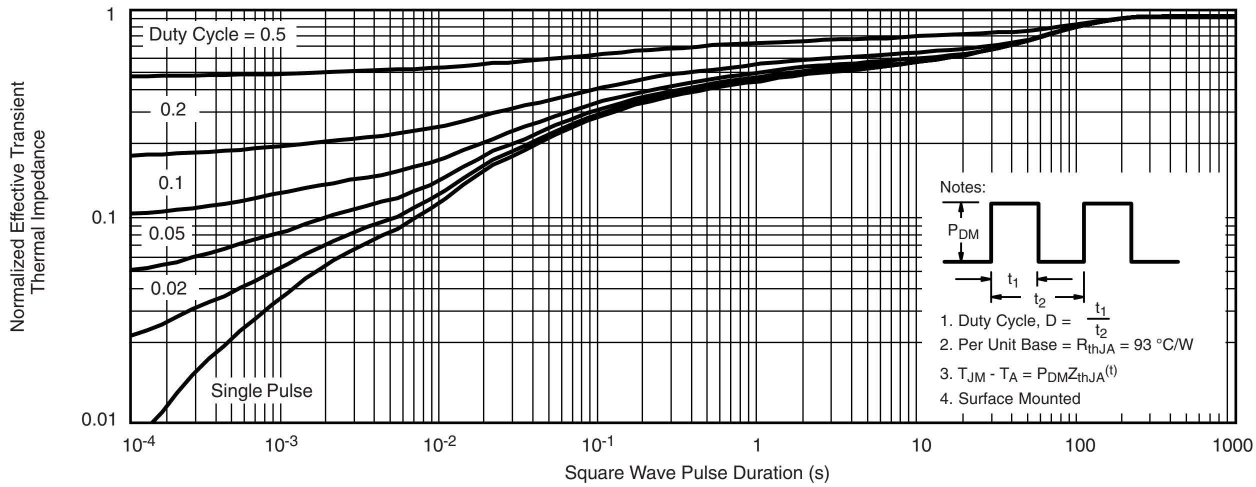
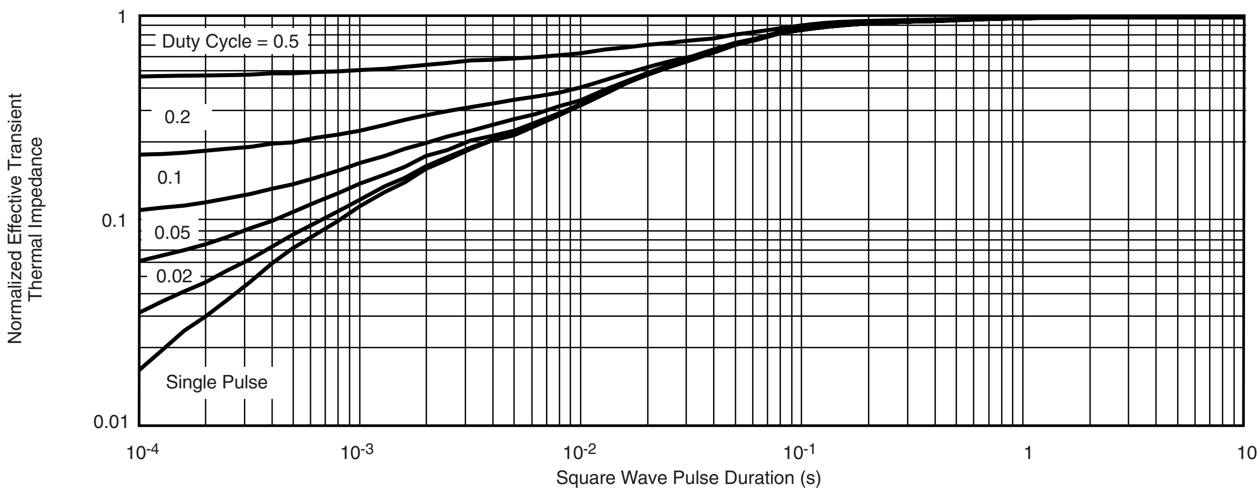


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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