CD4094B Types

CMOS
8-Stage Shift-and-Store
Bus Register

High-Voltage Types (20-Volt Rating)

■ CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

The CD4094B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

■ 3-state parallel outputs for connection to common bus
■ Separate serial outputs synchronous to both positive and negative clock edges for cascading
■ Medium speed operation -- 5 MHz at 10 V (typ.)
■ Standardized, symmetrical output characteristics
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Noise margin (full package temperature range):
 1 V at V_{DD} = 5 V   2 V at V_{DD} = 10 V
 2.5 V at V_{DD} = 15 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

■ Serial-to-parallel data conversion
■ Remote control holding register
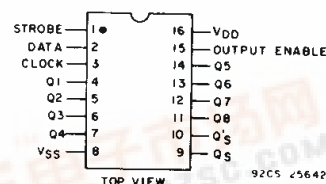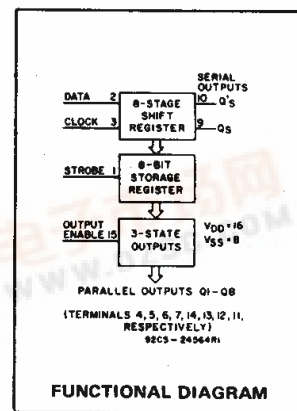■ Dual-rank shift, hold, and bus applications

FUNCTIONAL DIAGRAM

Fig. 1 – Terminal assignment.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
 Voltages referenced to V_{SS} Terminal) .... −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
 For T_A = −55°C to +100°C 500mW
 For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... −55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
 At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C
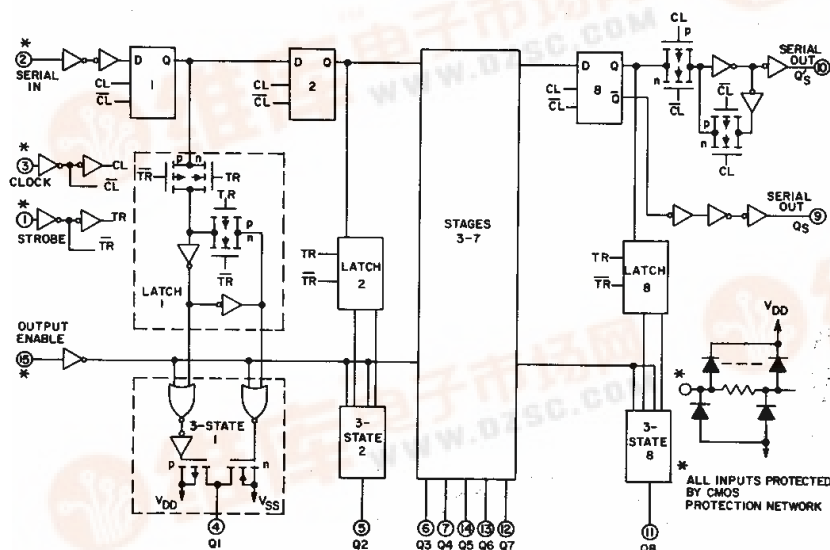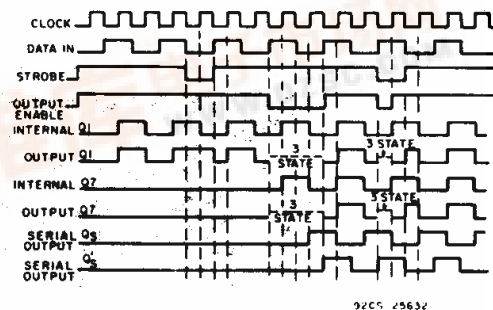

Fig. 2 – CD4094B Logic diagram.

Fig. 3 – Timing diagram.

RECOMMENDED OPERATING CONDITIONS at $T_A = 25°C$, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	125	–	ns
	10	55	–	
	15	35	–	
Clock Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	83	–	
Clock Input Frequency, f_{CL}	5	dc	1.25	MHz
	10		2.5	
	15		3	
Clock Input Rise or Fall time, t_rCL, t_fCL:*	5	–	15	μs
	10		5	
	15		5	
Strobe Pulse Width, t_W	5	200	–	ns
	10	80	–	
	15	70	–	

*If more than one unit is cascaded t_fCL (for Q_S only) should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the output driving stage for the estimated capacitive load.
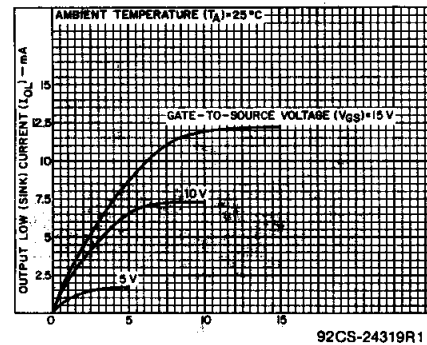
TRUTH TABLE

CL▲	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	QN	QS*	Q'S
⌐_	0	X	X	OC	OC	Q7	NC
⌐_	0	X	X	OC	OC	NC	Q7
_⌐	1	0	X	NC	NC	Q7	NC
_⌐	1	1	0	0	Q_{N-1}	Q7	NC
_⌐	1	1	1	1	Q_{N-1}	Q7	NC
⌐_	1	1	1	NC	NC	NC	Q7

▲ = Level Change   Logic 1 ≡ High
X = Don't Care   Logic 0 ≡ Low
NC = No Change
OC = Open Circuit

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output.

Fig. 4 — Typical output low (sink) current characteristics.

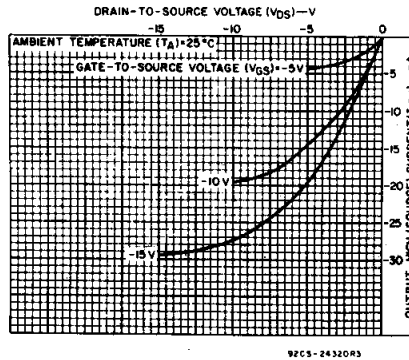Fig. 5 — Minimum output low (sink) current characteristics.

Fig. 6 — Typical output high (source) current characteristics.
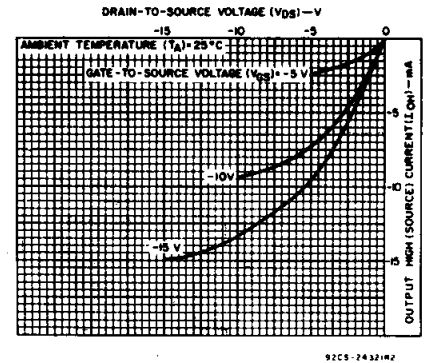

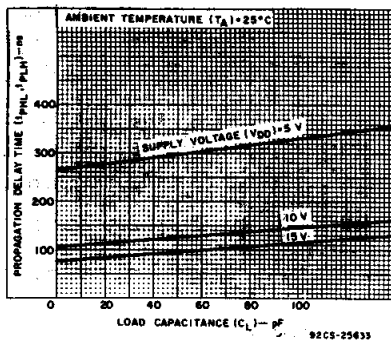Fig. 7 — Minimum output high (source) current characteristics.

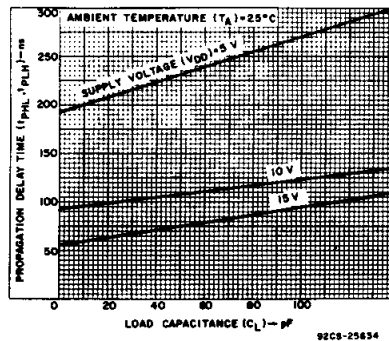Fig. 8 — Clock-to-serial output Q_S propagation delay vs C_L.

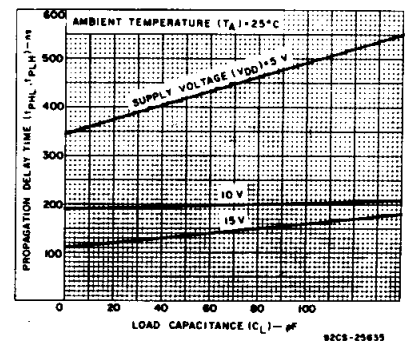Fig. 9 — Clock-to-serial output Q'_S propagation delay vs C_L.

Fig. 10 — Clock-to-parallel output propagation delay vs C_L.

"CD4094B-MIL"

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER-ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)				+25			UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	V
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12		$±10^{-4}$	±0.4	μA
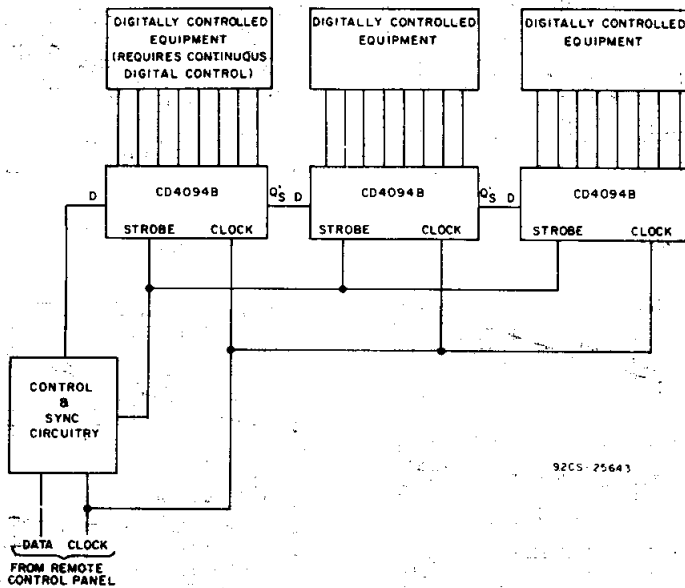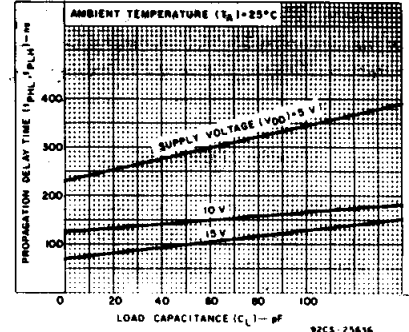
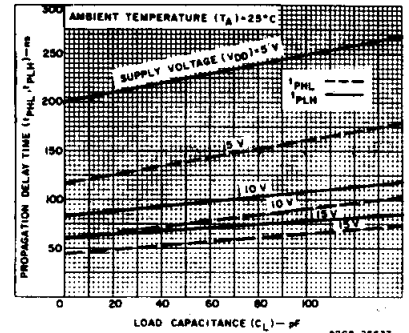Fig. 11 – Strobe-to-parallel output propagation delay vs C_L.

Fig. 12 – Output enable-to-parallel output propagation delay vs C_L.

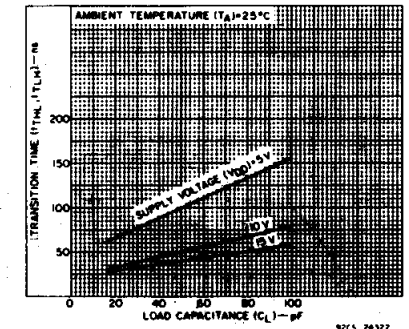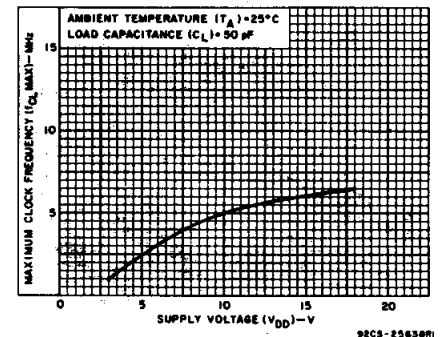Fig. 13 – Typical transition time vs. load capacitance.

Fig. 15 – Typical maximum-clock-frequency vs. supply voltage.

Fig. 14 – Remote control holding register.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A=25°C$; Input t_r, $t_f = 20\,ns$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$

CHARACTERISTIC	VDD (V)	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}	5	–	300	600	
Clock to Serial Output Q_S	10	–	125	250	ns
	15	–	95	190	
	5	–	230	460	
Clock to Serial Output Q'_S	10	–	110	220	ns
	15	–	75	150	
	5	–	420	840	
Clock to Parallel Output	10	–	195	390	ns
	15	–	135	270	
	5	–	290	580	
Strobe to Parallel Output	10	–	145	290	ns
	15	–	100	200	
Output Enable to Parallel Output: t_{PHZ}, t_{PZH}	5	–	140	280	
	10	–	60	120	ns
	15	–	45	90	
	5	–	100	200	
t_{PLZ}, t_{PZL}	10	–	50	100	ns
	15	–	40	80	
Minimum Strobe Pulse Width, t_W	5	–	100	200	
	10	–	40	80	ns
	15	–	35	70	
Minimum Clock Pulse Width, t_W	5	–	100	200	
	10	–	50	100	ns
	15	–	40	83	
Minimum Data Setup Time, t_S	5	–	60	125	
	10	–	30	55	ns
	15	–	20	35	
Transition Time; t_{THL}, t_{TLH}	5	–	100	200	
	10	–	50	100	ns
	15	–	40	80	
Maximum Clock Input Rise or Fall Time, t_rCL, t_fCL	5	15	–	–	
	10	5	–	–	µs
	15	5	–	–	
Maximum Clock Input Frequency, f_{CL}	5	1.25	2.5	–	
	10	2.5	5	–	MHz
	15	3	6	–	
Input Capacitance C_{IN} (Any Input)	–	–	5	7.5	pF

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).
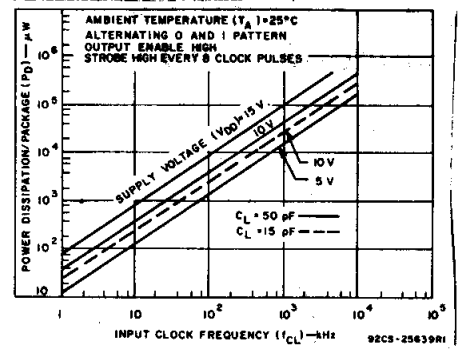

Fig. 16 — Dynamic power dissipation vs input clock frequency.
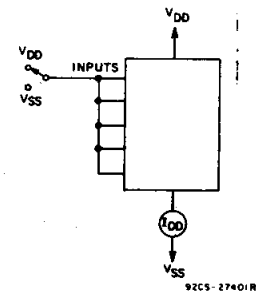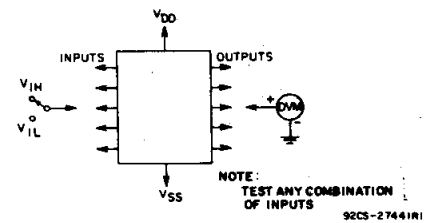

Fig. 17 — Quiescent device current test circuit.
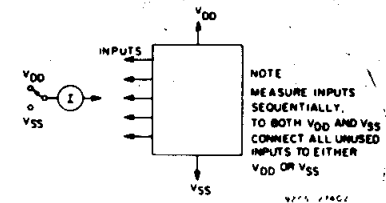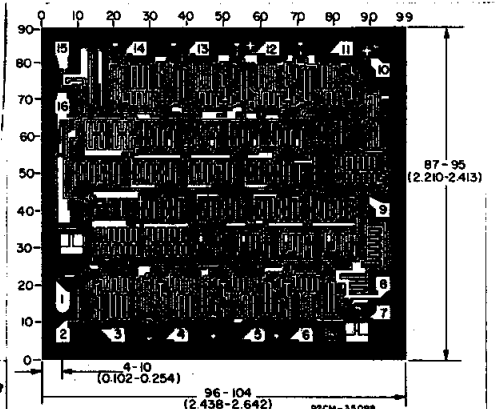

Fig. 18 — Input voltage test circuit.

Fig. 19 — Input current test circuit.

Dimensions and Pad Layout for CD4094B Chip.

3

COMMERCIAL CMOS HIGH VOLTAGE ICs

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
7702501EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4094BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4094BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4094BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4094BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4094BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4094BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4094BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4094BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4094BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4094BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4094BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4094BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4094BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

Reel Diameter

Reel Width (W1)

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1	Q2
Q3	Q4

Q1	Q2
Q3	Q4

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4094BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4094BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4094BNSR	SO	NS	16	2000	346.0	346.0	33.0
CD4094BPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

J (R−GDIP−T**)   CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN
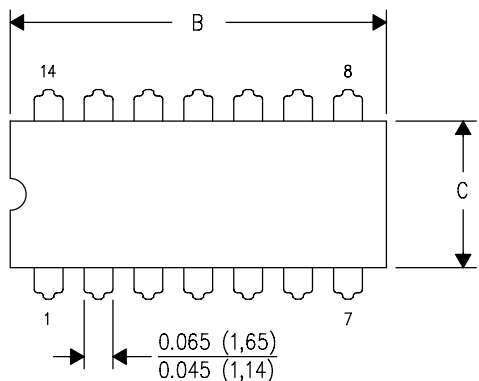
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\dfrac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\dfrac{0.060\ (1,52)}{0.015\ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\dfrac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

A

0°−15°

$\dfrac{0.014\ (0,36)}{0.008\ (0,20)}$
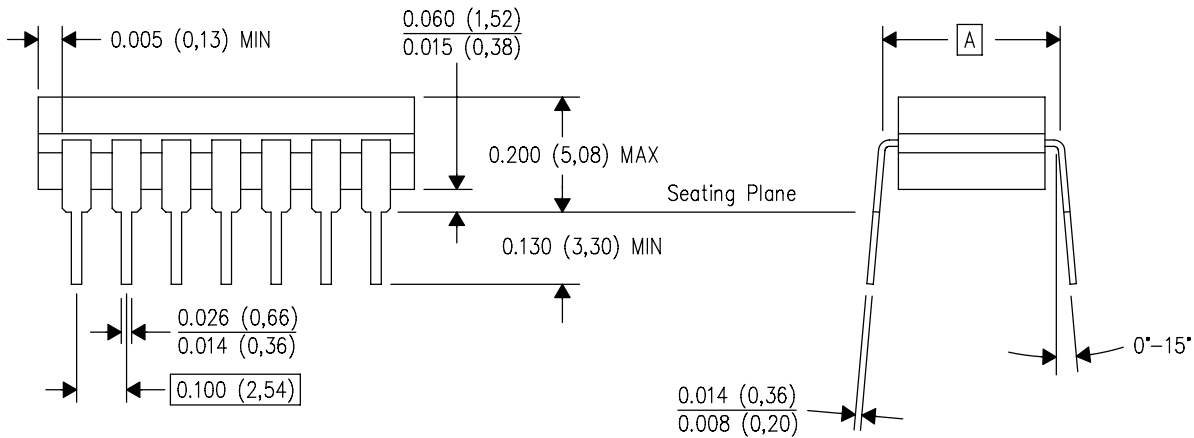
4040083/F 03/03

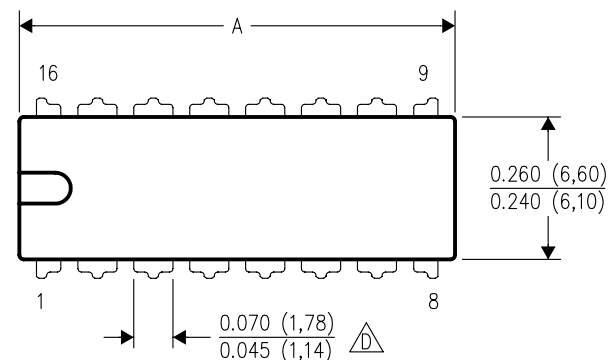NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

N (R−PDIP−T**)
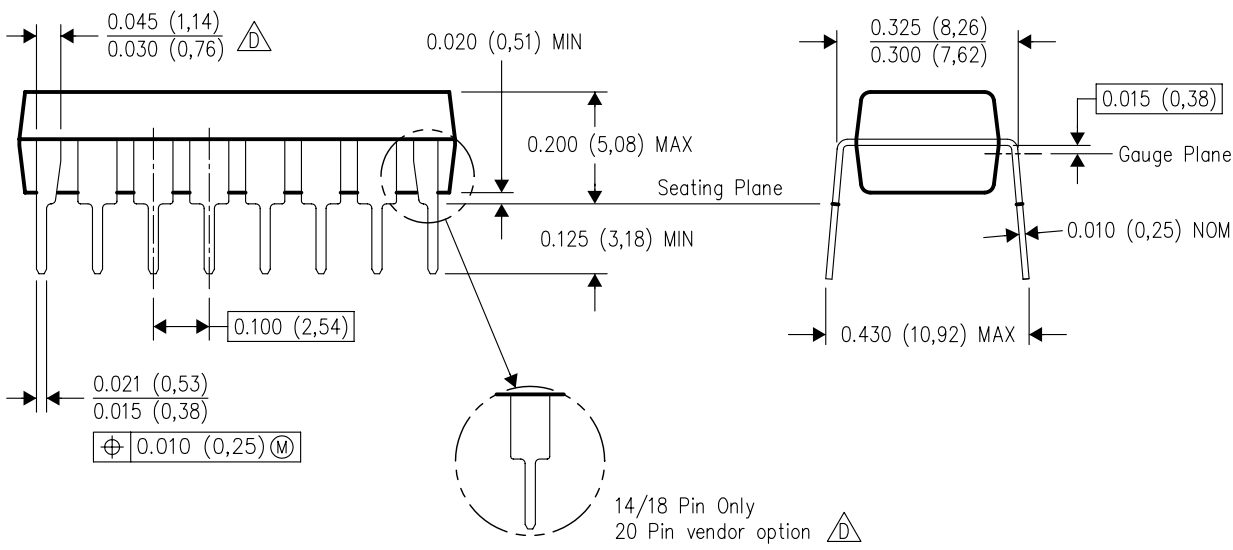
PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION (C)	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) (D)

0.045 (1,14) / 0.030 (0,76) (D)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) (M)

14/18 Pin Only
20 Pin vendor option (D)

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002
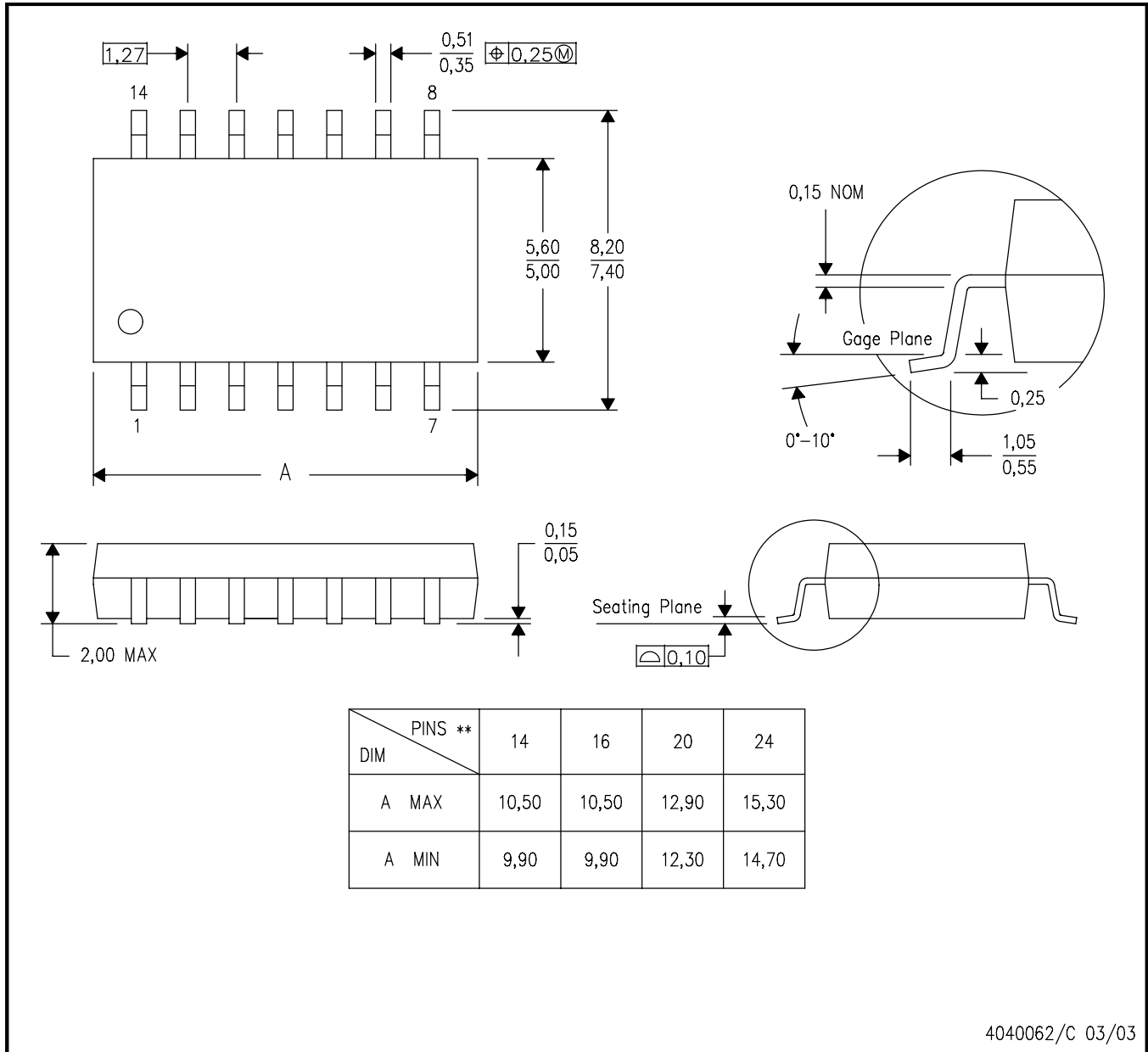
NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
    (C) Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
    (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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MECHANICAL DATA

NS (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

1,27

$\frac{0,51}{0,35}$ ⊕ 0,25Ⓜ

14   8

$\frac{5,60}{5,00}$ $\frac{8,20}{7,40}$

1   7

A

0,15 NOM

Gage Plane

0,25

0°–10° $\frac{1,05}{0,55}$

$\frac{0,15}{0,05}$

2,00 MAX

Seating Plane

⌒ 0,10

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
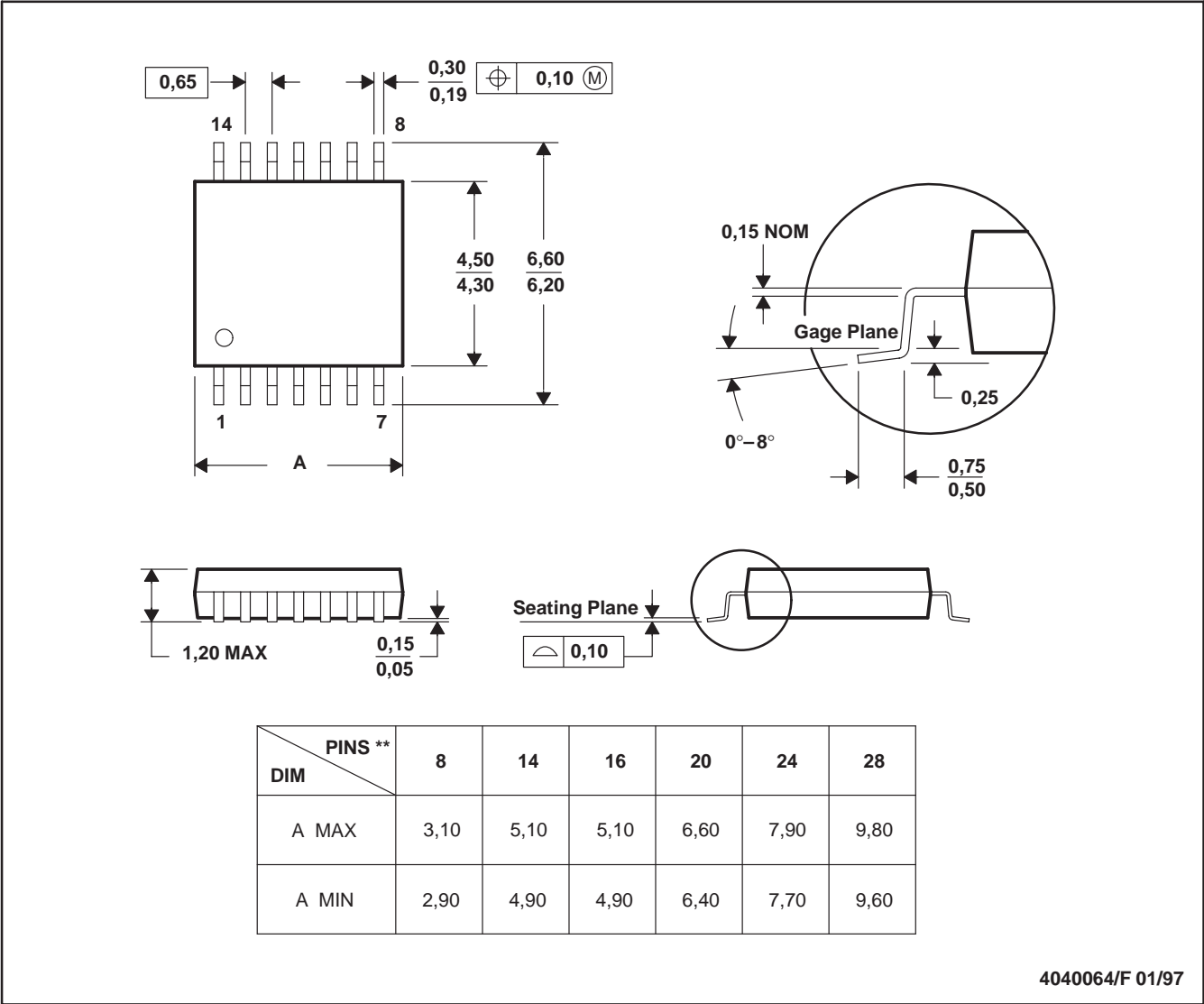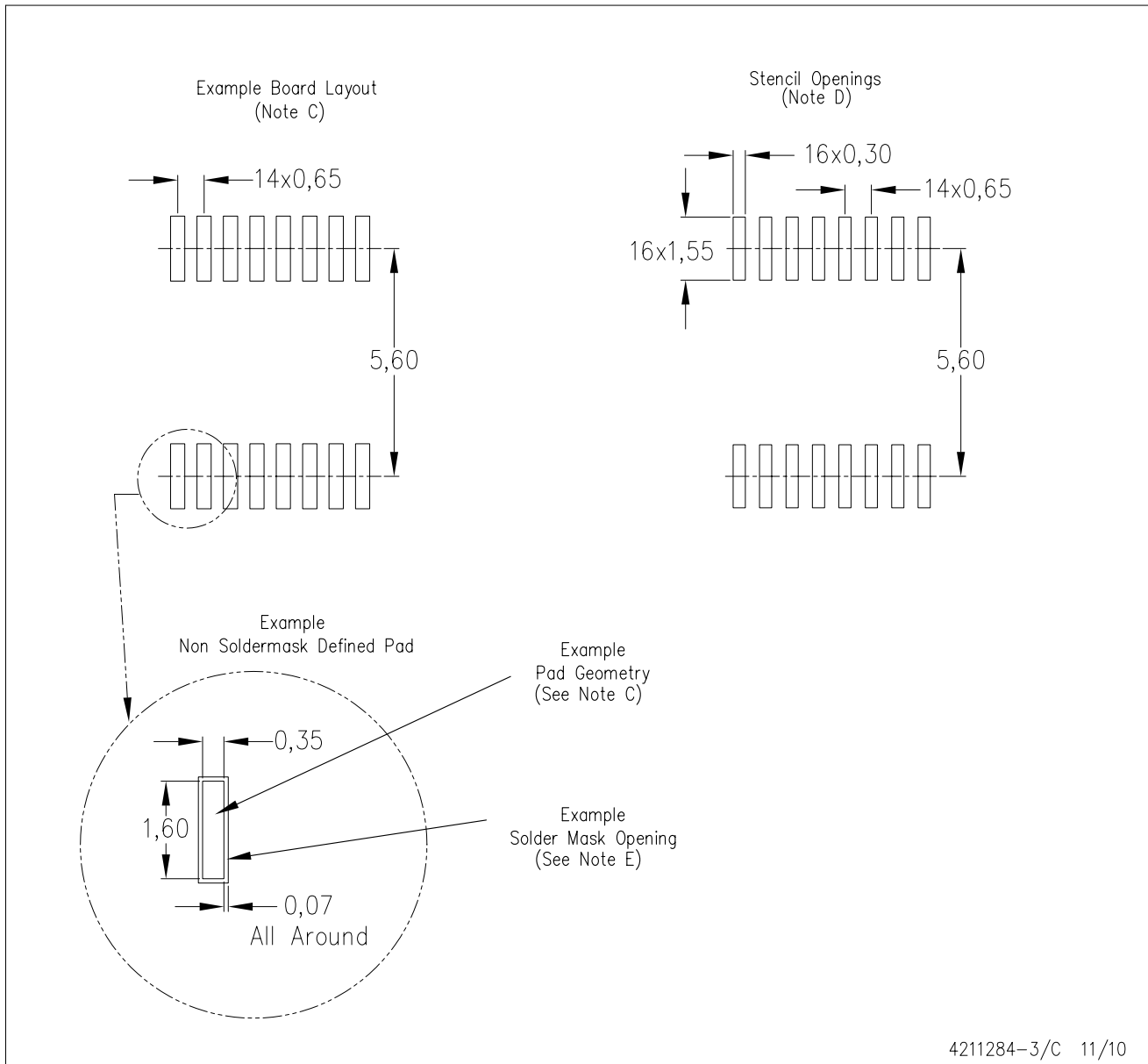C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PW (R-PDSO-G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

←— 14x0,65

5,60

Stencil Openings
(Note D)

16x0,30

14x0,65

16x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211284-3/C 11/10

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC-7351 is recommended for alternate designs.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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